

# **MELSEC STlite Series**

Modular Input/Output System

Quick Start Guide

# About this Manual

The texts, illustrations, diagrams, and examples contained in this manual are intended exclusively as support material for the explanation, handling and operation of the components of the MELSEC STlite Series.

If you have any questions concerning the programming and operation of the equipment described in this manual, please contact your relevant sales office or department (refer to back of cover).

Current information and answers to frequently asked questions are also available through the Internet ([www.mitsubishi-automation.com](http://www.mitsubishi-automation.com))

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| <b>Quick Start Guide<br/>MELSEC STlite Series<br/>Article no.:</b> |                |                                      |
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|  |                |                                      |

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# Safety Information

## General Safety Information

### For use by qualified staff only

This manual is only intended for use by properly trained and qualified electrical technicians who are fully acquainted with the relevant automation technology safety standards. All work with the hardware described, including system design, installation, configuration, maintenance, service and testing of the equipment, may only be performed by trained electrical technicians with approved qualifications who are fully acquainted with all the applicable automation technology safety standards and regulations. Any operations or modifications to the hardware and/or software of our products not specifically described in this manual may only be performed by authorised Mitsubishi Electric staff.

### Proper use of the products

The devices of the MELSEC STlite series are only intended for the specific applications explicitly described in this manual. All parameters and settings specified in this manual must be observed. The products described have all been designed, manufactured, tested and documented in strict compliance with the relevant safety standards. Unqualified modification of the hardware or software or failure to observe the warnings on the products and in this manual may result in serious personal injury and/or damage to property. Only peripherals and expansion equipment specifically recommended and approved by Mitsubishi Electric may be used with the devices of the MELSEC STlite series.

All and any other uses or application of the products shall be deemed to be improper.

### Relevant safety regulations

All safety and accident prevention regulations relevant to your specific application must be observed in the system design, installation, configuration, maintenance, servicing and testing of these products.

The regulations listed below are particularly important in this regard. This list does not claim to be complete, however; you are responsible for being familiar with and conforming to the regulations applicable to you in your location.

- VDE Standards
  - VDE 0100  
Regulations for the erection of power installations with rated voltages below 1000 V
  - VDE 0105  
Operation of power installations
  - VDE 0113  
Electrical installations with electronic equipment
  - VDE 0160  
Electronic equipment for use in power installations
  - VDE 0550/0551  
Regulations for transformers
  - VDE 0700  
Safety of electrical appliances for household use and similar applications
  - VDE 0860  
Safety regulations for mains-powered electronic appliances and their accessories for household use and similar applications
- Fire safety regulations
- Accident prevention regulations
  - Electrical systems and equipment

**Safety warnings in this manual**

In this manual warnings that are relevant for safety are identified as follows:



**DANGER:**

*Failure to observe the safety warnings identified with this symbol can result in health and injury hazards for the user.*



**CAUTION:**

*Failure to observe the safety warnings identified with this symbol can result in damage to the equipment or other property.*

## General Safety Information and Precautions

The following safety precautions are intended as a general guideline for using PLC systems together with other equipment. These precautions must always be observed in the design, installation and operation of all control systems.



### **DANGER:**

- **Observe all safety and accident prevention regulations applicable to your specific application. Always disconnect all power supplies before performing installation and wiring work or opening any of the assemblies, components and devices.**
- **Assemblies, components and devices must always be installed in a shockproof housing fitted with a proper cover and fuses or circuit breakers.**
- **Devices with a permanent connection to the mains power supply must be integrated in the building installations with an all-pole disconnection switch and a suitable fuse.**
- **Check power cables and lines connected to the equipment regularly for breaks and insulation damage. If cable damage is found immediately disconnect the equipment and the cables from the power supply and replace the defective cabling.**
- **Before using the equipment for the first time check that the power supply rating matches that of the local mains power.**
- **Take appropriate steps to ensure that cable damage or core breaks in the signal lines cannot cause undefined states in the equipment.**
- **You are responsible for taking the necessary precautions to ensure that programs interrupted by brownouts and power failures can be restarted properly and safely. In particular, you must ensure that dangerous conditions cannot occur under any circumstances, even for brief periods. EMERGENCY OFF must be switched forcibly, if necessary.**
- **EMERGENCY OFF facilities conforming to EN 60204/IEC 204 and VDE 0113 must remain fully operative at all times and in all PLC operating modes. The EMERGENCY OFF facility reset function must be designed so that it cannot ever cause an uncontrolled or undefined restart.**
- **You must implement both hardware and software safety precautions to prevent the possibility of undefined control system states caused by signal line cable or core breaks.**
- **When using modules always ensure that all electrical and mechanical specifications and requirements are observed exactly.**

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# Symbols used in the manual

## Use of instructions

Instructions concerning important information are marked separately and are displayed as follows:

### NOTE

| Text of instruction

## Use of numbering in the figures

Numbering within the figures is displayed by white numbers within black circles and is explained in a table following it using the same number, e.g.:

① ② ③ ④

## Use of handling instructions

Handling instructions are steps that must be carried out in their exact sequence during startup, operation, maintenance and similar operations.

They are numbered consecutively (black numbers in white circles):

- ① Text.
- ② Text.
- ③ Text.

## Use of footnotes in tables

Instructions in tables are explained in footnotes underneath the tables (in superscript). There is a footnote character at the appropriate position in the table (in superscript).

If there are several footnotes for one table then these are numbered consecutively underneath the table (black numbers in white circle, in superscript):

- ① Text
- ② Text
- ③ Text

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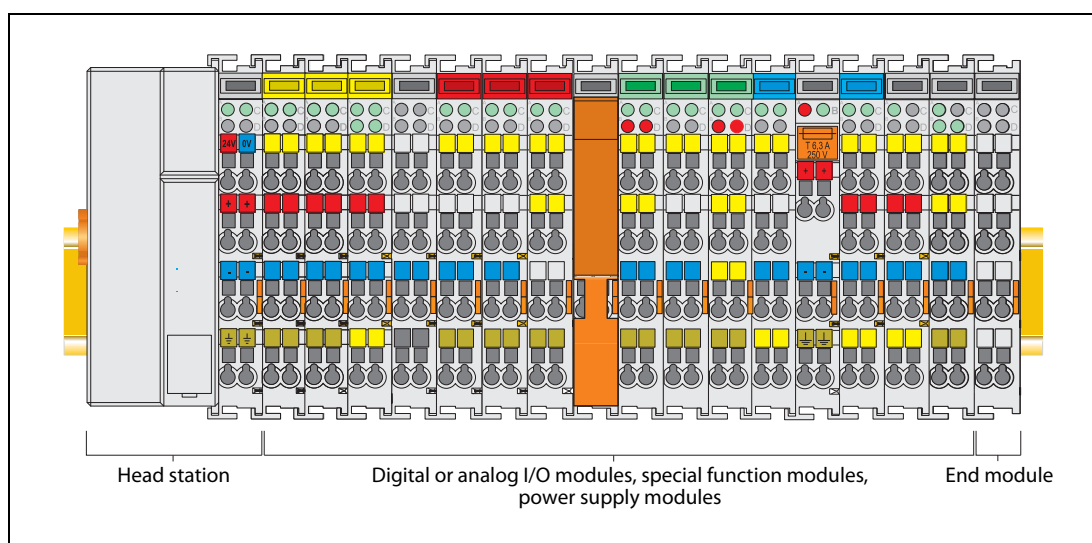
# 1 Introduction

This Quick Start Guide explains the basic procedures for the first-time use of the modules of the MELSEC STlite series.

For additional information and a detailed mounting and wiring description of the MELSEC STlite series, please refer to the installation manual.

## 1.1 System Configuration

STlite is a modular, field bus independent I/O system. It is comprised of a head station and up to 64 connected modules for any type of signal. Together, these make up the field bus node. An end module completes the node.



**Fig. 1-1:** Field bus node

Head stations are available for different field bus systems, such as Profibus DP, Ethernet TCP/IP or CC-Link.

The head station contains the field bus interface, electronics and a power supply terminal. The field bus interface connects the node to the relevant field bus. The electronics process the data of the I/O modules or special function modules and make it available for the field bus communication. The 24 V system supply and the 24 V field supply are fed in via the integrated power supply terminal.

Modules for diverse digital and analog I/O functions as well as special functions can be connected to the head station. Populating the nodes with STlite modules is based on the requirements of the application. The communication between the head station and the bus modules is carried out via an internal bus.

STlite has a clear port level with LEDs for status indication, insertable markers and pullout group identification plate bracket. The 3-wire technology supplemented by a ground wire connection allows for direct sensor/actuator wiring.

"ST" means "Slice Type terminal", and refers to the narrow width of the modules (only 12 mm!).

### 1.1.1 Components of the STlite Series

| Type of module         |             | Name       | ID number | Description   | Color code            |
|------------------------|-------------|------------|-----------|---|-----------------------|
| Head stations          | Profibus DP | STL-PB1    | 51247152  | Head station for the connection to Profibus DP            | Colorless             |
|                        | CC-Link     | STL-BT1    | 51247154  | Head station for the connection to CC-Link                |                       |
|                        | Ethernet    | STL-ETH1   | 51247153  | Head station for the connection to Ethernet TCP/IP        |                       |
| Power supply modules   |             | STL-PS     | 51205036  | Power supply modules<br>24 V DC                           | passive               |
|                        |             | STL-BPS    | 51244880  |   | with bus power supply |
| Digital input modules  |             | STL-DI8-V1 | 51205052  | 8 inputs for source type sensors, 24 V DC                 | response time 0.2 ms  |
|                        |             | STL-DI8-V2 | 51205053  |   | response time 3.0 ms  |
| Digital output modules |             | STL-DO4    | 51205045  | 4 transistor outputs, 24 V DC, 0.5 A, source type         | Red                   |
|                        |             | STL-DO8    | 51205043  | 8 transistor outputs, 24 V DC, 0.5 A, source type         |                       |
|                        |             | STL-RO2    | 51205044  | 2 relay outputs 230 V AC / 30V DC, 500 VA/60 W            |                       |
| Analog input modules   | Voltage     | STL-AD2-V  | 51205046  | 2 inputs 0 to 10 V  | Green                 |
|                        |             | STL-AD4-V1 | 51205049  | 4 inputs 0 to 10 V  |                       |
|                        |             | STL-AD4-V2 | 51205050  | 4 inputs -10 to 10 V                                      |                       |
|                        | Current     | STL-AD2-I  | 51205047  | 2 inputs 4 to 20 mA                                       |                       |
|                        |             | STL-AD4-I  | 51205051  | 4 inputs 4 to 20 mA                                       |                       |
|                        | Temperature | STL-TI2    | 51205048  | 2 inputs for Pt100 resistance thermometers                |                       |
| Analog output modules  | Voltage     | STL-DA2-V  | 51205042  | 2 outputs 0 to 10 V                                       | Blue                  |
|                        |             | STL-DA4-V1 | 51205038  | 4 outputs 0 to 10 V                                       |                       |
|                        |             | STL-DA4-V2 | 51205039  | 4 outputs -10 to 10 V                                     |                       |
|                        | Current     | STL-DA2-I  | 51205041  | 2 outputs 4 to 20 mA                                      |                       |
|                        |             | STL-DA4-I  | 51205040  | 4 outputs 4 to 20 mA                                      |                       |
| Encoder module         |             | STL-ENC    | 51205116  | Input module for incremental encoder with RS422 interface | Colorless             |
| Counter module         |             | STL-C100   | 51244881  | Forward/reverse counter, 24 V DC, max. frequency 100 kHz  |                       |
| Interface module       |             | STL-SSI    | 51205057  | Input module for SSI encoder                              |                       |
| Bus end module         |             | STL-ET     | 51205037  | End module for the termination of the internal bus        |                       |

**Tab. 1-1:** Head stations and modules of the STlite series

#### NOTES

For the specifications of all available STlite modules please refer to the installation manual of the STlite series.

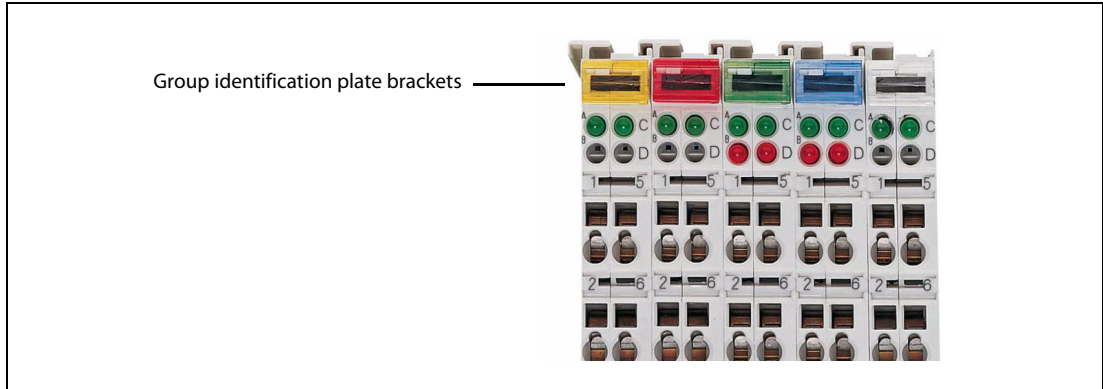
For the process images of the modules, please refer to the appendix of this manual.

### 1.1.2 Identification of the Modules

Please note that the name of the module is not printed on the module. However, there are several methods to identify a module.

#### Color coded group identification plate bracket

The pullout group marker carriers of the module offer an rough distinguishing mark.



**Fig. 1-2:** The module type can easily be recognised by the color of the group marker carrier.

| Color of group identification plate brackets | Type of module          |                     |
|--|-------------------------|---------------------|
| Yellow                                       | Digital input module    |                     |
| Red  | Digital output module   |                     |
| Green  | Analog input module     |                     |
| Blue   | Analog output module    |                     |
| Colorless                                    | Special function module | Encoder module      |
|  |                         | Counter module      |
|  |                         | Interface module    |
|  | System module           | Head station        |
|  |                         | Power supply module |
|  |                         | Bus end module      |

**Tab. 1-2:** Color code of the STlite series

#### ID number of the module

The ID number, which is unique for each type of module (see table 1-1), is printed on the front side of the modules.



**Fig. 1-3:** ID number at the front of a module

**Type label of the modules**

A brief description is printed on the side of each module.



**Fig. 1-4:** Example for a type label

## 2 Profibus DP

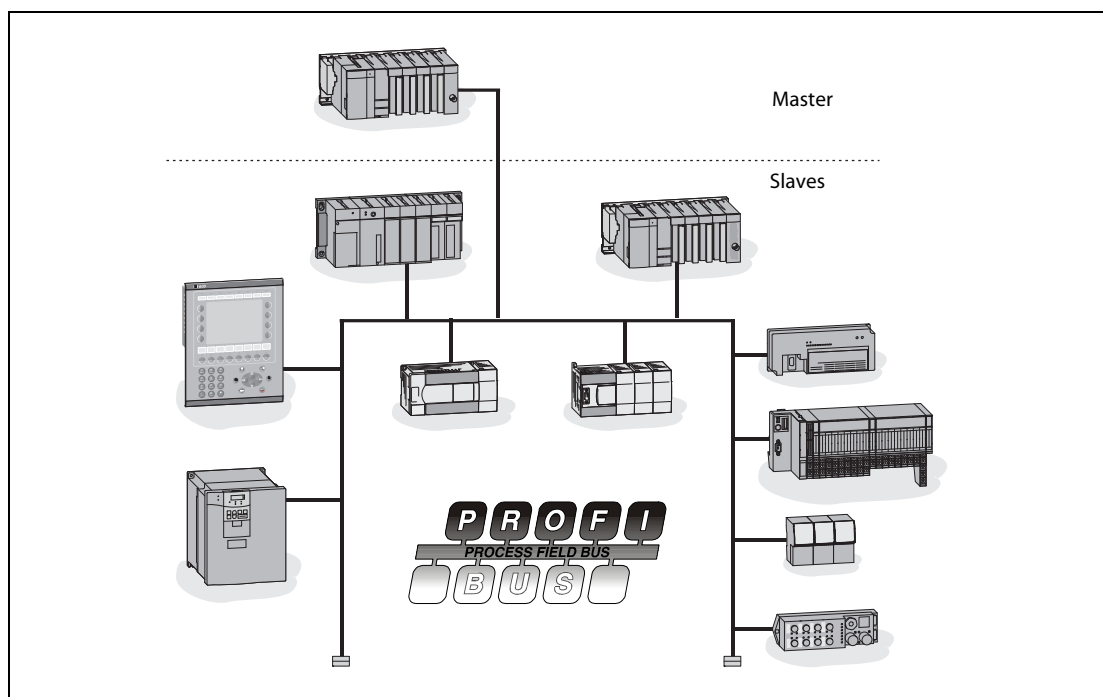
### 2.1 Overview

Profibus is one of the most widely used automation networks in Europe. It provides a wide possible range of compatible devices while delivering fast and robust communication.

Profibus offers users the option to mix devices from different companies. It is an open network ranging from simple I/O stations through to complex PLCs. The network allows extremely fast data exchange with a wide variety of slave devices.

Profibus DP (Decentralized Peripherals) is used to operate sensors and actuators via a centralized controller in production (factory) automation applications.

As this is an open network, Mitsubishi Profibus units can also be connected to master and slave devices from other manufacturers.



**Fig. 2-1:** Typical Profibus configuration

#### Structure

A Profibus DP system consists of a master and up to 124 slaves.

- **Master:** A Profibus DP Master exchanges the data with the slaves via Profibus DP and controls the bus. It transfers the data between a supervisory control (e. g. a PLC) and the decentralized peripheral equipment. The master cyclically reads the input data from the slaves and cyclically writes the output data to the slaves
- **Slave:** Profibus DP slaves are the link to the field side. They edit the input data of the peripheral equipment for the communication with the master and output the master data to the peripheral equipment.

All field devices are typically connected in a line structure with up to 32 nodes (master and slaves) in one segment. The beginning and end of each segment must be terminated with a resistor. These resistors are usually implemented as optionally activatable in the devices or plugs. If there are more than 32 nodes or the network span is being extended, repeaters must be used to link the networks.

Transmission speeds from 9.6 kbit/s to 12 Mbit/s can be used. The maximum cable length of a bus segment is limited from 100 to 1200 m, depending on the bit rate used. With up to 3 repeaters allowed, the maximum distance between two stations is 400 to 4800 m.

**Cable types**

To help reduce costs Profibus DP uses RS 485 technology with shielded 2-wire cabling.



## 2.2 Head Station STL-PB1 (Profibus DP)

The head station STL-PB1 serves as Profibus DP slave. It displays the peripheral data of all connected STlite modules on Profibus DP.



**Fig. 2-2:** Head station STL-PB1 for Profibus DP (with connected digital input module)

In the initialization phase the head station determines the physical structure of the node and creates a process image from this with all inputs and outputs. I/O modules with a bit width smaller than 8 can be combined to form one byte in order to optimize the address space.

In addition the possibility exists to deactivate projected I/O modules. In this manner the physical structure of the node can be individually designed with regard to the peripheral signals, without undertaking any changes to an already existing control application. This is done by correspondingly parametering the modules with the aid of the planning environment (for instance, GX Configurator-DP).

The diagnostics concept is based on an identification and channel based diagnostics in accordance with EN 50170-2 (Profibus). Thus it is not necessary to program modules for the evaluation of manufacturer specific diagnostics information.

### NOTE

For the specifications of the head station STL-PB1 please refer to the installation manual of the STlite series.

2.2.1 View

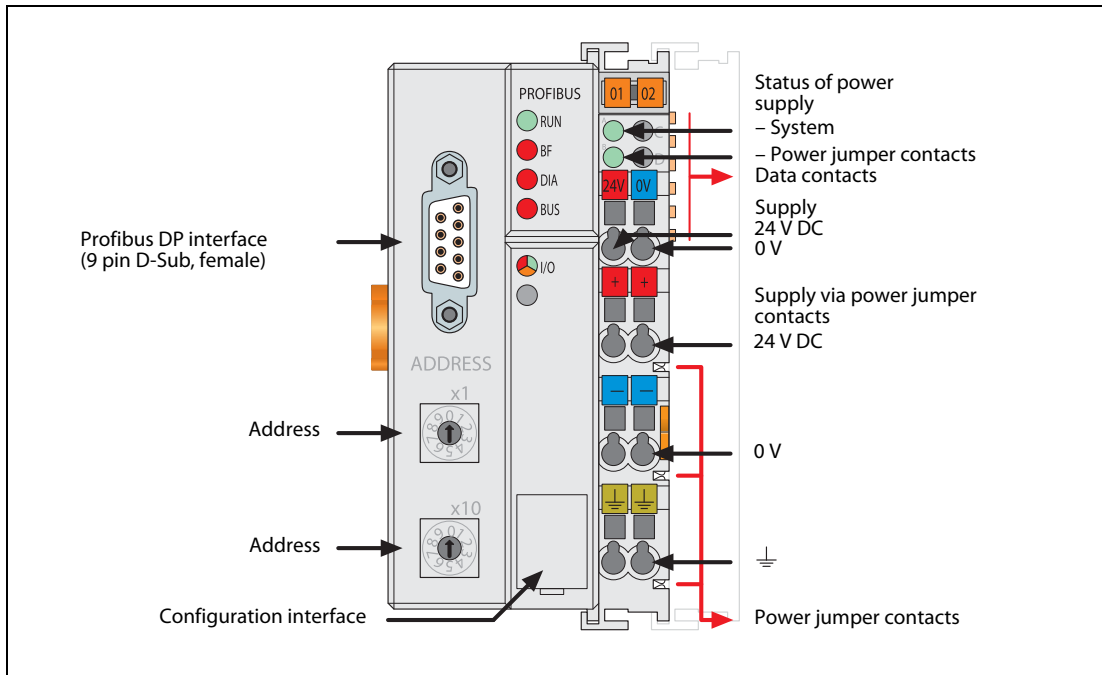


Fig. 2-3: Head station STL-PB1 (Profibus DP)

2.2.2 Device Supply

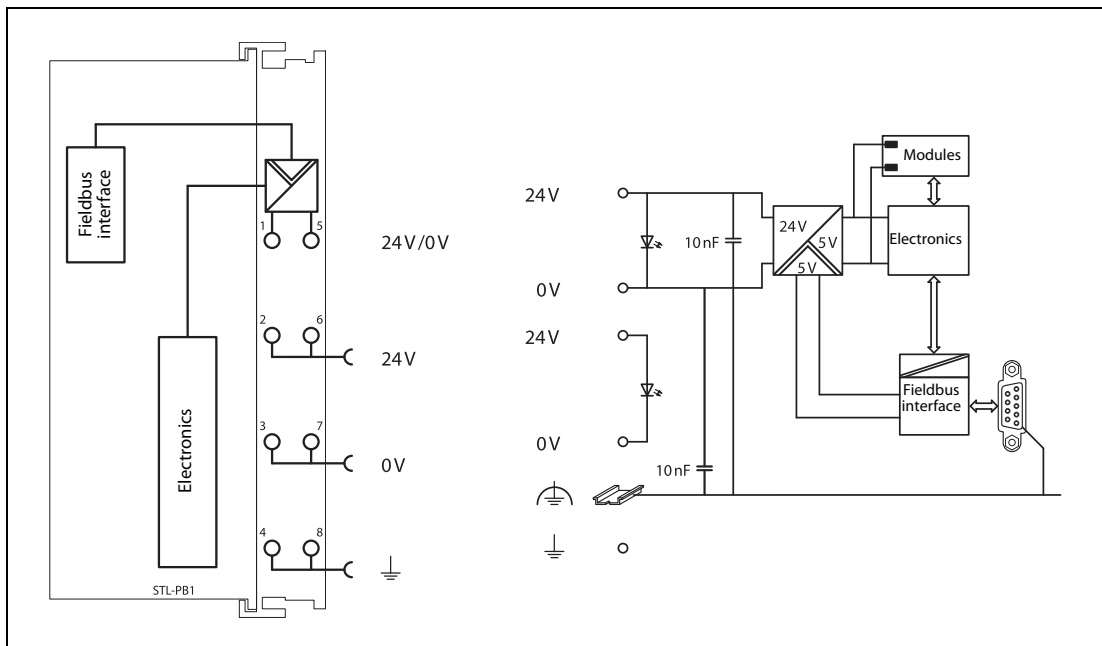


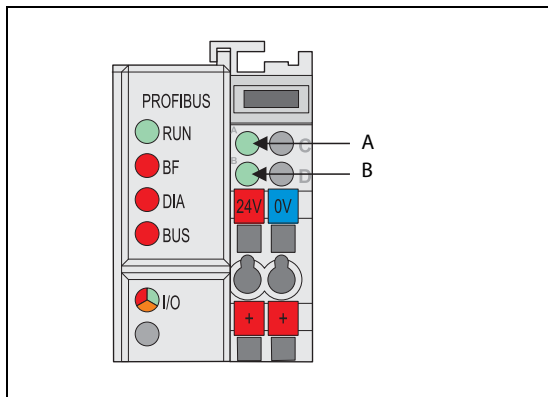
Fig. 2-4: Block diagram for the head station STL-PB1 (Profibus DP)

The device supply is intended both for the system and the field units. Two external supply voltages are required:

- 24 V DC for the head station
- 24 V DC for the connected STlite modules (forwarded via the power jumper contacts)

The fieldbus interface is supplied with electrically isolated voltage from the internal system supply module.

### 2.2.3 Display Elements



**Fig. 2-5:** The operating condition of the head station is signaled via LEDs.

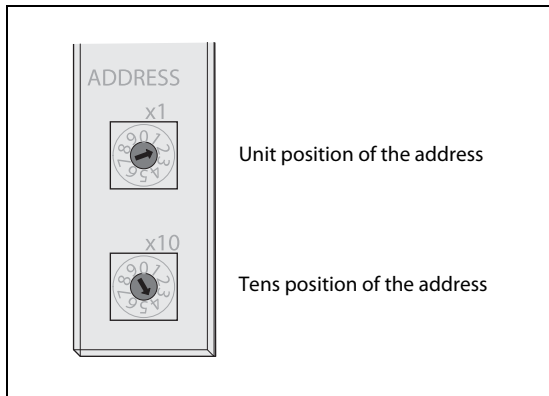
| LED | Color | Status                            | Description  |
|-----|-------|-----------------------------------|--|
| RUN | Green | ON                                | The head station is correctly initialized.*  |
| BF  | Red   | ON                                | The BF-LED indicates whether the communication functions via the Profibus.*  |
|     |       | OFF                               |  |
|     |       | Blinking                          |  |
| DIA | Red   | ON                                | The DIA-LED indicates an external diagnostics.*<br>The signaling is not supported by all devices or must be explicitly enabled for each channel.   |
|     |       | OFF                               |  |
| BUS | Red   | Blinking                          | The BUS-LED signals a projecting fault with the Profibus DP projecting of the station.*  |
|     |       | OFF                               |  |
| IO  | Green | ON                                | Data cycle on the internal bus   |
|     | Red   | ON                                | Hardware error of the head station   |
|     |       | Blinking                          | <ul style="list-style-type: none"> <li>When starting: internal bus is initialized</li> <li>During operation: general internal bus fault</li> </ul> |
|     |       | Blinking cyclically               | Fault message during internal bus reset and internal fault   |
|     | Amber | ON                                | Access to the head station firmware in the Flash-EEPROM  |
| —   | OFF   | No data cycle on the internal bus |  |
| A   | Green | ON                                | System supply is ok.   |
|     |       | OFF                               | System supply failed.  |
| B   | Green | ON                                | Field supply (power jumper contacts) is ok.  |
|     |       | OFF                               | Field supply failed.   |

**Tab. 2-1:** Description of the LEDs of the STL-PB1

\* The state of the Profibus communication is displayed by the four LEDs RUN, BF, DIA and BUS. Detailed fault messages are indicated with a blink code. Please refer to the manual of the STL-PB1 for a detailed description of these LEDs.

### 2.2.4 Setting the Station Address

The station address (decimal) is determined using two rotary switches on the STL-PB1.



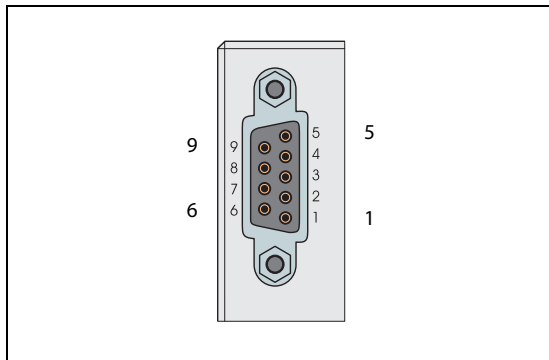
**Fig. 2-6:** Rotary switches of the STL-PB1

The switch “x1 ” determines the units position of the address, the switch “x10 ” determines the decimal positions of the address (for example “x1”: 2, “x10 ”: 4 -> address = 2 + 10 x 4 = 42).

Valid station addresses are between 1 and 99. The head station also permits the station address 0.

The station address is taken over by the head station after switching on the device (initialization phase). Adjustments of the switch have no effect during operation.

### 2.2.5 Pin Configuration of the Profibus DP Interface



**Fig. 2-7:** 9-pin D-SUB female connector for connection to Profibus DP

| Pin of the D-SUB connector | Signal    | Description               |
|----------------------------|-----------|---------------------------|
| 1                          | —         | Not used                  |
| 2                          | —         | Not used                  |
| 3                          | RXD/TXD-P | Receive/transmit data (+) |
| 4                          | RTS       | Ready to send             |
| 5                          | GND       | Supply ground (earth)     |
| 6                          | VP        | Voltage supply            |
| 7                          | —         | Not used                  |
| 8                          | RXD/TXD-N | Receive/transmit data (-) |
| 9                          | —         | Not used                  |

**Tab. 2-2:** Pin configuration of the Profibus DP interface of the STL-PB1

### 2.2.6 Wiring

Since RS 485 transmission technology is used, all devices are connected in a line structure. To connect the STL-PB1 to a Profibus DP network, use only the Profibus connector and shielded twisted pair Profibus cable complying with EN50170. Cable type A is strongly recommended.

| Parameter            | Specification          |
|----------------------|------------------------|
| Wave resistance      | 135 to 165 Ω           |
| Capacitance per unit | ≤ 30 pF/m              |
| Loop resistance      | ≤ 110 Ω/km             |
| Core diameter        | < 0.64 mm              |
| Core cross section   | < 0.34 mm <sup>2</sup> |

**Tab. 2-3:** Specifications for cable type A

The maximum line length for a bus segment depends on the transmission speed.

| Transmission speed                | Max. bus segment length |
|-----------------------------------|-------------------------|
| 9.6 / 19.2 / 45.45 / 93.75 kbit/s | 1200 m                  |
| 187.5 kbit/s                      | 1000 m                  |
| 500 kbit/s                        | 400 m                   |
| 1.5 Mbit/s                        | 200 m                   |
| 3 / 6 / 12 Mbit/s                 | 100 m                   |

**Tab. 2-4:** Max. bus segment length



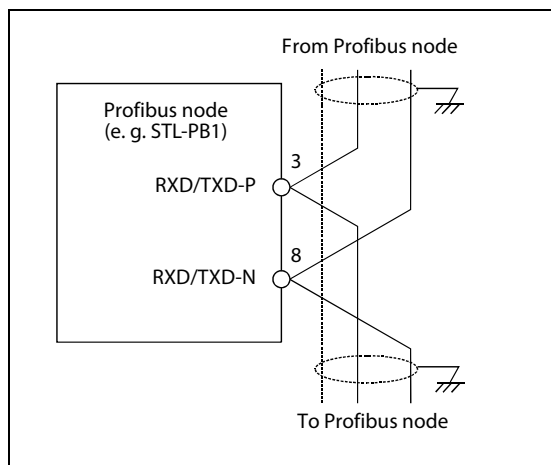
**CAUTION:**

**When the Profibus cable is laid, do not lay it close to main circuits or power lines.**

**They should be installed 100 mm (3.9 inch) or more from each other. Not doing so could result in noise that would cause malfunctioning.**

When connecting the nodes, ensure that the data cables are not mixed up. To achieve high interference resistance of the system against electromagnetic radiation, a shielded data cable (type A is shielded) should definitely be used. The shielding is to be connected to the protective ground on both sides ensuring good conductivity via large area shield clamps. Equipotential bonding of all connected field devices is also recommended.

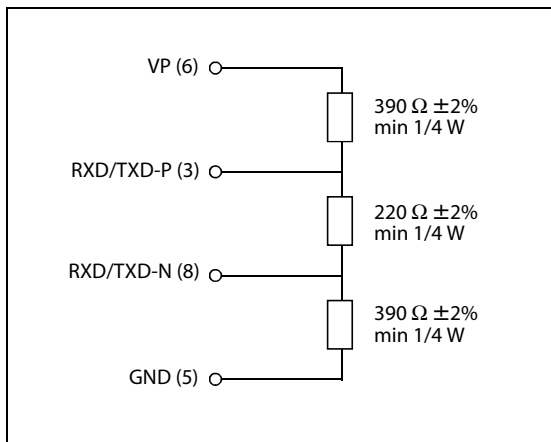
Stubs must absolutely be avoided with transmission rates greater than or equal to 1.5 MBit/s.



**Fig. 2-8:** Connection of the Profibus cable

### Bus Terminator

Each end of the Profibus DP network must be terminated with resistors. Since the STL-PB1 is not equipped with built-in terminating resistors, use a Profibus connector with a bus terminator if the STL-PB1 is situated at the beginning or end of a network.



**Fig. 2-9:** Termination of the Profibus

### 2.2.7 Local Process Image

After switching on, the head station STL-PB1 recognizes all connected STlite modules which supply data or wait for data (data width/bit width > 0). Analog and digital I/O modules can be mixed.

**NOTE**

For the number of input and output bits or bytes of the connected STlite modules please refer to the corresponding I/O module description in the appendix of this manual.

The head station produces an internal process image from the data width and the type of STlite module as well as the position of the STlite modules in the node. It is divided into an input and an output data area.

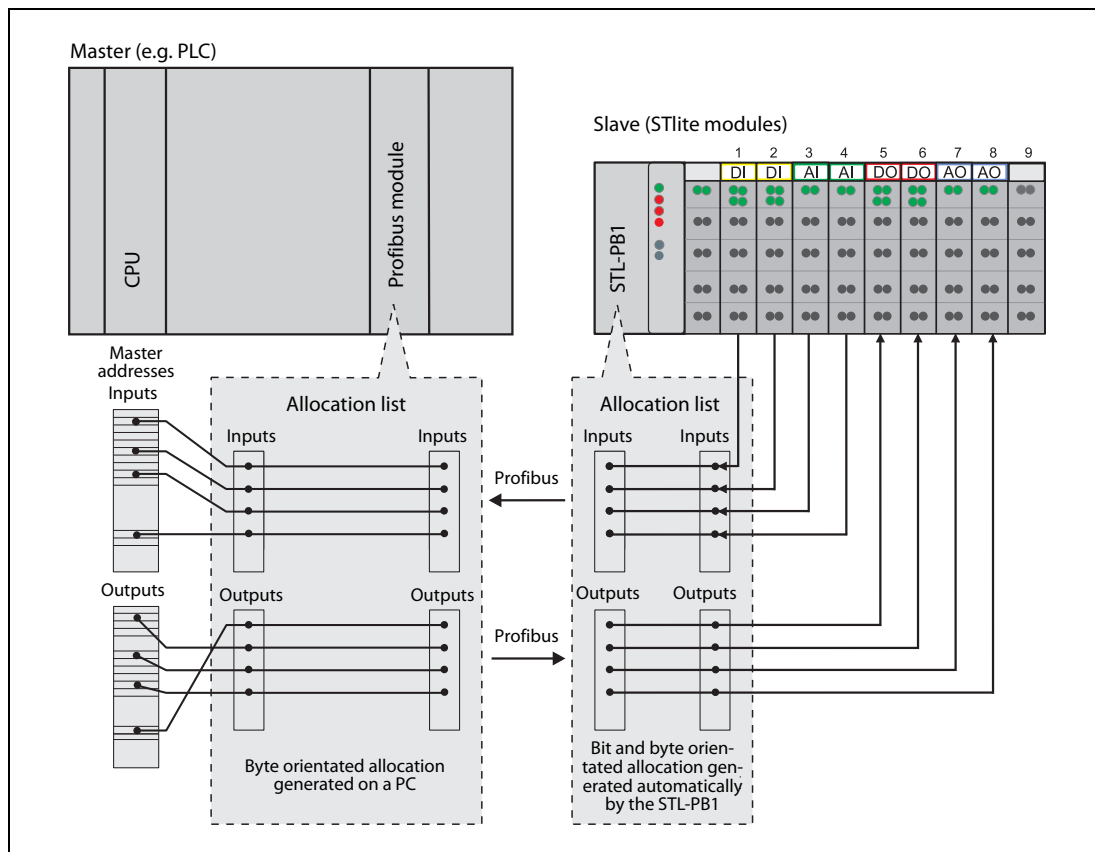
The data of the STlite modules is separated for the local input and output process image in the sequence of their position after the head station.

#### Allocation of the Input and Output Data

The process data is exchanged via the Profibus with the master.

- A maximum of 244 bytes of data is transmitted from the master to the node.
- The head station responds by returning a maximum of 244 bytes input data to the master.

Modules are configured according to their physical arrangement when projecting the node, which can be taken over from a hardware catalogue of the configuration programs. The information covering the possible modules is contained in the GSD files.



**Fig. 2-10:** Allocation of input and output data

**Process Data Structure for Profibus DP**

With some I/O modules, the structure of the process data is fieldbus specific. Depending on how the head station is parameterized, the status bytes (S), control bytes (C) and data bytes (D0...Dn) of the byte or word orientated modules are transmitted via Profibus in Motorola or Intel format.

**NOTE**

For the meaning of input and output bits or bytes of the connected STLite modules please refer to the corresponding I/O module description in the appendix of this manual.

● Digital I/O modules

| Type of module         | Name       | ID number | Description                                       | Process Image [Bit] |        |
|------------------------|------------|-----------|---|---------------------|--------|
|                        |            |           |   | Input               | Output |
| Digital input modules  | STL-DI8-V1 | 51205052  | 8 inputs for source type sensors, 24 V DC         | 8                   | 0      |
|                        | STL-DI8-V2 | 51205053  |   | 8                   | 0      |
| Digital output modules | STL-DO4    | 51205045  | 4 transistor outputs, 24 V DC, 0.5 A, source type | 0                   | 4      |
|                        | STL-DO8    | 51205043  | 8 transistor outputs, 24 V DC, 0.5 A, source type | 0                   | 8      |
|                        | STL-RO2    | 51205044  | 2 relay outputs 230 V AC / 30V DC, 500 VA/60 W    | 0                   | 2      |

**Tab. 2-5:** Profibus DP process data of digital input and output modules

● Two-channel analog input modules

| Type of module                    | Name      | ID number | Description                                | Register communication | Process Image [Byte] |        |
|-----------------------------------|-----------|-----------|--|------------------------|----------------------|--------|
|                                   |           |           |  |                        | Input                | Output |
| Analog input module (voltage)     | STL-AD2-V | 51205046  | 2 inputs 0 to 10 V                         | Yes                    | 6                    | 6      |
|                                   |           |           |  | No                     | 4                    | 0      |
| Analog input module (current)     | STL-AD2-I | 51205047  | 2 inputs 4 to 20 mA                        | Yes                    | 6                    | 6      |
|                                   |           |           |  | No                     | 4                    | 0      |
| Analog input module (temperature) | STL-TI2   | 51205048  | 2 inputs for Pt100 resistance thermometers | Yes                    | 6                    | 6      |
|                                   |           |           |  | No                     | 4                    | 0      |

**Tab. 2-6:** Profibus DP process data of two-channel analog input modules

| Register communication | Channel | Data type |        |       |        |
|------------------------|---------|-----------|--------|-------|--------|
|                        |         | MOTOROLA  |        | INTEL |        |
|                        |         | Input     | Output | Input | Output |
| Yes                    | 1       | S0        | C0     | S0    | C0     |
|                        |         | D1        | D1     | D0    | D0     |
|                        |         | D0        | D0     | D1    | D1     |
|                        | 2       | S1        | C1     | S1    | C1     |
|                        |         | D3        | D3     | D2    | D2     |
|                        |         | D2        | D2     | D3    | D3     |
| No                     | 1       | D1        | —      | D0    | —      |
|                        |         | D0        | —      | D1    | —      |
|                        | 2       | D3        | —      | D2    | —      |
|                        |         | D2        | —      | D3    | —      |

**Tab. 2-7:** Mapping for two-channel analog input modules



● Four-channel analog input modules

| Type of module                 | Name       | ID number | Description          | Register communication | Process Image [Byte] |        |
|--------------------------------|------------|-----------|----------------------|------------------------|----------------------|--------|
|                                |            |           |                      |                        | Input                | Output |
| Analog input modules (voltage) | STL-AD4-V1 | 51205049  | 4 inputs 0 to 10 V   | Yes                    | 12                   | 12     |
|                                |            |           |                      | No                     | 8                    | 0      |
|                                | STL-AD4-V2 | 51205050  | 4 inputs -10 to 10 V | Yes                    | 12                   | 12     |
|                                |            |           |                      | No                     | 8                    | 0      |
| Analog input module (current)  | STL-AD4-I  | 51205051  | 4 inputs 4 to 20 mA  | Yes                    | 12                   | 12     |
|                                |            |           |                      | No                     | 8                    | 0      |

**Tab. 2-8:** Profibus DP process data of four-channel analog input modules

| Register communication | Channel | Data type |        |       |        |
|------------------------|---------|-----------|--------|-------|--------|
|                        |         | MOTOROLA  |        | INTEL |        |
|                        |         | Input     | Output | Input | Output |
| Yes                    | 1       | S0        | C0     | S0    | C0     |
|                        |         | D1        | D1     | D0    | D0     |
|                        |         | D0        | D0     | D1    | D1     |
|                        | 2       | S1        | C1     | S1    | C1     |
|                        |         | D3        | D3     | D2    | D2     |
|                        |         | D2        | D2     | D3    | D3     |
|                        | 3       | S2        | C2     | S2    | C2     |
|                        |         | D5        | D5     | D4    | D4     |
|                        |         | D4        | D4     | D5    | D5     |
|                        | 4       | S3        | C3     | S3    | C3     |
|                        |         | D7        | D7     | D6    | D6     |
|                        |         | D6        | D6     | D7    | D7     |
| No                     | 1       | D1        | —      | D0    | —      |
|                        |         | D0        | —      | D1    | —      |
|                        | 2       | D3        | —      | D2    | —      |
|                        |         | D2        | —      | D3    | —      |
|                        | 3       | D5        | —      | D4    | —      |
|                        |         | D4        | —      | D5    | —      |
|                        | 4       | D7        | —      | D6    | —      |
|                        |         | D6        | —      | D7    | —      |

**Tab. 2-9:** Mapping for four-channel analog input modules

● Two-channel analog output modules

| Type of module                 | Name      | ID number | Description          | Register communication | Process Image [Byte] |        |
|--------------------------------|-----------|-----------|----------------------|------------------------|----------------------|--------|
|                                |           |           |                      |                        | Input                | Output |
| Analog output module (voltage) | STL-DA2-V | 51205042  | 2 outputs 0 to 10 V  | Yes                    | 6                    | 6      |
|                                |           |           |                      | No                     | 0                    | 4      |
| Analog output module (current) | STL-DA2-I | 51205041  | 2 outputs 4 to 20 mA | Yes                    | 6                    | 6      |
|                                |           |           |                      | No                     | 0                    | 4      |

**Tab. 2-10:** Profibus DP process data of two-channel analog output modules

| Register communication | Channel | Data type |        |       |        |
|------------------------|---------|-----------|--------|-------|--------|
|                        |         | MOTOROLA  |        | INTEL |        |
|                        |         | Input     | Output | Input | Output |
| Yes                    | 1       | S0        | C0     | S0    | C0     |
|                        |         | D1        | D1     | D0    | D0     |
|                        |         | D0        | D0     | D1    | D1     |
|                        | 2       | S1        | C1     | S1    | C1     |
|                        |         | D3        | D3     | D2    | D2     |
|                        |         | D2        | D2     | D3    | D3     |
| No                     | 1       | —         | D1     | —     | D0     |
|                        |         | —         | D0     | —     | D1     |
|                        | 2       | —         | D3     | —     | D2     |
|                        |         | —         | D2     | —     | D3     |

**Tab. 2-11:** Mapping for two-channel analog output modules

● Four-channel analog output modules

| Type of module                  | Name       | ID number | Description           | Register communication | Process Image [Byte] |        |
|---------------------------------|------------|-----------|-----------------------|------------------------|----------------------|--------|
|                                 |            |           |                       |                        | Input                | Output |
| Analog output modules (voltage) | STL-DA4-V1 | 51205038  | 4 outputs 0 to 10 V   | Yes                    | 12                   | 12     |
|                                 |            |           |                       | No                     | 0                    | 8      |
|                                 | STL-DA4-V2 | 51205039  | 4 outputs -10 to 10 V | Yes                    | 12                   | 12     |
|                                 |            |           |                       | No                     | 0                    | 8      |
| Analog output module (current)  | STL-DA4-I  | 51205040  | 4 outputs 4 to 20 mA  | Yes                    | 12                   | 12     |
|                                 |            |           |                       | No                     | 0                    | 8      |

**Tab. 2-12:** Profibus DP process data of four-channel analog output modules

| Register communication | Channel | Data type |        |       |        |
|------------------------|---------|-----------|--------|-------|--------|
|                        |         | MOTOROLA  |        | INTEL |        |
|                        |         | Input     | Output | Input | Output |
| Yes                    | 1       | S0        | C0     | S0    | C0     |
|                        |         | D1        | D1     | D0    | D0     |
|                        |         | D0        | D0     | D1    | D1     |
|                        | 2       | S1        | C1     | S1    | C1     |
|                        |         | D3        | D3     | D2    | D2     |
|                        |         | D2        | D2     | D3    | D3     |
|                        | 3       | S2        | C2     | S2    | C2     |
|                        |         | D5        | D5     | D4    | D4     |
|                        |         | D4        | D4     | D5    | D5     |
|                        | 4       | S3        | C3     | S3    | C3     |
|                        |         | D7        | D7     | D6    | D6     |
|                        |         | D6        | D6     | D7    | D7     |
| No                     | 1       | —         | D1     | —     | D0     |
|                        |         | —         | D0     | —     | D1     |
|                        | 2       | —         | D3     | —     | D2     |
|                        |         | —         | D2     | —     | D3     |
|                        | 3       | —         | D5     | —     | D4     |
|                        |         | —         | D4     | —     | D5     |
|                        | 4       | —         | D7     | —     | D6     |
|                        |         | —         | D6     | —     | D7     |

**Tab. 2-13:** Mapping for four-channel analog output modules

● Encoder module STL-ENC

| Type of module | Name    | ID number | Description                          | Register communication | Process Image [Byte] |        |
|----------------|---------|-----------|--------------------------------------|------------------------|----------------------|--------|
|                |         |           |                                      |                        | Input                | Output |
| Encoder module | STL-ENC | 51205116  | Input module for incremental encoder | Yes                    | 6                    | 6      |
|                |         |           |                                      | No (not possible)      | —                    | —      |

**Tab. 2-14:** Profibus DP process data of the encoder module

| Register communication | Channel | Data type |        |       |        |
|------------------------|---------|-----------|--------|-------|--------|
|                        |         | MOTOROLA  |        | INTEL |        |
|                        |         | Input     | Output | Input | Output |
| Yes                    | 1       | S0        | C0     | S0    | C0     |
|                        |         | D1        | D1     | D0    | D0     |
|                        |         | D0        | D0     | D1    | D1     |
|                        |         | S1        | C1     | S1    | C1     |
|                        |         | D3        | D3     | D2    | D2     |
|                        |         | D2        | D2     | D3    | D3     |

**Tab. 2-15:** Mapping for encoder module STL-ENC

● Counter module STL-C100

| Type of module | Name     | ID number | Description                                     | Register communication | Process Image [Byte] |        |
|----------------|----------|-----------|---|------------------------|----------------------|--------|
|                |          |           |   |                        | Input                | Output |
| Counter module | STL-C100 | 51244881  | Forward/reverse counter, max. frequency 100 kHz | Yes                    | 6                    | 6      |
|                |          |           |   | No (not possible)      | —                    | —      |

**Tab. 2-16:** Profibus DP process data of the counter module

| Register communication | Channel | Data type |        |       |        |
|------------------------|---------|-----------|--------|-------|--------|
|                        |         | MOTOROLA  |        | INTEL |        |
|                        |         | Input     | Output | Input | Output |
| Yes                    | 1       | S         | C      | S     | C      |
|                        |         | —         | —      | —     | —      |
|                        |         | D3        | D3     | D0    | D0     |
|                        |         | D2        | D2     | D1    | D1     |
|                        |         | D1        | D1     | D2    | D2     |
|                        |         | D0        | D0     | D3    | D3     |

**Tab. 2-17:** Mapping for counter module STL-C100

● SSI interface module

| Type of module   | Name    | ID number | Description                  | Register communication | Process Image [Byte] |        |
|------------------|---------|-----------|------------------------------|------------------------|----------------------|--------|
|                  |         |           |                              |                        | Input                | Output |
| Interface module | STL-SSI | 51205057  | Input module for SSI encoder | Yes                    | 6                    | 6      |
|                  |         |           |                              | No                     | 4                    | 0      |

**Tab. 2-18:** Profibus DP process data of the interface module STL-SSI

| Register communication                       | Channel | Data type |        |       |        |
|--|---------|-----------|--------|-------|--------|
|  |         | MOTOROLA  |        | INTEL |        |
|  |         | Input     | Output | Input | Output |
| Yes<br>(Alternative format, factory setting) | 1       | S0        | C0     | S0    | C0     |
|  |         | D1        | D1     | D0    | D0     |
|  |         | D0        | D0     | D1    | D1     |
|  |         | —         | —      | —     | —      |
|  |         | D3        | D3     | D2    | D2     |
|  |         | D2        | D2     | D3    | D3     |
| Yes<br>(Standard format)                     | 1       | S0        | C0     | S0    | C0     |
|  |         | —         | —      | —     | —      |
|  |         | D3        | D3     | D0    | D0     |
|  |         | D2        | D2     | D1    | D1     |
|  |         | D1        | D1     | D2    | D2     |
| No   | 1       | D0        | D0     | D3    | D3     |
|  |         | D3        | —      | D0    | —      |
|  |         | D2        | —      | D1    | —      |
|  |         | D1        | —      | D2    | —      |
|  |         | D0        | —      | D3    | —      |

**Tab. 2-19:** Mapping for interface module STL-SSI

## 2.2.8 Configuration

### Configuration of the I/O Modules

The configuration of the node is performed in accordance with the physical requirements of the head station and I/O modules.

The head station or the process data channel is to be configured on the first slot. The other slots are configured in accordance with the physical requirements of the I/O modules. Here only I/O modules with process data are relevant. The supply modules, bus internal system supply module and the bus end module are to be ignored for the configuration because they do not provide any process data.

One or two modules are entered in the hardware catalogue for each I/O module.

The module appear as "name/ID number/type/specifications", for example:  
STL-DO4/51205045/4DO/24V/0.5 A.

In the hardware catalogue of GX Configurator-DP you will find the entries \*STL-DO4 and \*STL-RO2. When using these denominations the head station adds the binary information of the current module in a byte which was previously opened with a STL-DO4 respectively a STL-RO2. The use of "\*" is only permitted when the number of outputs is less than or equal to the remaining bits in the previously opened byte. The binary I/O modules combined in a byte can be arranged at separate locations, i.e. binary I/O modules with a different signal type or also byte orientated I/O modules can be connected between.

In order to be able to individually arrange the scope of connected periphery units independent of the control program, it is possible to parameterize I/O modules in the configuration table as "not plugged". In this manner process data still present is filtered for the individual module and not transferred on the Profibus DP to and read by the periphery units.

### GSD Files

Under Profibus DP the features of the modules are defined by the manufacturers in the form of a GSD file (General Station Description).

Structure, content and coding of this unit main data are standardized and made available to the user allowing to project optional DP slaves using the project units of various manufacturers.

The GSD file is read by the configuration software and the corresponding settings are transmitted. For the necessary inputs and handling steps please refer to user manual of the FX Configurator DP or GX Configurator DP.

The GSD files for the STlite series can be downloaded from the following web-site:

- <http://www.mitsubishi-automation.com>  
Menu "MyMitsubishi" → (Login) → "Downloads" → "GSD files"

## 2.3 Configuration Example for MELSEC System Q

For this example, a Profibus DP slave consisting of the following STLite modules is used:

- Head station STL-PB1
- Digital input module STL-DI8-V1 (8 inputs)
- Digital output module STL-DO4 (4 outputs)
- Analog output module STL-DA4-V1 (4 channels, 0 to 10 V)
- Analog input module STL-AD2-V (2 channels, 0 to 10 V)
- End module STL-ET

### NOTES

For the specifications of the modules and the installation procedures please refer to the installation manual of the STLite series.

STLite modules with power contacts (male contacts) cannot be linked to modules with fewer power contacts. In this case install a power supply module between the two relevant modules.

### 2.3.1 Settings for the Slave Station

For this example, the station address of the STL-PB1 is set to "1" (switch x1 = 1, switch x10 = 0, please refer to section 2.2.4).

### 2.3.2 Configuring the Profibus DP

Start the Profibus configuration tool GX Configurator-DP. In the **Project** menu, click on **New**. Select the MELSEC System Q and the corresponding Profibus DP master module.

Don't modify the default settings at the next screens. Leave also the device addresses unchanged ("D1000" for input data and "D2000" for output data).

Select **Consistency** for the data transfer and **Data transfer only** as shown in the following figure.

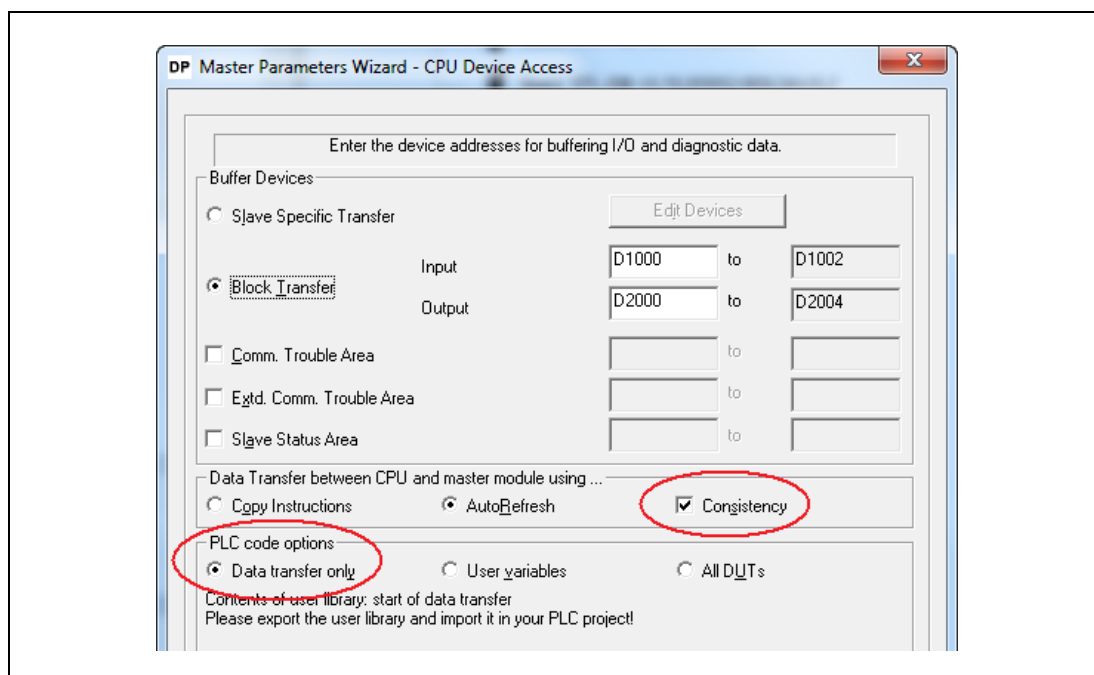
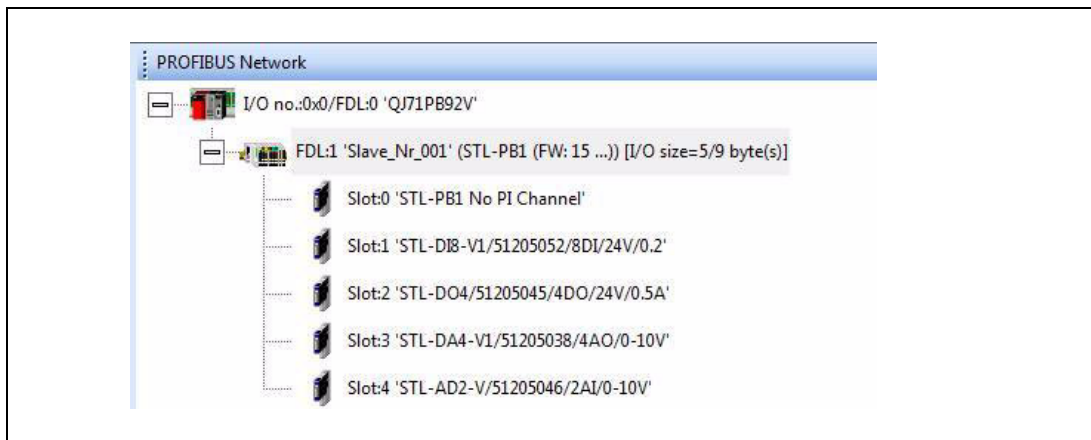


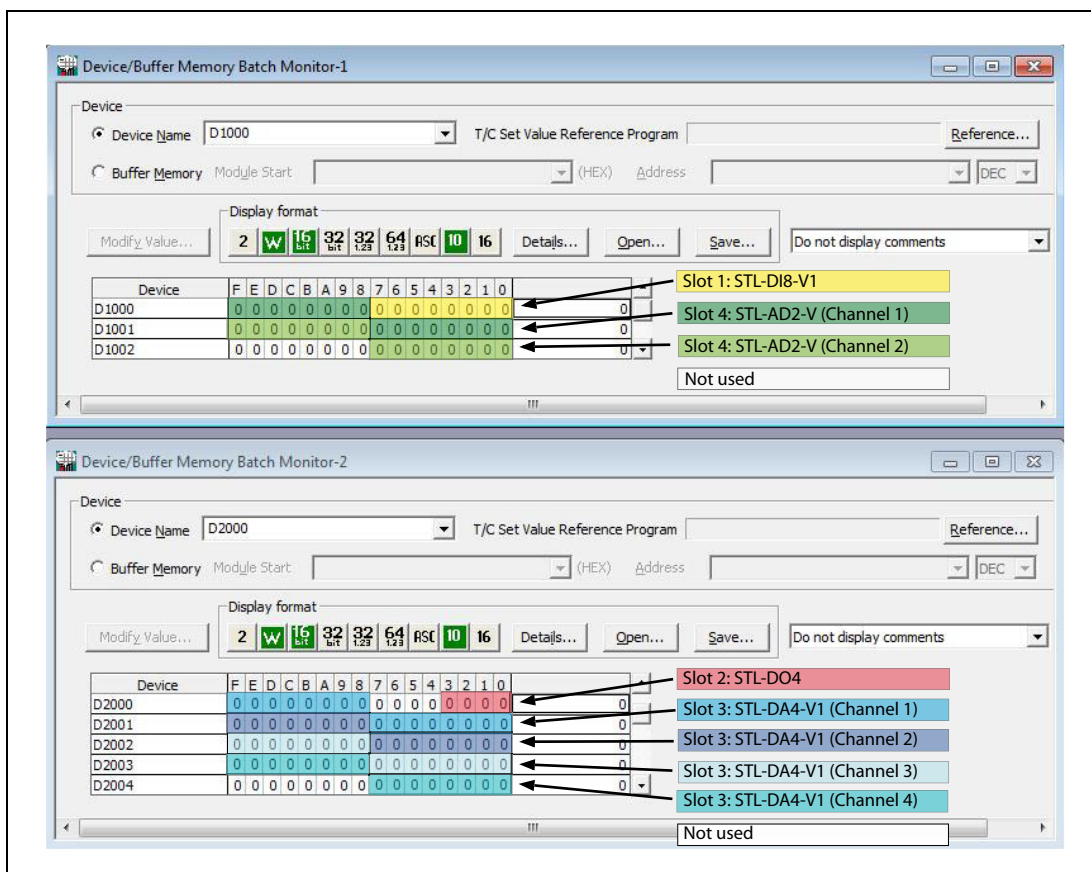
Fig. 2-11: Settings for input and output data

Next, add the GSD files for the MELSEC STlite series to your project (**Import Task -> Add GSD files**). Configure a slave station with the STL-PB1 and the STlite I/O modules in the order listed above. Again, leave all default settings unchanged.



**Fig. 2-12:** Slave configuration

After wiring the Profibus DP network, downloading the configuration to the PLC and starting the Profibus DP communication (set Y0 of the master module QJ71PB92V to "1"), you can monitor the data transfer in the Device Monitor of GX Works2.



**Fig. 2-13:** Allocation of the input and output data for this example

As can be seen in the above picture, the input respectively output data of one analog module channel is spread across two data registers. This is very unfavourable for the programming. The reason for this is the single byte occupied by each of the digital I/O modules.

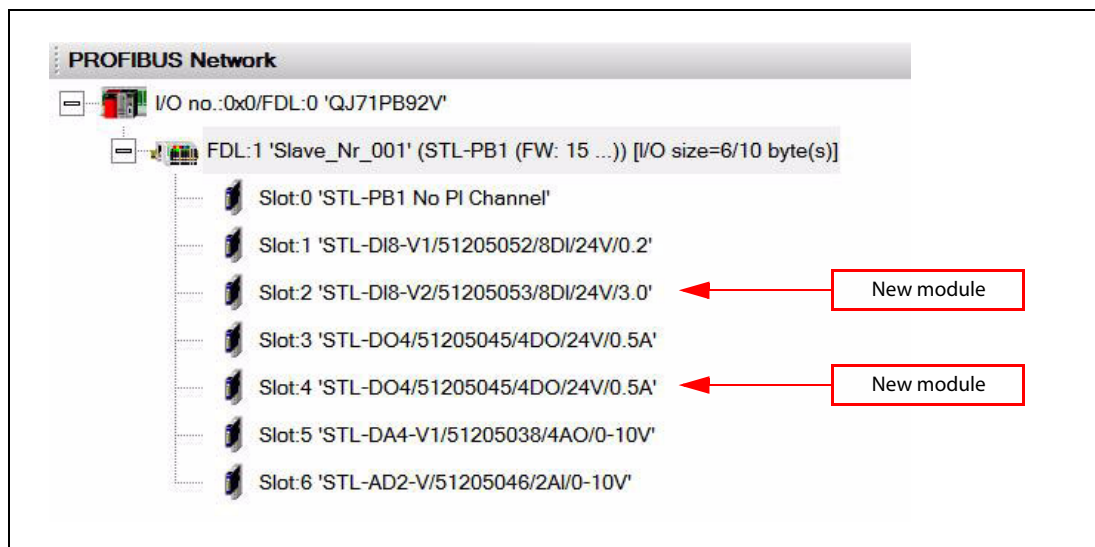


### Optimising the configuration

The input and output data of the analog modules can be shifted by adding one additional digital module for each data direction.

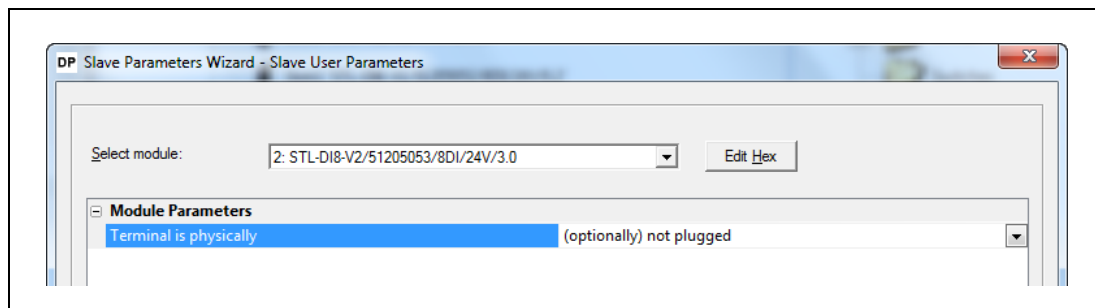
But you don't have to buy two modules just to simplify the programming – these two modules are only virtual!

Insert a digital input module with 8 inputs on slot 2 and another digital output module on slot 4.

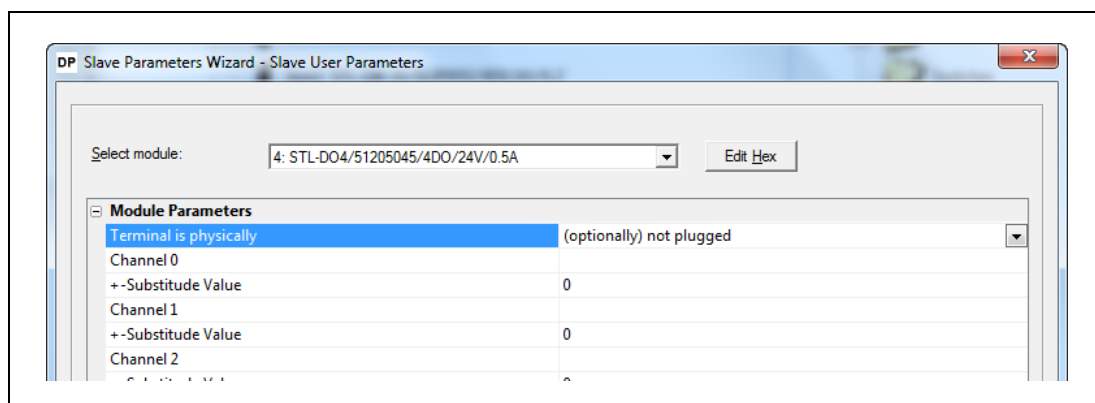


**Fig. 2-14:** New configuration with two dummy modules

When a module is added to the configuration, the module parameters can be set. Select "... not plugged" for both modules.



**Fig. 2-15:** The new digital input module on slot 2 is "physically not plugged".



**Fig. 2-16:** The additional digital output module on slot 4 is also "not plugged".

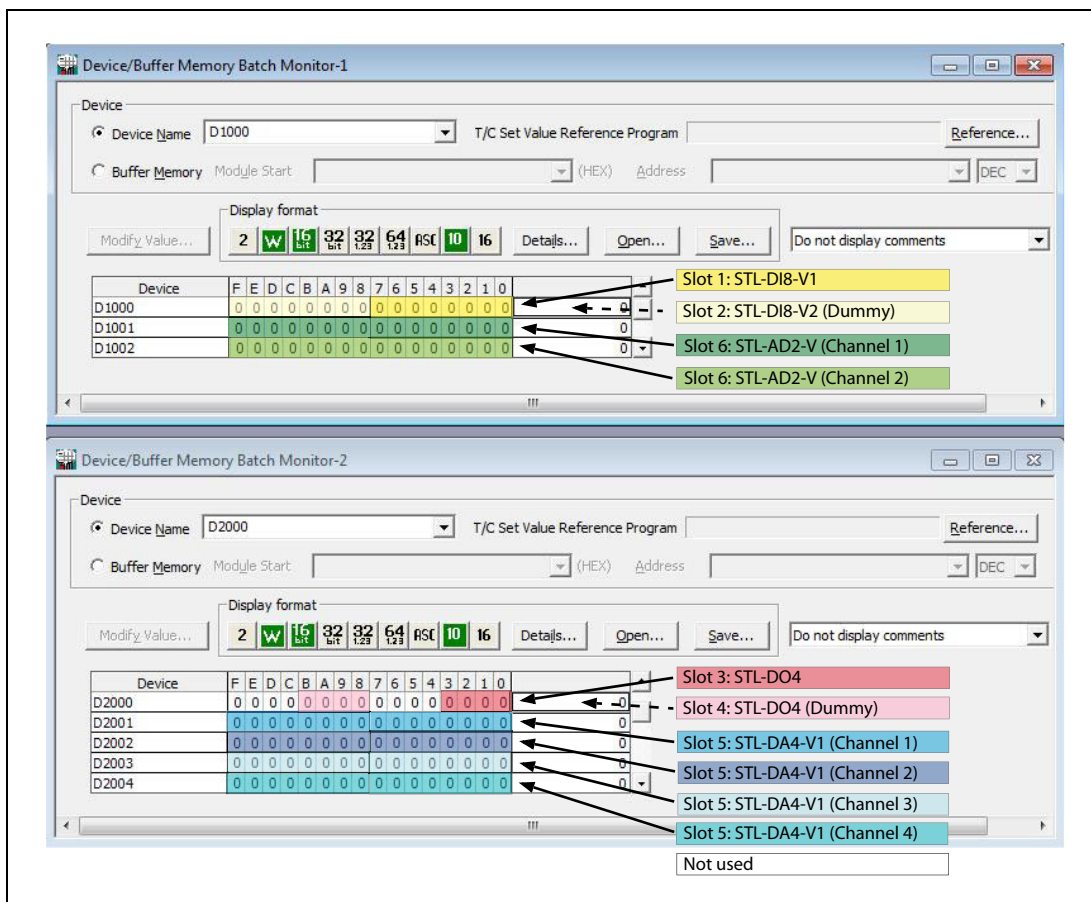


Fig. 2-17: Optimised allocation of the input and output data

For the process images of the individual STLite modules please refer to the appendix, section A.1. For example, reading a value of 16384 (4000H) from D1001 means that a voltage of 5.00 V is applied to channel 1 of the STL-AD2-V or, if you want to output 10 V on channel 1 of the STL-DA4-V1, write 32760 (7FF8H) to D2001.

**Rearrangement of the Modules**

Another option for this example to allocate 16 bit input and output data to a single data register is to mount first the analog modules and afterwards the digital modules.

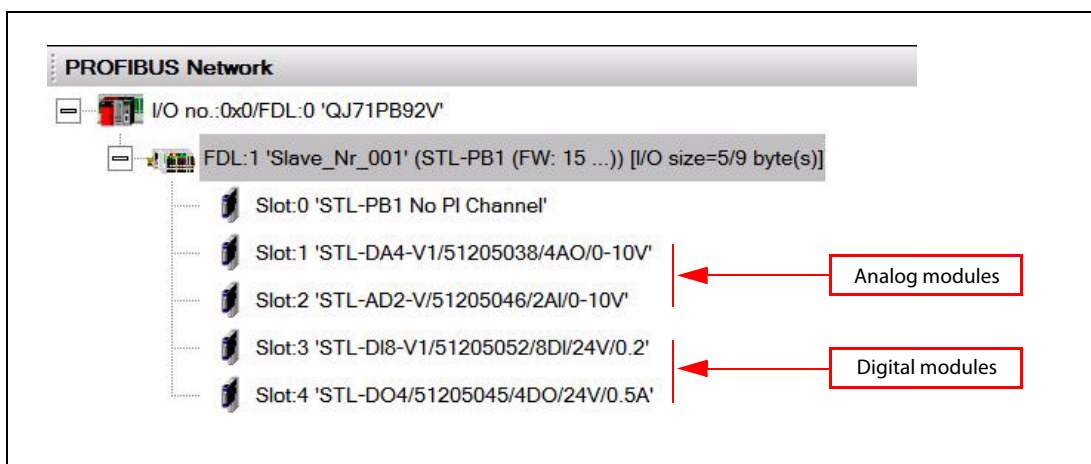


Fig. 2-18: Configuration with analog modules mounted first

The device monitor for this configuration is shown on the next page.



Fig. 2-19: Device monitor for the configuration with the analog modules mounted first

### 2.3.3 Saving devices

A digital output module with less than eight outputs (STL-DO4 or STL-RO2) will occupy a whole byte although only two or four bits are used. (See allocation for the digital output module STL-DO4 in the above figure.)

When, for example, another STL-DO4 is used in the configuration, this module can be entered as \*STL-DO4. The four bits belonging to this module will be entered in the same byte as the data for the previous STL-DO4. Since the byte is now complete, any other STL-DO4 has to be entered as STL-DO4.

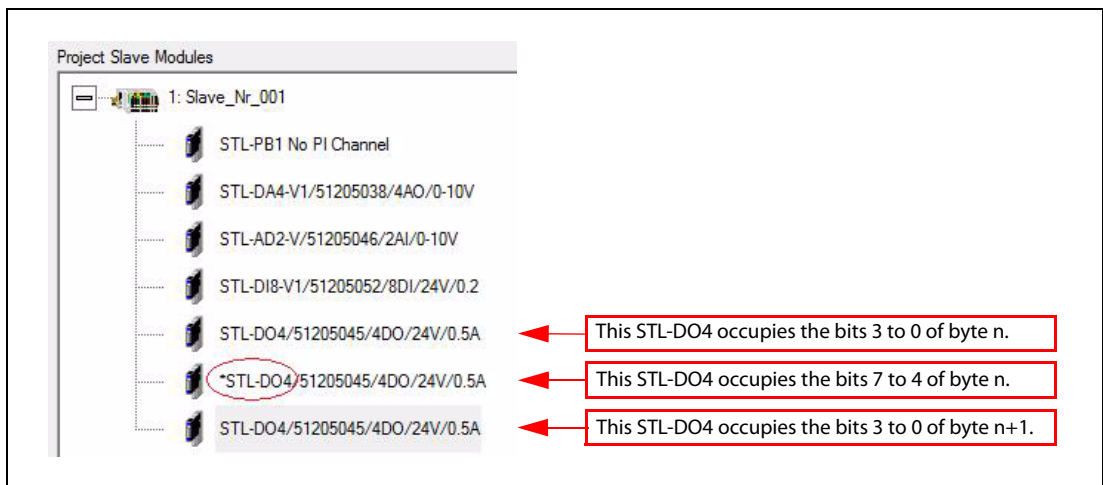


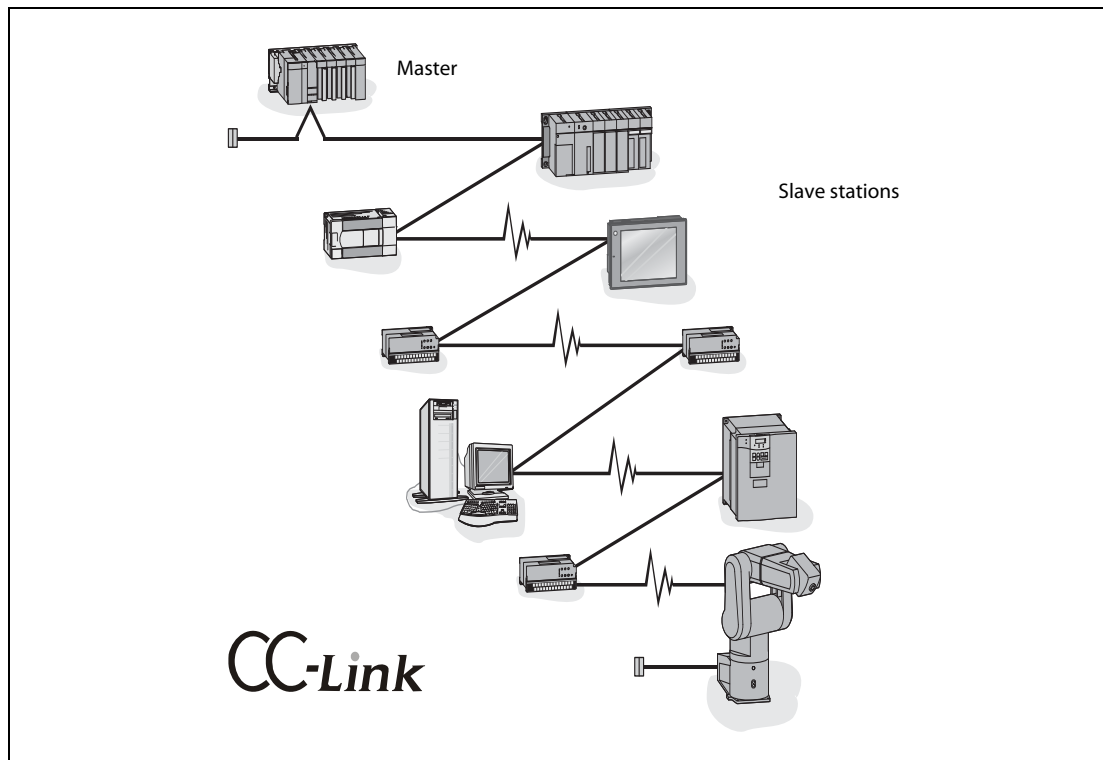
Fig. 2-20: The amount of used devices is reduced when the denomination "\*" is used.



## 3 CC-Link

### 3.1 Overview

The open fieldbus and control network CC-Link (Control & Communication Link) provides fast data communications with different devices. As with all manufacturer specific networks, CC-Link is quickly implemented and is guaranteed to work. CC-Link is also an open network and therefore allows many third-party products now appearing on the market with CC-Link connectivity.



**Fig. 3-1:** Typical CC-Link configuration

#### Structure

A CC-Link system consists of a master and up to 64 slave stations.

- **Master:** The master has the control information (parameters) and controls the entire network. One Master station is required in each network. The station number is fixed to 0.
- **Slave:** The CC-Link slaves are the link to the field side. They edit the input data of the peripheral equipment for the communication with the master and output the master data to the peripheral equipment.
- **Station:** A station is a device that is connected via the CC-Link. Station numbers from 1 to 64 can be assigned.
- **Remote device station:** A station that can use bit data and word data (Example: Digital and analog I/O modules).
- **Remote I/O station:** A station that can only use bit data (Example: Digital I/O modules)

Transmission speeds from 156 kbit/s to 10 Mbit/s can be used. The maximum transmission distance is limited from 100 to 1200 m, depending on the bit rate used.

#### Cable types

The data communications requires standardized shielded twisted-pair cable with 3 wires.

## 3.2 Head Station STL-BT1 (CC-Link)

The head station STL-BT1 is used in a remote station or a remote I/O station on CC-Link. It displays the peripheral data of all connected STlite modules to the CC-Link.



**Fig. 3-2:** Head station STL-BT1 for CC-Link (with connected digital input module)

The head station determines the physical structure of the node and automatically creates a local process image from this with all inputs and outputs. This could involve a mixed arrangement of analog (word by word data exchange) and digital (byte by byte data exchange) modules.

The data of the analog modules are mapped into the process image according to the order of their position downstream of the head station.

The bits of the digital modules are compiled to form bytes and also mapped into the process image attached to the data of the analog modules. Should the number of digital I/Os exceed 8 bits, the head station automatically starts another byte.

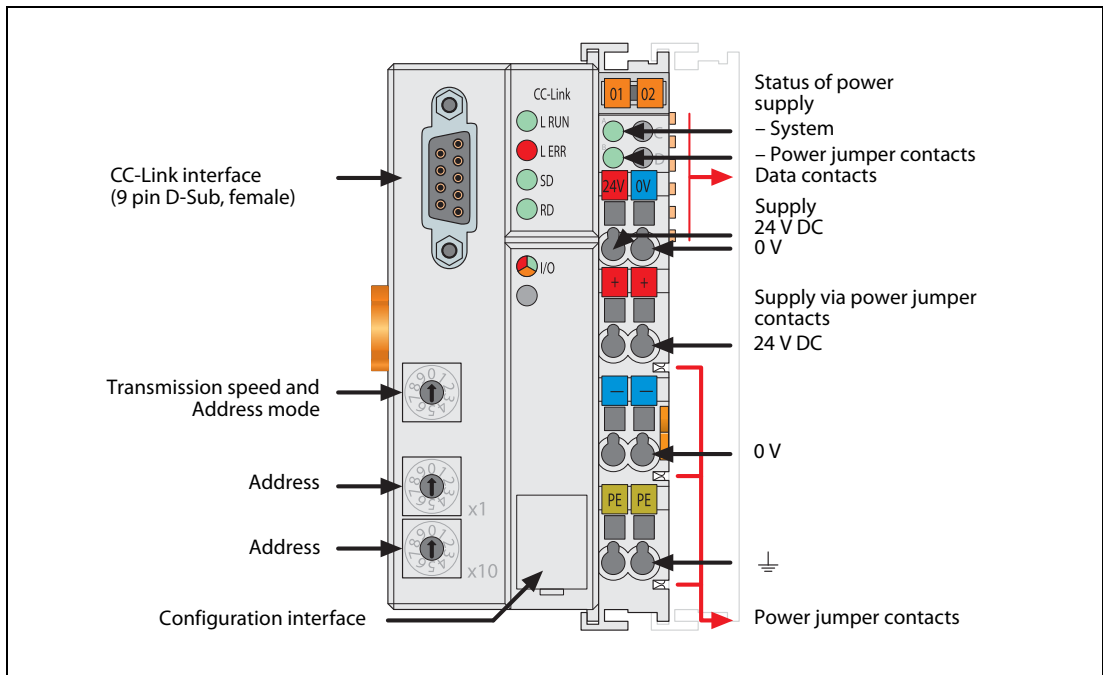
The process image is subdivided into an input and output data area. The process data can be read in via CC-Link and further processed in a control system. The process output data is sent via CC-Link.

The STL-BT1 can occupy up to four stations.

### NOTE

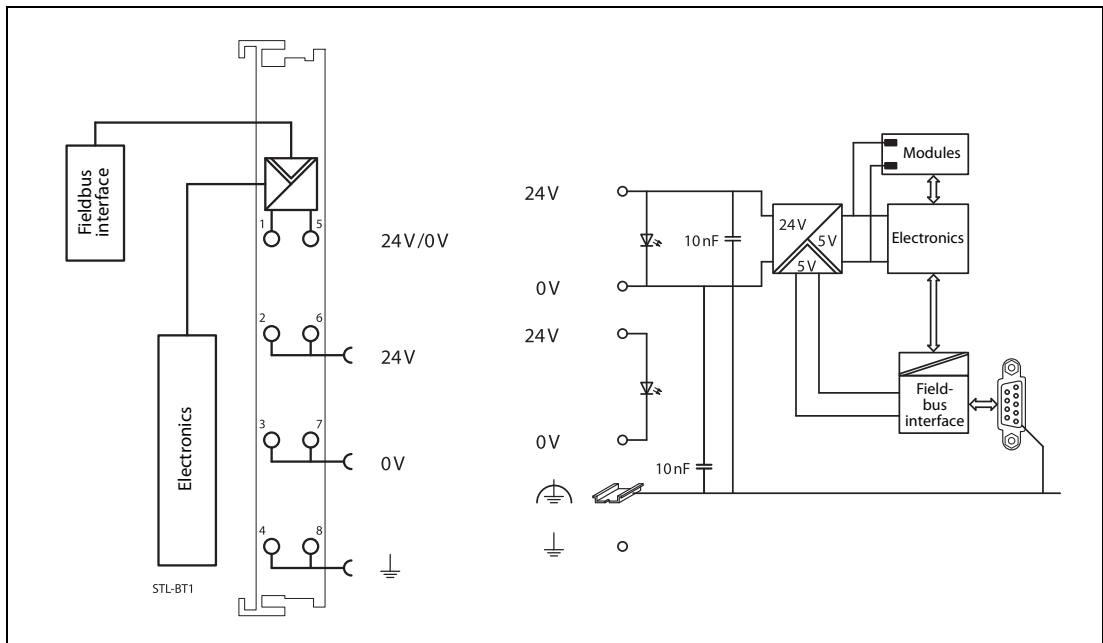
For the specifications of the head station STL-BT1 please refer to the installation manual of the STlite series.

**3.2.1 View**



**Fig. 3-3:** Head station STL-BT1 (CC-Link)

**3.2.2 Device Supply**



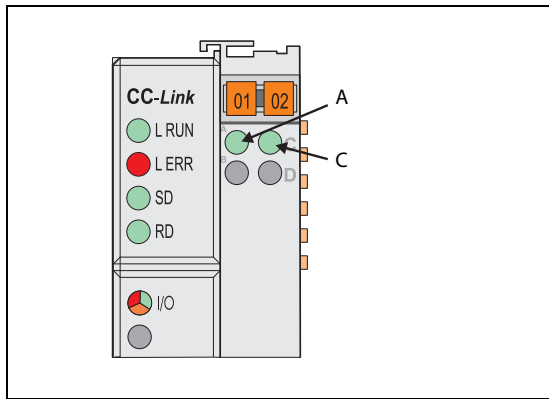
**Fig. 3-4:** Block diagram for the head station STL-BT1 (CC-Link)

The device supply is intended both for the system and the field units. Two external supply voltages are required:

- 24 V DC for the head station
- 24 V DC for the connected STlite modules (forwarded via the power jumper contacts)

The fieldbus interface is supplied with electrically isolated voltage from the internal system supply module.

### 3.2.3 Display Elements



**Fig. 3-5:** The operating condition of the head station is signalled via LEDs.

| LED   | Color | Status     | Description   |
|-------|-------|------------|---|
| L.RUN | Green | ON         | Data link is being executed.*   |
| L.ERR | Red   | ON         | Communication error (host).*  |
|       |       | Flickering | Switch type setting was changed while power was ON.*                                  |
| SD    | Green | ON         | Data is being transmitted.*   |
| RD    | Green | ON         | Data is being received.*  |
| IO    | Green | ON         | Node operation*   |
|       |       | Blinking   | Waiting for initial data*   |
|       | Red   | Blinking   | <ul style="list-style-type: none"> <li>Start up</li> <li>Faults occurring*</li> </ul> |
| A     | Green | ON         | System supply is ok.  |
|       |       | OFF        | System supply failed.   |
| B     | Green | ON         | Field supply (power jumper contacts) is ok.   |
|       |       | OFF        | Field supply failed.  |

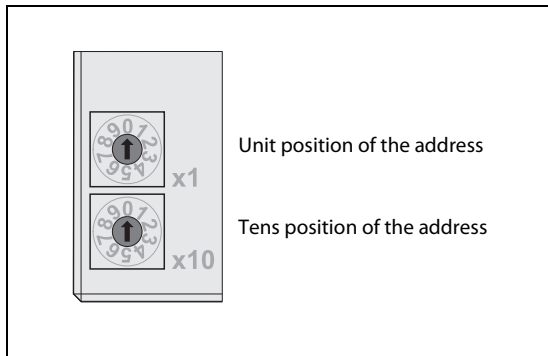
**Tab. 3-1:** Description of the LEDs of the STL-BT1

\* The state of the CC-Link communication is displayed by the four LEDs L.RUN, L.ERR, SD and RD. Detailed fault messages are indicated with a blink code of the IO LED. Please refer to the manual of the STL-BT1 for a detailed description of these LEDs.



### 3.2.4 Setting the Station Address

The station address (decimal) is determined using two rotary switches on the STL-BT1.



**Fig. 3-6:** Rotary switches of the STL-BT1

The switch "x1" determines the units position of the address, the switch "x10" determines the decimal positions of the address (for example "x1": 2, "x10": 3 -> address = 2 + 10 x 3 = 32).

A valid CC-Link station address can be set within the range from 1 to 64.

The setting is only read during the power up sequence. Changing the switch position during operation does not change the configuration of the head station. Turn off and on the power supply for the head station to accept the changing.

Rules for CC-Link station numbers:

- Set station number in sequence .
- The station numbers can be set regardless of the order in which stations are connected.
- Do not duplicate station numbers.
- Specify unoccupied station numbers as reserved stations.

### 3.2.5 Setting the Transmission Speed and Address Mode

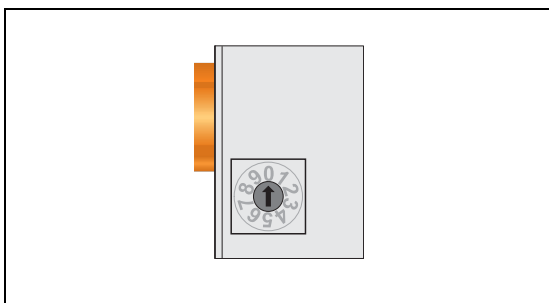
The STL-BT1 supports five different transmission speeds and two address modes (fixed address mode and auto address mode).

In **auto address mode** the head station determines the number of addresses (numbers of occupied stations) according to the connected STLite modules (one to four addresses per head station).

In **fixed address mode** the head station sets the number of occupied stations to four irrespective to the connected STLite modules.

**NOTE**

Number of units and number of stations:  
 The number of units is the number of devices that are physically connected to a single CC-Link.  
 The number of stations is the total number of occupied stations among all slave stations that are connected via the CC-Link. One unit can occupy up to four station numbers.

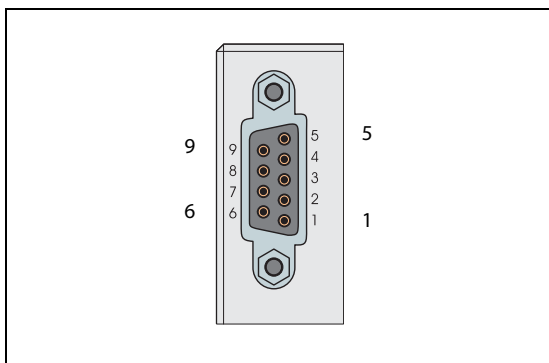


**Fig. 3-7:** Transmission speed and address mode selector switch of the STL-BT1

| Transmission speed | Position of the selector switch                     |   |
|--------------------|---|---|
|                    | Fixed address mode<br>(STL-BT1 occupies 4 stations) | Auto address mode<br>(STL-BT1 occupies 1 to 4 stations) |
| 156 kbit/s         | 0   | 5   |
| 625 kbit/s         | 1   | 6   |
| 2.5 Mbit/s         | 2   | 7   |
| 5 Mbit/s           | 3   | 8   |
| 10 Mbit/s          | 4   | 9   |

**Tab. 3-2:** Selection of transmission speed and address mode

### 3.2.6 Pin Configuration of the CC-Link Interface



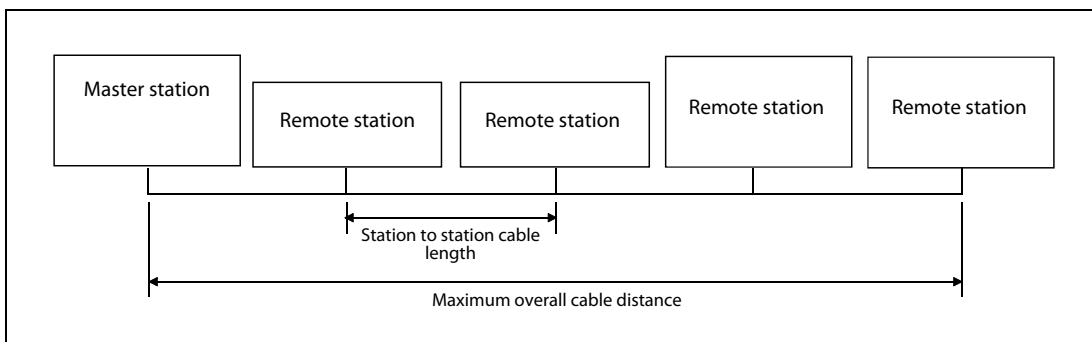
**Fig. 3-8:** 9-pin D-SUB female connector for connection to CC-Link

| Pin of the D-SUB connector | Signal | Description |
|----------------------------|--------|-------------|
| 1                          | —      | Not used    |
| 2                          | —      |             |
| 3                          | DA     | Data A      |
| 4                          | DG     | Data ground |
| 5                          | —      | Not used    |
| 6                          | —      |             |
| 7                          | —      |             |
| 8                          | DB     | Data B      |
| 9                          | —      | Not used    |
| Housing                    | SLD    | Shield      |

**Tab. 3-3:** Pin configuration of the CC-Link interface of the STL-BT1

### 3.2.7 Wiring

#### Maximum overall cable distance



**Fig. 3-9:** Definition of cable length

| Transmission speed | Station to station cable length | Maximum overall cable distance |
|--------------------|---------------------------------|--------------------------------|
| 156 kbit/s         | ≥ 20 cm                         | 1200 m                         |
| 625 kbit/s         |                                 | 900 m                          |
| 2.5 Mbit/s         |                                 | 400 m                          |
| 5 Mbit/s           |                                 | 160 m                          |
| 10 Mbit/s          |                                 | 100 m                          |

**Tab. 3-4:** The maximum overall cable distance depends on the transmission speed

**CC-Link Dedicated Cable**

Use the CC-Link dedicated cable for the CC-Link system. If a cable other than the CC-Link dedicated cable is used, the performance of the CC-Link system cannot be guaranteed.

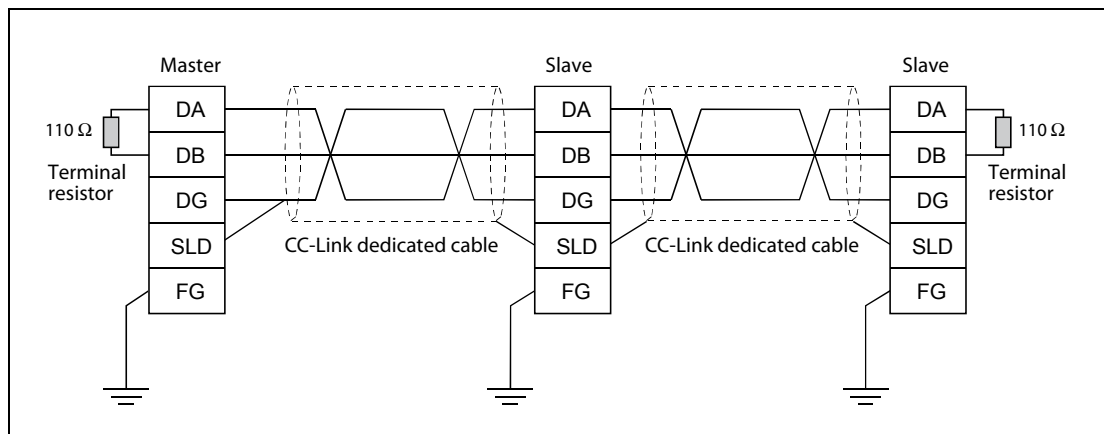
If you have any questions regarding the CC-Link dedicated cable or CC-Link in general, visit the CC-Link Partner Association homepage <http://www.cclink.org/>.

**NOTE**

For details, refer to the CC-Link cable wiring manual issued by CC-Link Partner Association

**Connection to CC-Link**


- The master module can be situated anywhere in the network.
- Star connection is not allowed.
- Make a daisy chain without drops.
- Each end of a CC-Link network must be terminated with a resistor.
- Use the fieldbus connector STL-CCLink con for connection to the D-SUB connector of the head station STL-BT1 (see next page).



**Fig. 3-10:** Wiring of a CC-Link network

**NOTE**

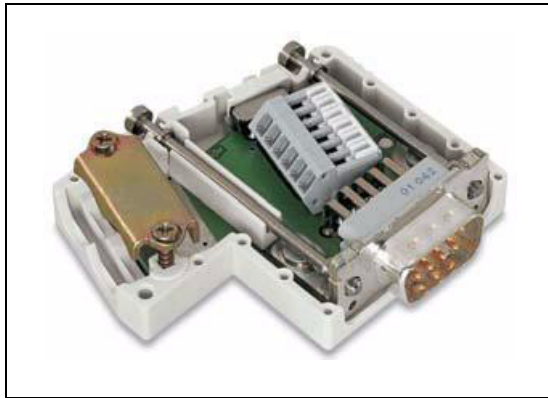
Connect the shielded wire of the CC-Link dedicated cable to "SLD" of each device, and ground both ends of the shielded wire.



**CAUTION:**  
**When the CC-Link cable is laid, do not lay it close to main circuits or power lines. They should be installed 100 mm (3.9 inch) or more from each other. Not doing so could result in noise that would cause malfunctioning.**

**CC-Link Fieldbus Connector**

The fieldbus connector STL-CCLink con connects a CC-Link device to a CC-Link line.

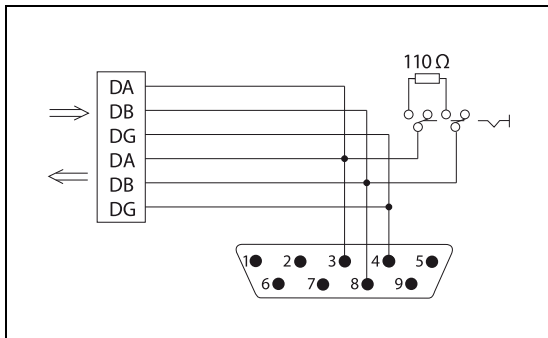


**Fig. 3-11:** Connector STL-CCLink con

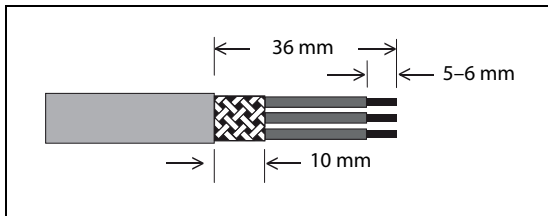
The fieldbus connector has the following features:

- Two horizontal cable entries (One input and one output).
- Fast and maintenance-free CAGE CLAMP® connection, can be held in the open position with the help of an actuation slide mechanism.
- Externally operable switch to activate or deactivate the terminating resistor.

For the first and last station on the bus, the switch must be set to "ON" (terminating resistor activated). Set the switch to "OFF" for the intermediate stations on the bus (terminating resistor deactivated).



**Fig. 3-12:** Internal wiring of the connector STL-CCLink con



**Fig. 3-13:** Required preparation of the CC-Link cable for connection to the connector STL-CCLink con

### 3.2.8 Local Process Image

After switching on, the head station STL-BT1 recognizes all connected STlite modules which supply data or wait for data (data width/bit width > 0). Analog and digital I/O modules can be mixed.

The head station produces an internal process image from the data width and the type of STlite module as well as the position of the STlite modules in the node. It is divided into an input and an output data area.

The data of the digital STlite modules are bit orientated, i.e. the data exchange is made bit for bit. The analog and special function STlite modules are all byte orientated modules, i.e. modules where the data exchange is made byte for byte.

#### NOTE

For the number of input and output bits or bytes of the connected STlite modules please refer to the corresponding I/O module description in the appendix of this manual.

The data of the STlite I/O modules are separated for the local input and output process image in the sequence of their position after the head station in the individual process image.

In the respective I/O area, first of all analog modules are mapped, then all digital modules, even if the order of the connected analog and digital modules does not comply with this order. The bits of the digital modules are grouped, each of these groups having a data width of 1 byte. Should the number of digital I/Os exceed 8 bits, the head station automatically starts another byte.

#### NOTE

A process image restructuring may result if a node is changed or extended. In this case the process data addresses also change in comparison with earlier ones. In the event of adding a module, take the process data of all previous modules into account.

#### Address Area per Station

The areas shown in the following table are allocated for the remote I/O (RX/RY: bit devices) and remote registers (RWw/RWr: word devices) by the master station, depending on the number of occupied stations.

#### NOTE

Sixteen points of the remote I/O are reserved for the system.

| Type of data                   |                  | Number of occupied stations |           |           |            |
|--------------------------------|------------------|-----------------------------|-----------|-----------|------------|
|                                |                  | 1                           | 2         | 3         | 4          |
| Remote input: RX <sup>①</sup>  | Total            | 32 points                   | 64 points | 96 points | 128 points |
|                                | User area        | 16 points                   | 48 points | 80 points | 112 points |
| Remote output: RY <sup>②</sup> | Total            | 32 points                   | 64 points | 96 points | 128 points |
|                                | User area        | 16 points                   | 48 points | 80 points | 112 points |
| Remote registers               | RWr <sup>③</sup> | 4 points                    | 8 points  | 12 points | 16 points  |
|                                | RWw <sup>④</sup> | 4 points                    | 8 points  | 12 points | 16 points  |

**Tab. 3-5:** The size of the address area depends on the number of occupied stations

① RX: Inputs from digital input modules

② RY: Outputs to digital output modules

③ RWr: Input data from analog modules or special function modules (e. g. counter)

④ RWw: Output data to analog modules or special function modules

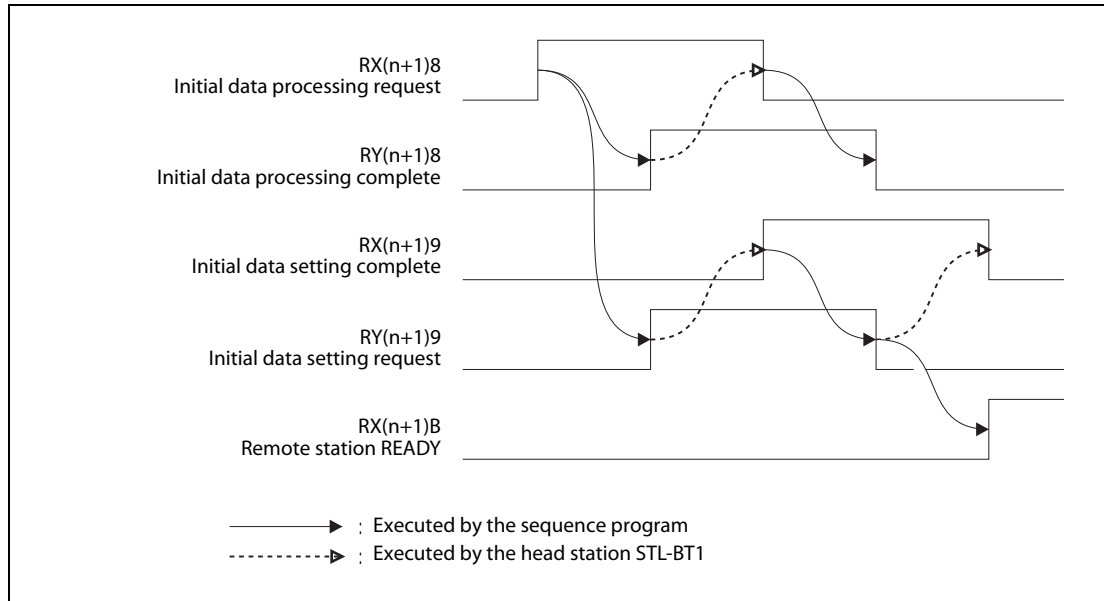
The position of the remote I/O system area is shown in the following table.

| RX / RY  | Number of occupied stations |                |                |           |
|----------|-----------------------------|----------------|----------------|-----------|
|          | 1                           | 2              | 3              | 4         |
| 00 to 0F | User area                   | User area      | User area      | User area |
| 10 to 1F | System area                 |                |                |           |
| 20 to 2F | Cannot be used              | System area    | System area    | User area |
| 30 to 3F |                             | Cannot be used |                |           |
| 40 to 4F |                             | Cannot be used | System area    |           |
| 50 to 5F |                             |                | Cannot be used |           |
| 60 to 6F |                             |                | Cannot be used |           |
| 70 to 7F |                             |                | System area    |           |

**Tab. 3-6:** *User areas and system areas*

**Initial Data Transfer**

After power-on or hardware reset, the head station STL-BT1 requests its initial data (i.e. the system bits for fault behaviour) from the master station as described below.



**Fig. 3-14:** Timing diagram of the system flags

| Remote device |          | Signal name                      | Description   |
|---------------|----------|----------------------------------|---|
| Input         | Output   |                                  |   |
| RX(n+1)8      |          | Initial data processing request  | After the power is turned on or after the hardware reset, the initial data processing request flag is turned on by the head station STL-BT1 in order to request the initial data setting. It is turned off when the initial data processing complete flag RY(n+1)8 is turned on.                          |
|               | RY(n+1)8 | Initial data processing complete | After the power is turned on or after the hardware reset, the initial data processing complete processing is executed by the initial data processing request, and this flag is turned on after the processing is completed.   |
| RX(n+1)9      |          | Initial data setting complete    | When there is an initial data setting request (i.e. RY(n+1)9 is turned on), this flag is turned on by the initial data setting completion. When the initial data setting request flag is turned off after the initial data setting completion, the initial data setting complete flag is also turned off. |
|               | RY(n+1)9 | Initial data setting request     | This flag is turned on to set or modify the initial data.   |
| RX(n+1)A      |          | Error status                     | This flag is turned on when an error occurs in the head station STL-BT1.  |
| RX(n+1)B      |          | Remote station READY             | This is turned on when the initial data setting is complete and the head station STL-BT1 is in the READY status, after the power is turned on or after the hardware reset. It is turned off during the test mode. (This is used to interlock the read and write from the master module.)                  |

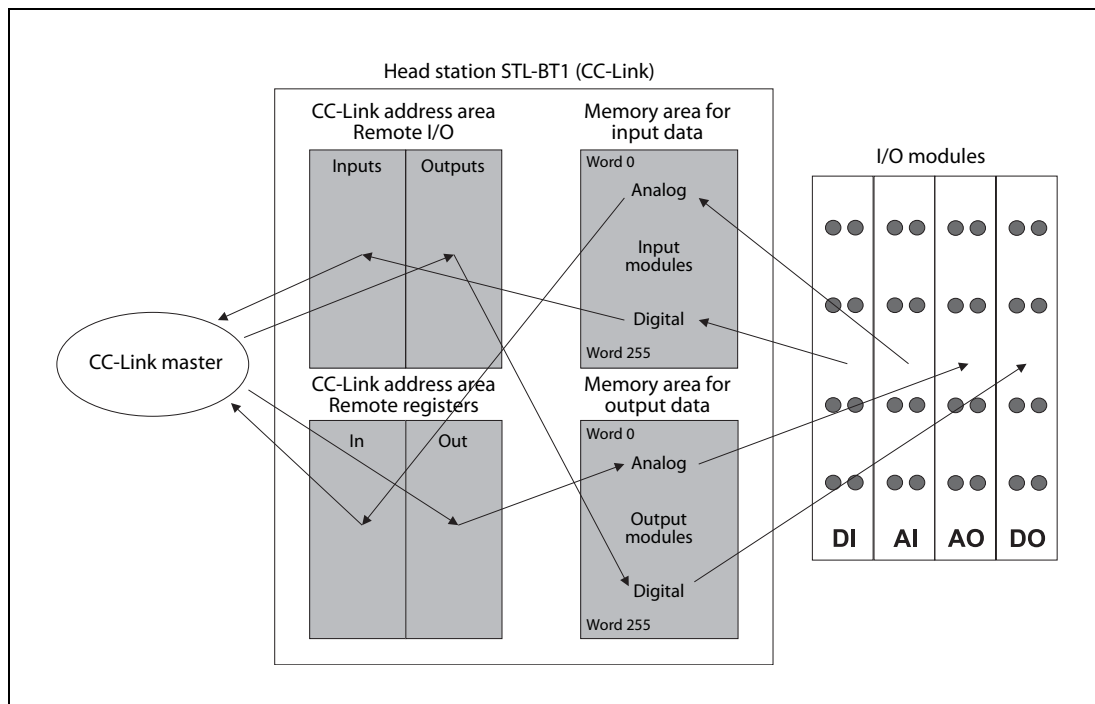
**Tab. 3-7:** Remote devices for initialization



### Data Exchange

After mapping the I/O-data of the STlite I/O modules to the local process image the head station cyclically transfers the digital input data from the process image to the Remote I/O area and the analog input data to the Remote Register area.

In the same way the digital output data from the Remote I/O area and the analog output data from the Remote Register area to the are transferred to the process image.



**Fig. 3-15:** Data exchange for CC-Link

**Allocation of the Input and Output Data**

**NOTE**

For the meaning of input and output bits or bytes of the connected STLite modules please refer to the corresponding I/O module description in the appendix of this manual.

The index k in the following tables points to the next free Remote input/output or Remote register (read/write).

- Digital I/O modules

| Type of module        | Name       | ID number | Description                               | Process Image [Bit] |        |
|-----------------------|------------|-----------|---|---------------------|--------|
|                       |            |           |   | Input               | Output |
| Digital input modules | STL-DI8-V1 | 51205052  | 8 inputs for source type sensors, 24 V DC | 8                   | 0      |
|                       | STL-DI8-V2 | 51205053  |   | 8                   | 0      |

**Tab. 3-8:** Process data of digital input modules

| Remote input | Signal name | Remote output | Signal name |
|--------------|-------------|---------------|-------------|
| RXn(k)       | X0          |               |             |
| RXn(k+1)     | X1          |               |             |
| RXn(k+2)     | X2          |               |             |
| RXn(k+3)     | X3          |               |             |
| RXn(k+4)     | X4          |               |             |
| RXn(k+5)     | X5          |               |             |
| RXn(k+6)     | X6          |               |             |
| RXn(k+7)     | X7          |               |             |

**Tab. 3-9:** Allocation of data for the digital input modules STL-DI8-V1 and STL-DI8-V2

| Type of module         | Name    | ID number | Description                                       | Process Image [Bit] |        |
|------------------------|---------|-----------|---|---------------------|--------|
|                        |         |           |   | Input               | Output |
| Digital output modules | STL-DO4 | 51205045  | 4 transistor outputs, 24 V DC, 0.5 A, source type | 0                   | 4      |
|                        | STL-DO8 | 51205043  | 8 transistor outputs, 24 V DC, 0.5 A, source type | 0                   | 8      |
|                        | STL-RO2 | 51205044  | 2 relay outputs 230 V AC / 30V DC, 500 VA/60 W    | 0                   | 2      |

**Tab. 3-10:** Process data of digital output modules

| Remote input | Signal name | Remote output | Signal name |
|--------------|-------------|---------------|-------------|
|              |             | RYn(k)        | Y0          |
|              |             | RYn(k+1)      | Y1          |
|              |             | RYn(k+2)      | Y2          |
|              |             | RYn(k+3)      | Y3          |

**Tab. 3-11:** Allocation of data for the digital output module STL-DO4

| Remote input | Signal name | Remote output | Signal name |
|--------------|-------------|---------------|-------------|
|              |             | RYn(k)        | Y0          |
|              |             | RYn(k+1)      | Y1          |
|              |             | RYn(k+2)      | Y2          |
|              |             | RYn(k+3)      | Y3          |
|              |             | RYn(k+4)      | Y4          |
|              |             | RYn(k+5)      | Y5          |
|              |             | RYn(k+6)      | Y6          |
|              |             | RYn(k+7)      | Y7          |

**Tab. 3-12:** Allocation of data for the digital output module STL-DO8

| Remote input | Signal name | Remote output | Signal name |
|--------------|-------------|---------------|-------------|
|              |             | RYn(k)        | Y0          |
|              |             | RYn(k+1)      | Y1          |

**Tab. 3-13:** Allocation of data for the relay output module STL-RO2

● Two-channel analog input modules

| Type of module       |             | Name      | ID number | Description                                | Process Image [Byte] |        |
|----------------------|-------------|-----------|-----------|--|----------------------|--------|
|                      |             |           |           |  | Input                | Output |
| Analog input modules | Voltage     | STL-AD2-V | 51205046  | 2 inputs 0 to 10 V                         | 4                    | 0      |
|                      | Current     | STL-AD2-I | 51205047  | 2 inputs 4 to 20 mA                        |                      |        |
|                      | Temperature | STL-TI2   | 51205048  | 2 inputs for Pt100 resistance thermometers |                      |        |

**Tab. 3-14:** Process data of two-channel analog input modules

| Remote register | Signal name  | High byte | Low byte | Remote register | Signal name | High byte | Low byte |
|-----------------|--------------|-----------|----------|-----------------|-------------|-----------|----------|
| RWrn(k)         | AI Channel 1 | D1        | D0       |                 |             |           |          |
| RWrn(k+1)       | AI Channel 2 | D3        | D2       |                 |             |           |          |

**Tab. 3-15:** Allocation of data for two-channel analog input modules

● Four-channel analog input modules

| Type of module       |         | Name       | ID number | Description          | Process Image [Byte] |        |
|----------------------|---------|------------|-----------|----------------------|----------------------|--------|
|                      |         |            |           |                      | Input                | Output |
| Analog input modules | Voltage | STL-AD4-V1 | 51205049  | 4 inputs 0 to 10 V   | 8                    | 0      |
|                      |         | STL-AD4-V2 | 51205050  | 4 inputs -10 to 10 V |                      |        |
|                      | Current | STL-AD4-I  | 51205051  | 4 inputs 4 to 20 mA  |                      |        |

**Tab. 3-16:** Process data of four-channel analog input modules

| Remote register | Signal name  | High byte | Low byte | Remote register | Signal name | High byte | Low byte |
|-----------------|--------------|-----------|----------|-----------------|-------------|-----------|----------|
| RWrn(k)         | AI Channel 1 | D1        | D0       |                 |             |           |          |
| RWrn(k+1)       | AI Channel 2 | D3        | D2       |                 |             |           |          |
| RWrn(k+2)       | AI Channel 3 | D5        | D4       |                 |             |           |          |
| RWrn(k+3)       | AI Channel 4 | D7        | D6       |                 |             |           |          |

**Tab. 3-17:** Allocation of data for four-channel analog input modules

● Two-channel analog output modules

| Type of module        |         | Name      | ID number | Description          | Process Image [Byte] |        |
|-----------------------|---------|-----------|-----------|----------------------|----------------------|--------|
|                       |         |           |           |                      | Input                | Output |
| Analog output modules | Voltage | STL-DA2-V | 51205042  | 2 outputs 0 to 10 V  | 0                    | 4      |
|                       | Current | STL-DA2-I | 51205041  | 2 outputs 4 to 20 mA |                      |        |

**Tab. 3-18:** Process data of two-channel analog output modules

| Remote register | Signal name | High byte | Low byte | Remote register | Signal name  | High byte | Low byte |
|-----------------|-------------|-----------|----------|-----------------|--------------|-----------|----------|
|                 |             |           |          | RWwn(k)         | AO Channel 1 | D1        | D0       |
|                 |             |           |          | RWwn(k+1)       | AO Channel 2 | D3        | D2       |

**Tab. 3-19:** Allocation of data for two-channel analog output modules

● Four-channel analog output modules

| Type of module        |         | Name       | ID number | Description           | Process Image [Byte] |        |
|-----------------------|---------|------------|-----------|-----------------------|----------------------|--------|
|                       |         |            |           |                       | Input                | Output |
| Analog output modules | Voltage | STL-DA4-V1 | 51205038  | 4 outputs 0 to 10 V   | 0                    | 8      |
|                       |         | STL-DA4-V2 | 51205039  | 4 outputs -10 to 10 V |                      |        |
|                       | Current | STL-DA4-I  | 51205040  | 4 outputs 4 to 20 mA  |                      |        |

**Tab. 3-20:** Process data of four-channel analog output modules

| Remote register | Signal name | High byte | Low byte | Remote register | Signal name  | High byte | Low byte |
|-----------------|-------------|-----------|----------|-----------------|--------------|-----------|----------|
|                 |             |           |          | RWwn(k)         | AO Channel 1 | D1        | D0       |
|                 |             |           |          | RWwn(k+1)       | AO Channel 2 | D3        | D2       |
|                 |             |           |          | RWwn(k+2)       | AO Channel 3 | D5        | D4       |
|                 |             |           |          | RWwn(k+3)       | AO Channel 4 | D7        | D6       |

**Tab. 3-21:** Allocation of data for four-channel analog output modules

● Encoder module STL-ENC

| Type of module | Name    | ID number | Description                          | Process Image [Byte] |        |
|----------------|---------|-----------|--------------------------------------|----------------------|--------|
|                |         |           |                                      | Input                | Output |
| Encoder module | STL-ENC | 51205116  | Input module for incremental encoder | 6                    | 6      |

**Tab. 3-22:** Process data of the encoder module

| Remote register | Signal name                  | High byte | Low byte | Remote register | Signal name                | High byte | Low byte |
|-----------------|------------------------------|-----------|----------|-----------------|----------------------------|-----------|----------|
| RWrn(k)         | Process data/<br>Status byte | D0        | S0       | RWwn(k)         | Set value/<br>Control byte | D0        | C0       |
| RWrn(k+1)       | Status byte/<br>Process data | S1        | D1       | RWwn(k+1)       | Control byte/<br>Set value | C1        | D1       |
| RWrn(k+2)       | Process data                 | D3        | D2       | RWwn(k+2)       | Set value                  | D3        | D2       |

**Tab. 3-23:** Allocation of data for the encoder module STL-ENC

● Counter module STL-C100

| Type of module | Name     | ID number | Description                                     | Process Image [Byte] |        |
|----------------|----------|-----------|---|----------------------|--------|
|                |          |           |   | Input                | Output |
| Counter module | STL-C100 | 51244881  | Forward/reverse counter, max. frequency 100 kHz | 6                    | 6      |

**Tab. 3-24:** Process data of the counter module

| Remote register | Signal name   | High byte | Low byte | Remote register | Signal name  | High byte | Low byte |
|-----------------|---------------|-----------|----------|-----------------|--------------|-----------|----------|
| RWrn(k)         | Status byte   | 0         | S        | RWwn(k)         | Control byte | 0         | C        |
| RWrn(k+1)       | Counter value | D1        | D0       | RWwn(k+1)       | Set value    | D1        | D0       |
| RWrn(k+2)       | Counter value | D3        | D2       | RWwn(k+2)       | Set value    | D3        | D2       |

**Tab. 3-25:** Allocation of data for the counter module STL-C100

● SSI interface module

| Type of module   | Name    | ID number | Description                  | Process Image [Byte] |        |
|------------------|---------|-----------|------------------------------|----------------------|--------|
|                  |         |           |                              | Input                | Output |
| Interface module | STL-SSI | 51205057  | Input module for SSI encoder | 4                    | 0      |

**Tab. 3-26:** Process data of the interface module STL-SSI

| Remote register | Signal name  | High byte | Low byte | Remote register | Signal name | High byte | Low byte |
|-----------------|--------------|-----------|----------|-----------------|-------------|-----------|----------|
| RWrn(k)         | Process data | D1        | D0       |                 |             |           |          |
| RWrn(k+1)       | Process data | D3        | D2       |                 |             |           |          |

**Tab. 3-27:** Allocation of data for the interface module STL-SSI

### 3.3 Configuration Example for MELSEC System Q

For this example, a CC-Link slave consisting of the following STLite modules is used:

- Head station STL-BT1
- Digital input module STL-DI8-V1 (8 inputs)
- Digital output module STL-DO4 (4 outputs)
- Analog output module STL-DA4-V1 (4 channels, 0 to 10 V)
- Analog input module STL-AD2-V (2 channels, 0 to 10 V)
- End module STL-ET

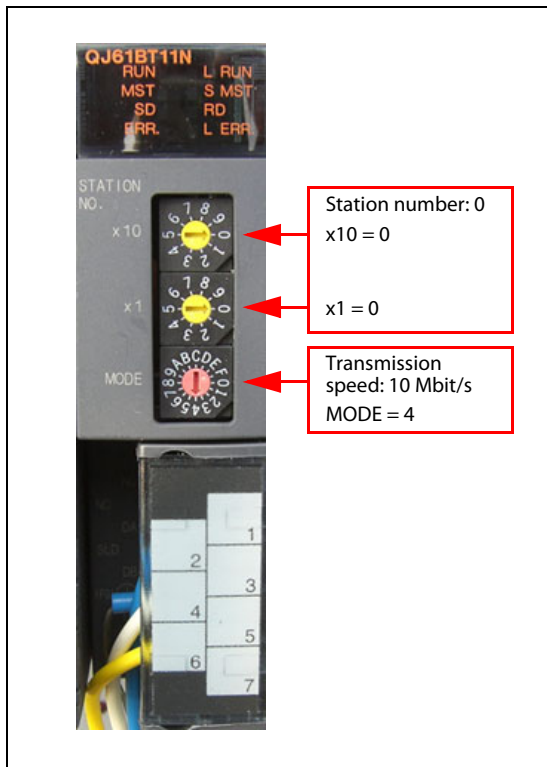
**NOTE**

For the specifications of the modules and the installation procedures please refer to the installation manual of the STLite series.

STLite modules with power contacts (male contacts) cannot be linked to bus modules with fewer power contacts. In this case install a power supply module between the two relevant modules.

#### 3.3.1 Settings for the Master Station

In this example, a QJ61BT11N is used as master station for the CC-Link. The station number is set to "0" and the mode switch to "4" for a transmission speed of 10 Mbit/s.



**Fig. 3-16:** Station number and transmission speed selector switches of the QJ61BT11N

### 3.3.2 Settings for the Slave Station

#### Station Address

For this example, the station address of the STL-BT1 is set to "1" (switch x1 = 1, switch x10 = 0, please refer to section 3.2.4).

#### Transmission Speed and Address Mode

The transmission speed and address mode selector switch of the STL-BT1 is set to "9". This will result in a transmission speed of 10 Mbit/s and auto address mode (see section 3.2.5). The auto address mode is needed since the slave station is later set to occupy 1 station.

### 3.3.3 Configuring the CC-Link Network

Start GX Works2. In the project navigator window, open the **Parameter**, double click on **Network parameter** and then on **CC-Link**.

Enter the following parameters for the master station.

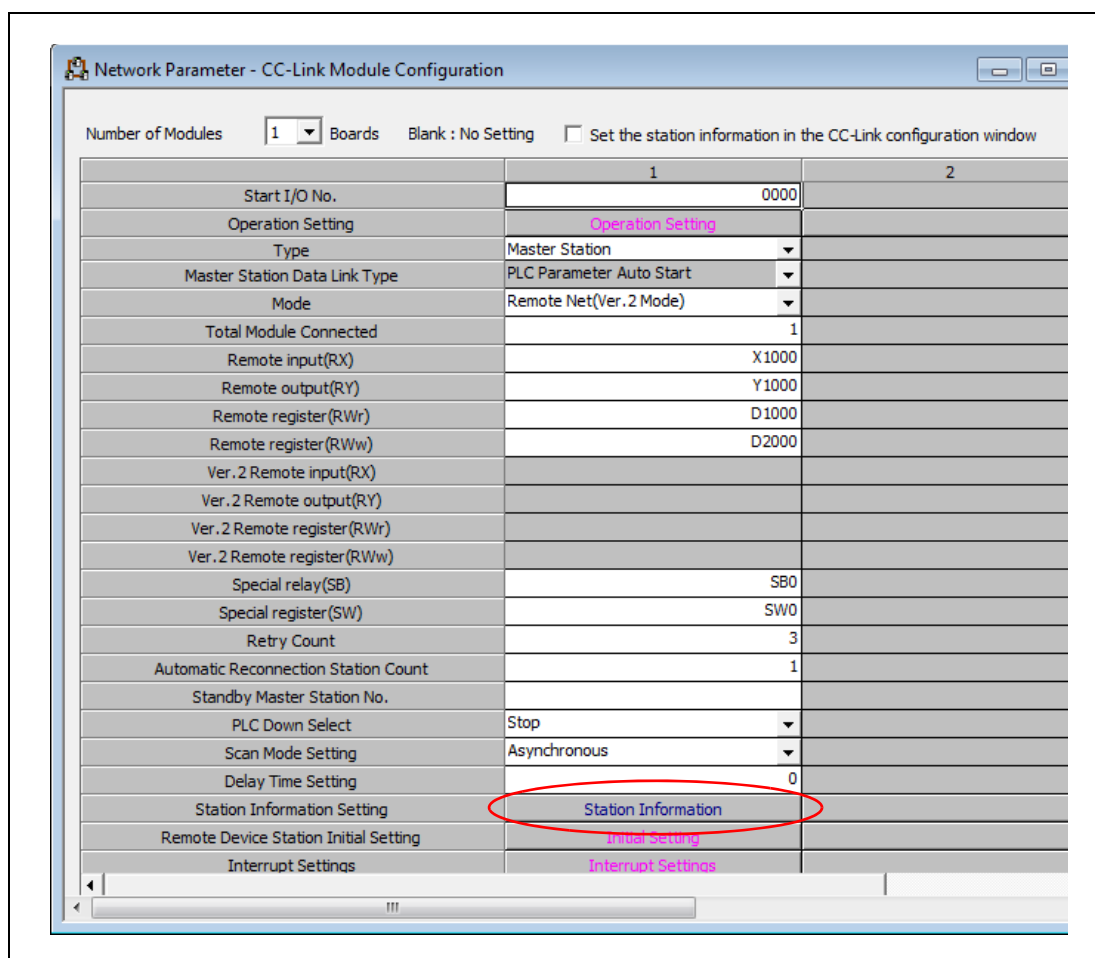
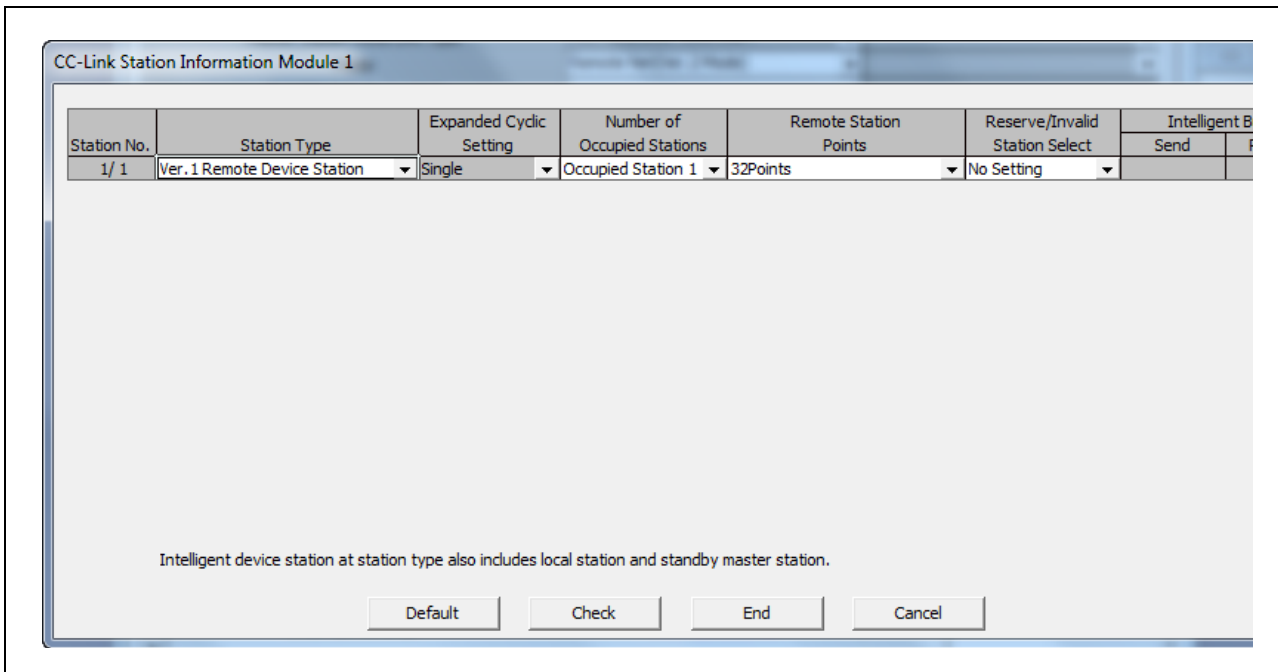


Fig. 3-17: CC-Link master parameter

Click on **Station Information**. This will open the screen shown on the next page.



**Abb. 3-18:** Parameter for the CC-Link slave station

Set the STlite modules to occupy 1 station. This will result in the following number of occupied devices in the PLC.

| Type of data    |   |           | Number of devices |
|-----------------|---|-----------|-------------------|
| Remote input    | RX (Inputs from digital input module STL-DI8-V1)    | Total     | 32 points         |
|                 |   | User area | 16 points         |
| Remote output   | RY (Outputs to digital output module STL-DO4)       | Total     | 32 points         |
|                 |   | User area | 16 points         |
| Remote register | RWr (Input data from analog input module STL-AD2-V) |           | 4 points          |
|                 | RWw (Output data to analog out module STL-DA4-V1)   |           | 4 points          |

**Tab. 3-28:** Number of remote devices for the CC-Link slave station

Combined with the head addresses for the remote devices entered in the master parameter, the process image is as follows (refer to section 3.2.8 and the appendix, section A.1):

| Type of data    |   | Devices                       | Remark   |
|-----------------|---|-------------------------------|--|
| Remote inputs   | RX (Inputs from digital input module STL-DI8-V1)    | User area<br>X1000 to X100F   | X1000 to X1007: X0 to X7 of STL-DI8-V1<br>X1008 to X100F: Not used       |
|                 |   | System area<br>X1010 to X101F | —  |
| Remote output   | RY (Outputs to digital output module STL-DO4)       | User area<br>Y1000 to Y100F   | Y1000 to Y1003: Y0 to Y3 of STL-DO4<br>X1004 to X100F: Not used          |
|                 |   | System area<br>Y1010 to Y101F | —  |
| Remote register | RWr (Input data from analog input module STL-AD2-V) | D1000 to D1003                | D1000: Channel 1, D1001: Channel 2<br>D1002, D1003: Not used             |
|                 | RWw (Output data to analog out module STL-DA4-V1)   | D2000 to D2003                | D2000: Channel 1, D2001: Channel 2<br>D2002: Channel 3, D2003: Channel 4 |

**Tab. 3-29:** Remote devices of the CC-Link slave station



### 3.3.4 Sequence Program for Initialization of the CC-Link Head Station

The program required for initialization of the head station STL-BT1 (refer to Fig. 3-14) is shown in the following illustrations.

|    | Class      | Label Name                      | Data Type          | Device | Address   |
|----|------------|---------------------------------|--------------------|--------|-----------|
| 1  | VAR_GLOBAL | RX_n_18_Init_Data_process_req   | Bit                | X1018  | %IX4120   |
| 2  | VAR_GLOBAL | RX_n_19_Init_Data_set_compl     | Bit                | X1019  | %IX4121   |
| 3  | VAR_GLOBAL | RX_n_1A_Error_Status            | Bit                | X101A  | %IX4122   |
| 4  | VAR_GLOBAL | RX_n_1B_Remote_station_READY    | Bit                | X101B  | %IX4123   |
| 5  | VAR_GLOBAL | RY_n_18_Init_Data_process_compl | Bit                | Y1018  | %QX4120   |
| 6  | VAR_GLOBAL | RY_n_19_Init_Data_set_req       | Bit                | Y1019  | %QX4121   |
| 7  | VAR_GLOBAL | STL_BT1_Station_IS_READY        | Bit                |        |           |
| 8  |            |                                 |                    |        |           |
| 9  | VAR_GLOBAL | Output_Byte1                    | Bit(0..7)          | Y1000  | %QX4096   |
| 10 | VAR_GLOBAL | Input_Byte1                     | Bit(0..7)          | X1000  | %IX4096   |
| 11 | VAR_GLOBAL | Output_Words                    | Word[Signed](0..3) | D2000  | %MW0.2000 |
| 12 | VAR_GLOBAL | Input_Words                     | Word[Signed](0..3) | D1000  | %MW0.1000 |
| 13 |            |                                 |                    |        |           |
| 14 |            |                                 |                    |        |           |

Abb. 3-19: Global Label settings

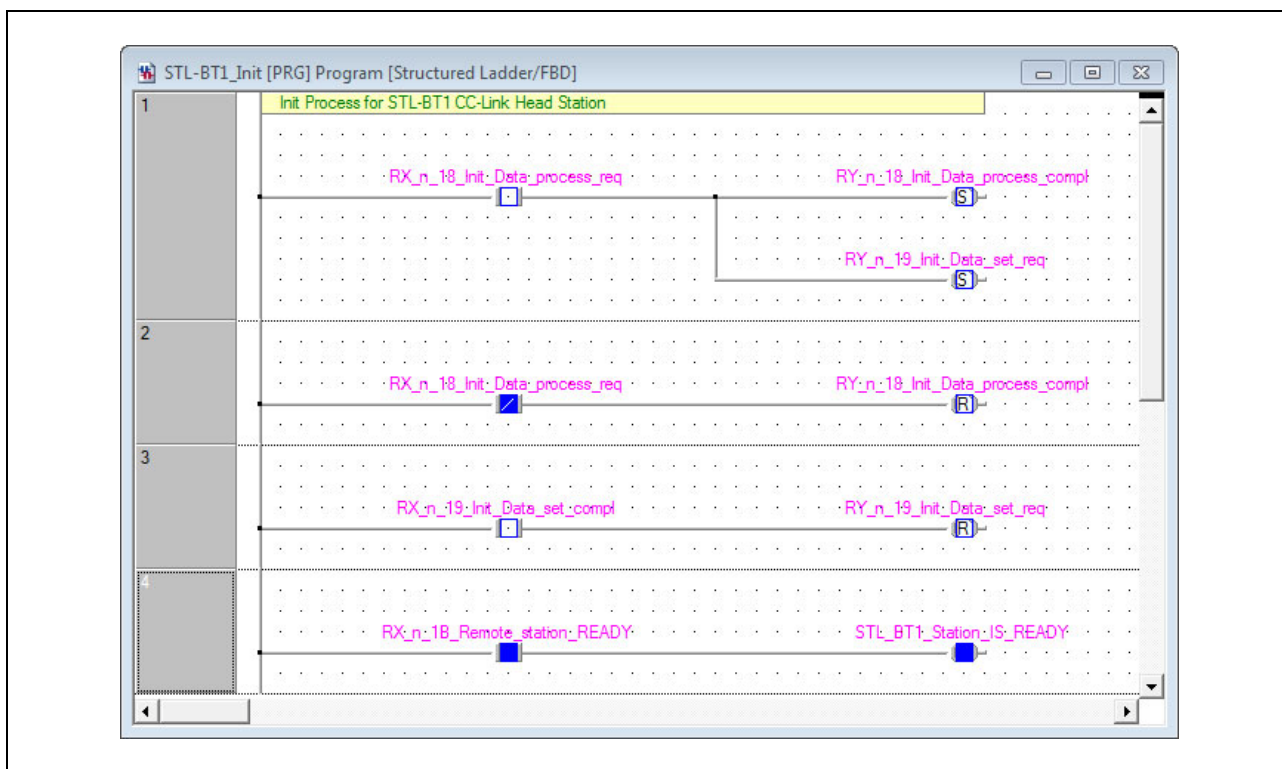


Abb. 3-20: Program for initialization of the STL-BT1

### 3.3.5 Monitoring the Data Transfer

After wiring the CC-Link network, downloading the program and the parameters to the PLC and starting the CC-Link communication by running the sequence program shown on the previous page, you can monitor the data transfer in the Device Monitor of GX Works2.

#### Remote inputs

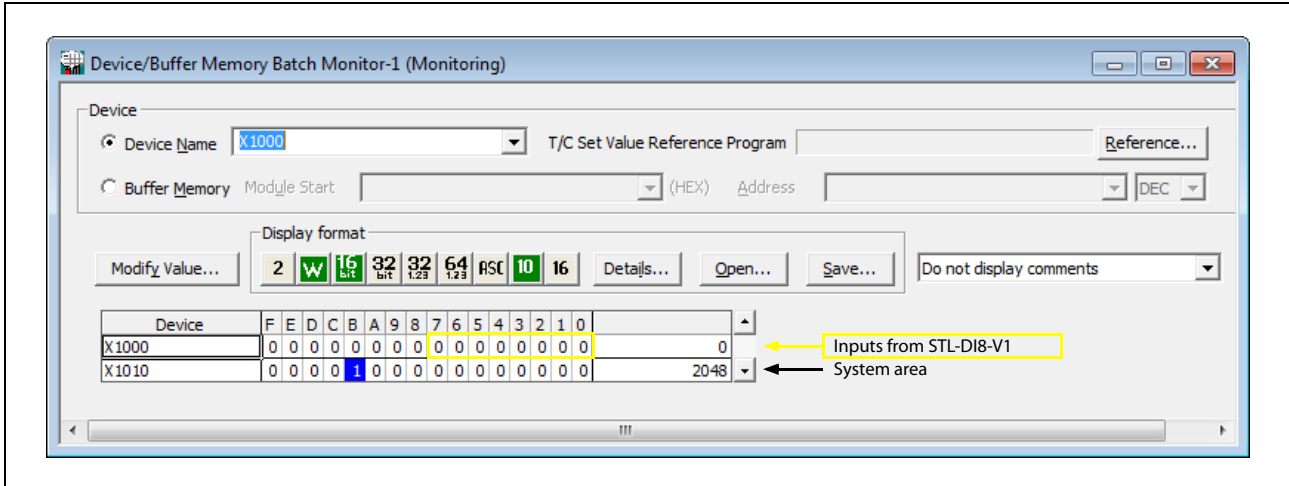


Abb. 3-21: Remote inputs (The input "Remote station ready" (X101B) is ON.)

#### Remote outputs

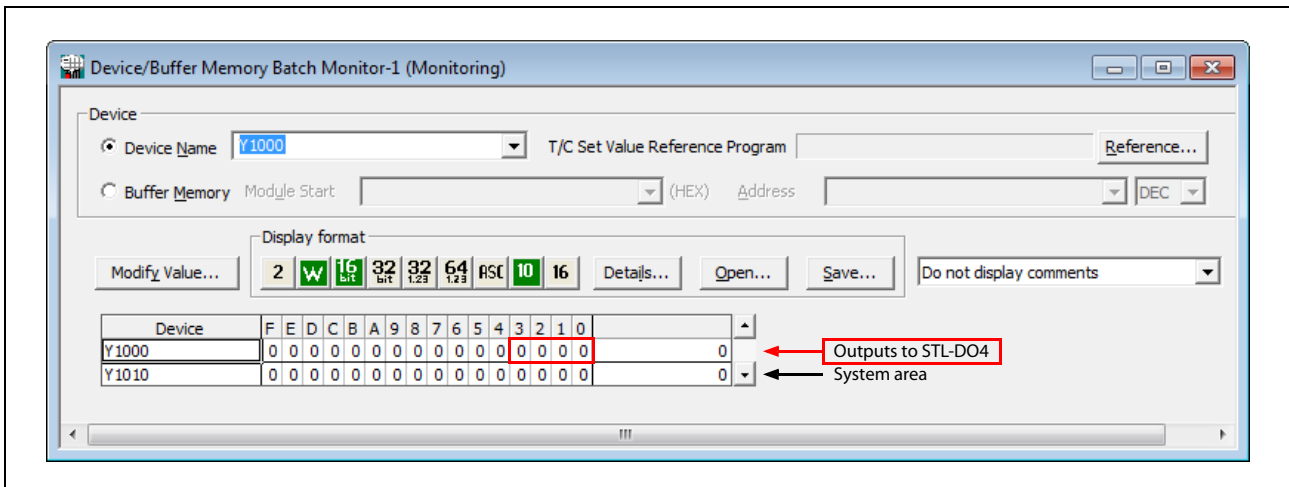
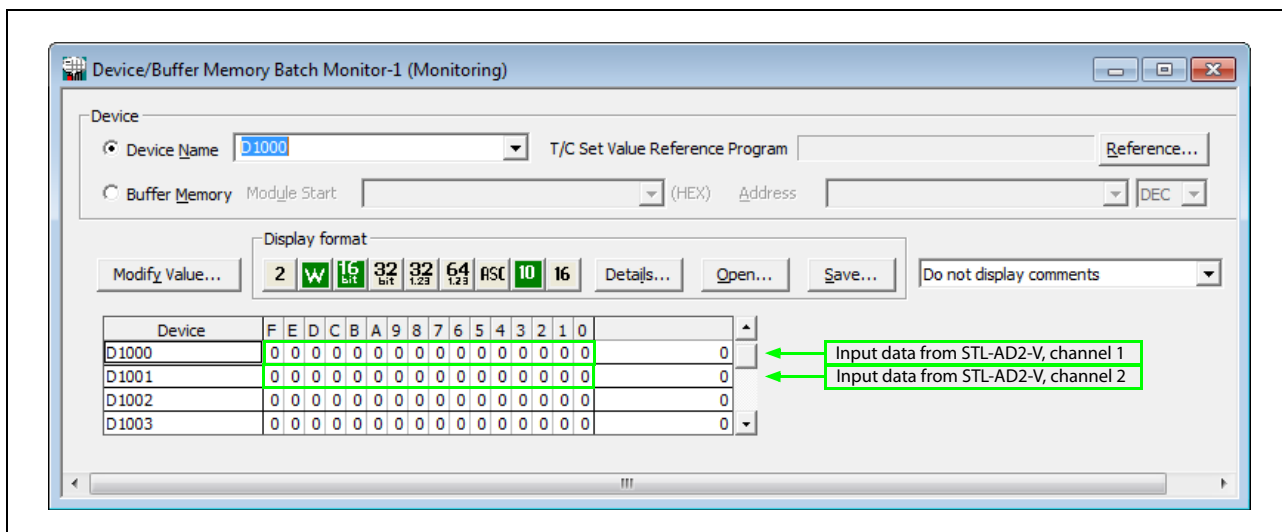


Abb. 3-22: Remote outputs for this example

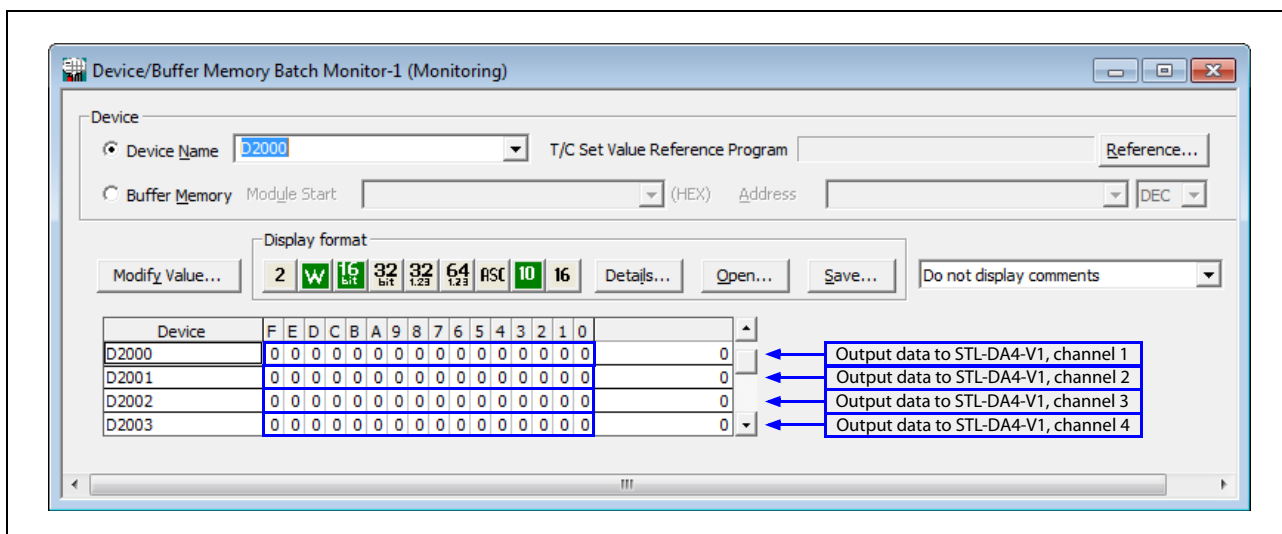
**Remote register RWr**



**Abb. 3-23:** Remote registers RWr

For the process images of the individual STlite modules please refer to the appendix, section A.1. For example, reading a value of 16384 (4000H) from D1000 means that a voltage of 5.00 V is applied to channel 1 of the STL-AD2-V.

**Remote register RWw**



**Abb. 3-24:** Remote registers RWw

If you want to output 10 V on channel 1 of the STL-DA4-V1, write 32760 (7FF8H) to D2000.



# 4 Ethernet

## 4.1 Overview

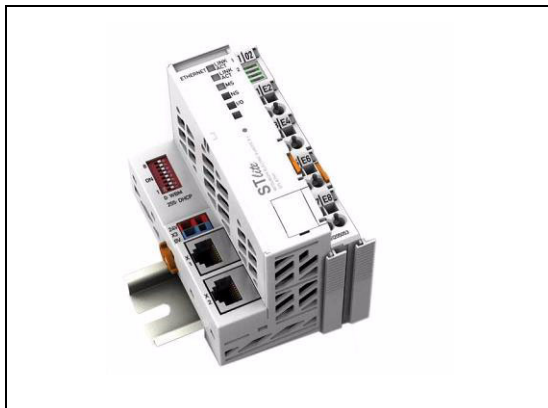
Ethernet is unrivalled for the widest possible set of connectable technologies. While being well established in the office and IT environments, its adoption into automation environments is both rapid and broad ranging.

Ethernet is a platform for a very wide range of data communications protocols. The combination of Ethernet and the extremely widespread TCP/IP protocol enables high-speed data communications between process supervision and the PLC.

There is also a growing demand for Ethernet to be used as a peer-to-peer network.

## 4.2 Head Station STL-ETH1 (Ethernet)

The head station STL-ETH1 connects the MELSEC STlite modules to the Ethernet fieldbus system. The STL-ETH1 can be used for widespread solutions in the field of factory automation.



**Fig. 4-1:** Head station STL-ETH1 for Ethernet (with connected digital input module)

Equipped with two RJ-45 ports, which both work as 2-channel switches, the head station enables easy and cost-effective cabling such as linear bus topology for which no additional external switches or hubs are required.

With the DIP switch the last byte of the IP address, as well as the assignment of the IP address (DHCP, BootP, firm setting) can be given.

In the head station, all input signals from the sensors are combined. After connection, the head station determines which I/O modules are on the node and creates a local process image from these. Analog and special function module data is sent via words and/or bytes; digital data is grouped bit-by-bit.

The local process image is divided into two data zones containing the data received and the data to be sent.

The data of the analog modules is mapped first into the process image. The modules are mapped in the order of their physical position after the head station.

The bits of the digital modules are combined into words and then mapped after the analog ones in the process image. If the number of digital I/Os is greater than 16 bits, the head station automatically begins a new word.

All sensor input signals are grouped in the head station (slave) and transferred to the higher-order controller (master) via the fieldbus. Process data linking is performed in the higher-order controller. The higher-order controller puts out the resulting data to the actuators via the bus and the node.

The fieldbus connection consists of two ports (RJ-45). An Ethernet switch integrated in the head station operates in the store and forward mode.

Both ports support:

- 10BASE-T / 100BASE-TX
- Full / Half duplex
- Autonegotiation
- Auto-MDI(X)

In order to send process data via Ethernet, the head station supports a series of network protocols.

The MODBUS/TCP(UDP) protocol and the Ethernet/IP protocol are implemented for exchanging process data. The two communication protocols can be used optional or together.

For the management and diagnosis of the system, the HTTP, SNMP and SNTP protocols are available.

For the data transfer via Ethernet the FTP is available.

For the automatic assignment of the IP address in the network, alternatively DHCP or BootP can be used.

An internal server is available for Web-based applications.

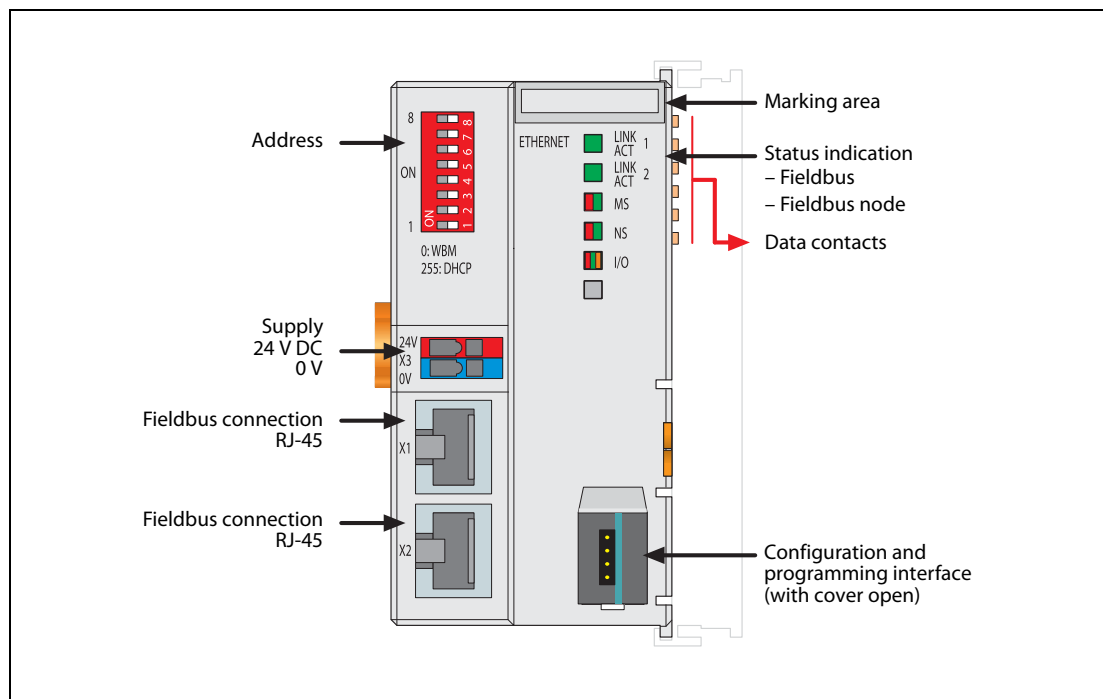
HTML pages stored in the head station allow access to information about the configuration, the status and the I/O data of the fieldbus node via Web browsers.

Using the implemented file system, it is also possible to store individual HTML pages.

#### NOTE

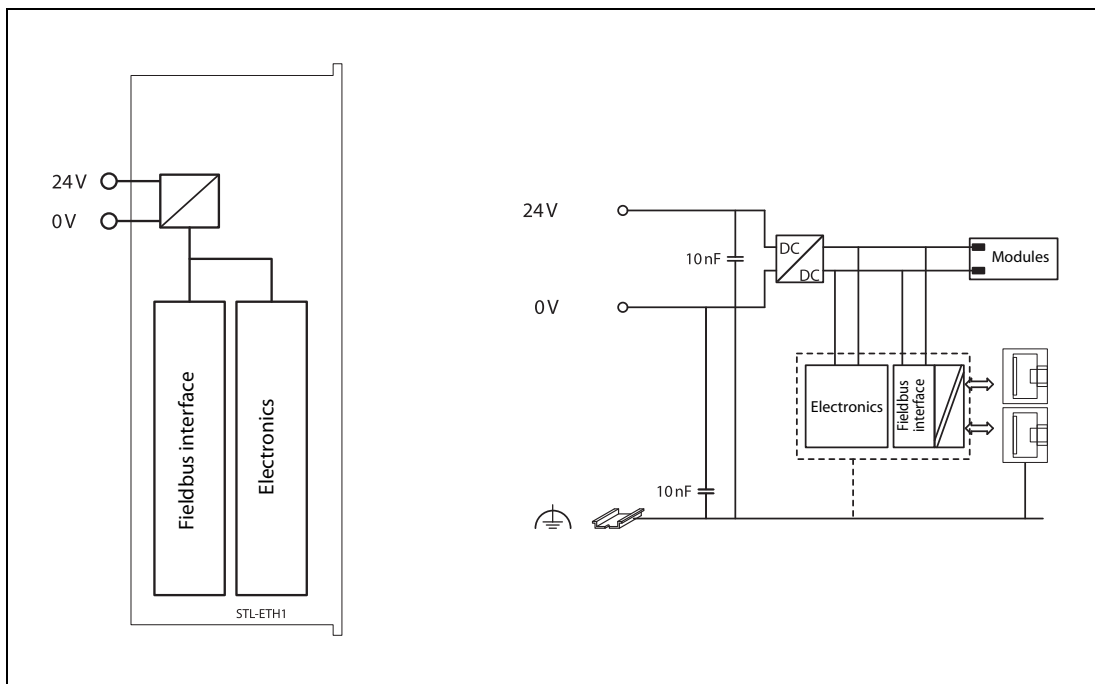
For the specifications of the head station STL-ETH1 please refer to the installation manual of the STLite series.

### 4.2.1 View



**Fig. 4-2:** Head station STL-ETH1 (Ethernet)

### 4.2.2 Device Supply

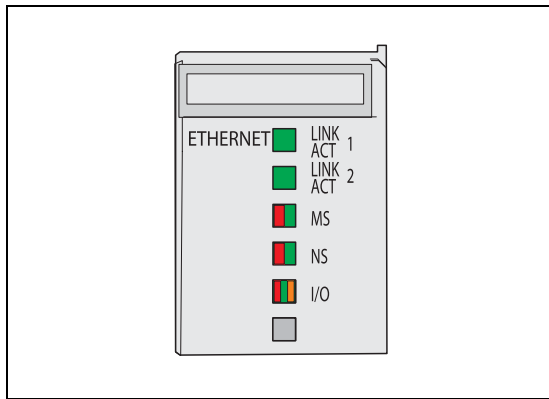


**Fig. 4-3:** Block diagram for the head station STL-ETH1 (Ethernet)

The device supply generates the necessary voltage to power the electronics of the device and the internal electronics of the connected I/O modules.

The fieldbus interface is galvanically separated from the electrical potential of the device via the transducer.

### 4.2.3 Display Elements



**Fig. 4-4:** The operating condition of the head station is signalled via LEDs.

The health of the Ethernet fieldbus is signalled through the top LED group (LINK ACT 1, LINK ACT 2, MS, and NS).

The two-colored LEDs "MS" (module status) and "NS" (network status) are solely used by the Ethernet/IP protocol. These two LEDs conform to the Ethernet/IP specifications.

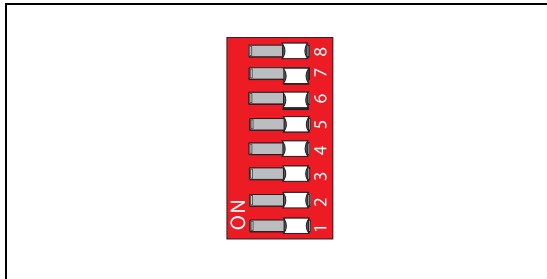
| Group           | LED               | Color   | Status  | Description   |
|-----------------|-------------------|---|---|---|
| Fieldbus status | LINK ACT 1        | Green   | ON  | The fieldbus node is connected to the physical network via port 1.  |
|                 |                   |   | Flashing  | The fieldbus node sends and receives Ethernet telegrams via port 1.   |
|                 |                   |   | OFF   | The fieldbus node is not connected to the physical network.   |
|                 | LINK ACT 2        | Green   | ON  | The fieldbus node is connected to the physical network via port 2.  |
|                 |                   |   | Flashing  | The fieldbus node sends and receives Ethernet telegrams via port 2.   |
|                 |                   |   | OFF   | The fieldbus node is not connected to the physical network.   |
|                 | MS                | Green   | ON  | Normal operation  |
|                 |                   |   | Flashing  | The system is not yet configured.   |
|                 |                   | Red   | ON  | The system indicates a not remediable error.  |
|                 |                   | Red/green   | Flashing  | Self test   |
|                 | NS                | Green   | ON  | At least one connection (MODBUS/TCP or Ethernet/IP) is established (also connection to the Message router applies). |
|                 |                   |   | Flashing  | No connection (MODBUS/TCP or Ethernet/IP).  |
| Red             |                   | ON  | The system indicates a double IP address in the network.  |   |
|                 |                   | Flashing  | At least one connection (MODBUS/TCP or Ethernet/IP) announced a Time-out, where the controller functions as target. |   |
| Red/green       |                   | Flashing  | Self test   |   |
| —               |                   | OFF   | No IP address is assigned to the system.  |   |
| Node status     | I/O               | Green   | ON  | The fieldbus node is operating correctly.   |
|                 |                   | Orange  | Flashing  | The internal data bus is initialized, 1-2 seconds of rapid flashing indicate start-up.                              |
|                 | Red               | ON  | Controller hardware defect  |   |
|                 |                   | Flashing  | General internal bus error*   |   |
|                 | Cyclical flashing | Up to three successive blinking sequences indicate internal data bus errors. There are short intervals between the sequences. |   |   |
| —               | OFF               | No data cycle on the internal bus. (The head station/controller supply is off.)   |   |   |

**Tab. 4-1:** Description of the LEDs of the STL-ETH1

\* The blinking of the I/O LED indicates an error message comprised of an error code and error argument. Please refer to the manual of the STL-ETH1 for a detailed description of the blink codes.



### 4.2.4 Address Selection Switch



**Fig. 4-5:** Address selection switch of the STL-ETH1

There are two ways to allocate the IP Address to the fieldbus node:

- Manually assignment of the IP address using of the address selection switch
- Automatic assignment of addresses via a DHCP server on the network.

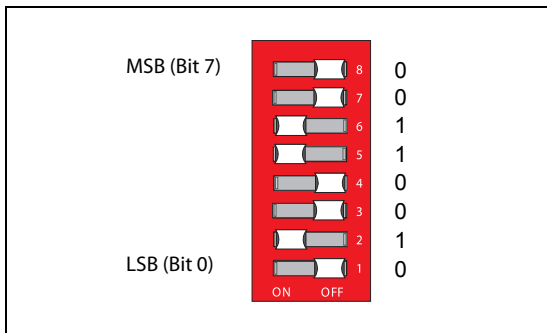
**NOTE**

The assignment of the IP addresses via DHCP and the changing of the static base address is not covered in this Quick start manual. For a detailed description please refer to the user’s manual for the STL-ETH1.

The address selection switch is used to set the host ID (last digit of the IP address). The coding of the host ID is bit by bit and begins with address selection switch 1 for bit 0 (LSB) and ends with address selection switch 8 for bit 7 (MSB).

The base address used depends on the IP address currently saved in the head station. With the original factory settings, the IP address is configured to the value 0.0.0.0. by default. In this case, the static base address 192.168.1.X is used.

Use the address selection switch to set the host ID, i.e., the last byte ("X") of the IP address saved in the head station with values between 1 and 254 binary coded.



**Fig. 4-6:** Example for an address selection switch setting for the host ID 50 (binary code: 00110010). This results in the IP address 192.168.1.50

Restart the head station after adjusting the address selection switch to apply the configuration changes.

**NOTES**

Use the address selection switch to set the last byte ("X") of the IP address to a value between 1 and 254. The DIP switch is then enabled and the IP address is composed of the base address stored in the head station and the host ID set on the DIP switch. The IP address setting via the Web-based Management System is disabled.

If you use the address selection switch to set the value 0 or 255, the address selection switch is disabled and the setting configured in the head station is used.

- With the value 0, the settings of the Web based Management System apply.
- If you set the value 255, the configuration via DHCP is activated.

### 4.2.5 Hardware Address (MAC ID)

Each ETHERNET head station STL-ETH1 has a unique and internationally unambiguous physical address, referred to as the MAC-ID (Media Access Control Identity). This is located on the rear of the controller and on a self-adhesive tearoff label on the side of the controller.

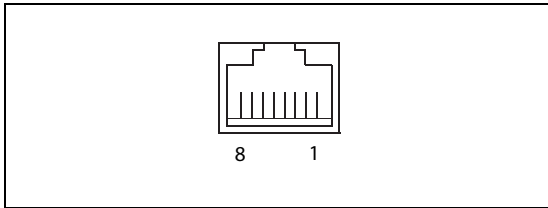
The MAC ID has a set length of 6 bytes (48 bits) (hexadecimal). The first three bytes identify the manufacturer. The second 3 bytes indicate the consecutive serial number for the hardware. (e.g. 00:30:DE:nn:nn:nn)

Write down the head station’s MAC address before mounting the head station.

### 4.2.6 Fieldbus Connection

The connection to the fieldbus is made via two RJ-45 plugs, which are connected to the fieldbus controller via an integrated switch.

The integrated switch works in store-and-forward operation and for each port, supports the transmission speeds 10/100 Mbit/s as well as the transmission modes full and half-duplex and autonegotiation. The wiring of these plugs corresponds to the specifications for 100BaseTX, which prescribes a category 5 twisted pair cable as the connecting cable. Cable types S-UTP (Screened Unshielded Twisted Pair) and STP (Shielded Twisted Pair) with a maximum segment length of 100 m (approximately 328 feet) can be used. The RJ-45 socket is physically lower, allowing the head station to fit in an 80 mm high enclosure once connected.



**Fig. 4-7:** RJ45 type modular jack

| Pin of the RJ45 plug | Signal | Description       |
|----------------------|--------|-------------------|
| 1                    | TD+    | Transmit-Data (+) |
| 2                    | TD-    | Transmit-Data (-) |
| 3                    | RD+    | Receive-Data (+)  |
| 4                    | —      | Not used          |
| 5                    | —      |                   |
| 6                    | RD-    | Receive-Data (-)  |
| 7                    | —      | Not used          |
| 8                    | —      |                   |

**Tab. 4-2:** Pin configuration of the fieldbus interface of the STL-ETH1



**CAUTION:**

**Not for use in telecommunication circuits!**

**Only use devices equipped with Ethernet or RJ-45 connectors in LANs. Never connect these devices with telecommunication networks.**

## 4.2.7 Process Data Architecture

After switching on the supply voltage, the head station identifies all I/O modules connected with the node that send or receive data (data width/bit width > 0). In the maximum total extension the node can consist of a mixed arrangement of a maximum of 64 analog, digital I/O modules or special function modules connected on the head station.

The data of the digital I/O modules are bit-oriented; i.e., digital data are sent bit by bit. The data of the analog and special function modules are byte-oriented; i.e., data are sent byte by byte.

The head station stores the process data in the process images. The head station works with a process output data image (PIO) and a process input data image (PII).

The PIO is filled by the fieldbus master with the process output data. The PII is filled by the head station with the process input data.

Into the input and output process image the data of the I/O modules are stored in the sequence of its position after the head station in the individual process image. First, all the byte-oriented I/O modules (analog I/O and special function modules) are stored in the process image, then the bit-oriented digital I/O modules. The bits of the digital I/O modules are grouped into bytes. If the amount of digital I/O information exceeds 8 bits, the head station automatically starts a new byte.

### NOTES

Avoid equipment damages due to addressing errors!

To avoid equipment damages within the field range, you must consider that, depending on the specific position of an I/O module in the fieldbus node, the process data of all previous byte or bit-oriented modules must be taken into account to determine its location in the process data map.

Consider the Process Data size for each module!

Observe the number of input and output bits or bytes for the individual I/O modules.

### Data Exchange

With the head station, data is exchanged either via the MODBUS/TCP protocol or via Ethernet/IP.

### NOTE

In this Quick start manual, only the data exchange via MODBUS/TCP is covered.

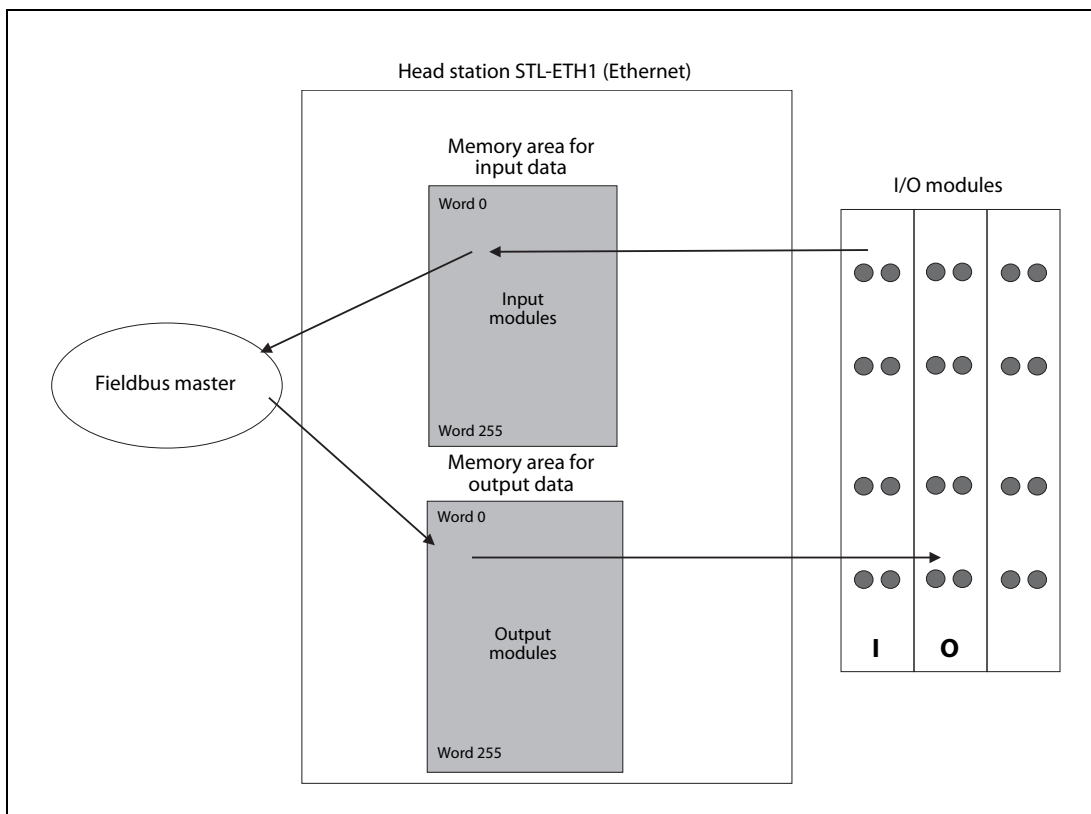
MODBUS/TCP works according to the master/slave principle. The master controller can be a PC or a PLC. The head station STL-ETH1 is a slave device.

The master requests communication. This request can be directed to certain nodes by addressing. The nodes receive the request and, depending on the request type, send a reply to the master.

The STL-ETH1 is essentially equipped with two interfaces for data exchange:

- the interface to the fieldbus (Master)
- the interface to the I/O modules.

Data exchange takes place between the fieldbus master and the I/O modules. If MODBUS is used as the fieldbus, the MODBUS master accesses the data using the MODBUS functions implemented in the head station.



**Fig. 4-8:** Memory areas and data exchange

The input module data can be read by the CPU and by the fieldbus side. Likewise, data can be written to the output modules from the CPU and the fieldbus side.

In addition, all output data is mirrored in the STL-ETH1 to a memory area with the address offset 0200H and 1000H. This allows output values to be read back in by adding 0200H or 1000H to the MODBUS address.

**Addressing**

Module inputs and outputs in a head station are addressed internally as soon as they are started. The order in which the connected modules are addressed depends on the type of module that is connected (input module, output module). The process image is formed from these addresses. The physical arrangement of the I/O modules in the fieldbus node is arbitrary.

Addressing first references complex modules (modules that occupy several bytes) in accordance with their physical order downstream of the head station; i.e., they occupy addresses starting from word 0.

Following these is the data for the remaining modules, compiled in bytes (modules that occupy less than one byte). In this process, byte by byte is filled with this data in the physical order. As soon a complete byte is occupied by the bit oriented modules, the process begins automatically with the next byte.

**NOTES**

Hardware changes can result in changes of the process image!  
 If the hardware configuration is changed and/or expanded; this may result in a new process image structure. In this case, the process data addresses also change. If adding modules, the process data of all previous modules has to be taken into account.

Observe process data quantity!  
 For the number of input and output bits or bytes of the individual IO modules please refer to the corresponding I/O module description in the appendix of this manual.

**Data Exchange between MODBUS/TCP Master and I/O Modules**

Data exchange between the MODBUS/TCP Master and the I/O modules is conducted using the MODBUS functions implemented in the controller by means of bit-by-bit or word-by-word reading and writing routines.

There are 4 different types of process data in the controller:

- Input words
- Output words
- Input bits
- Output bits

Access by word to the digital I/O modules is carried out in accordance with the following table:

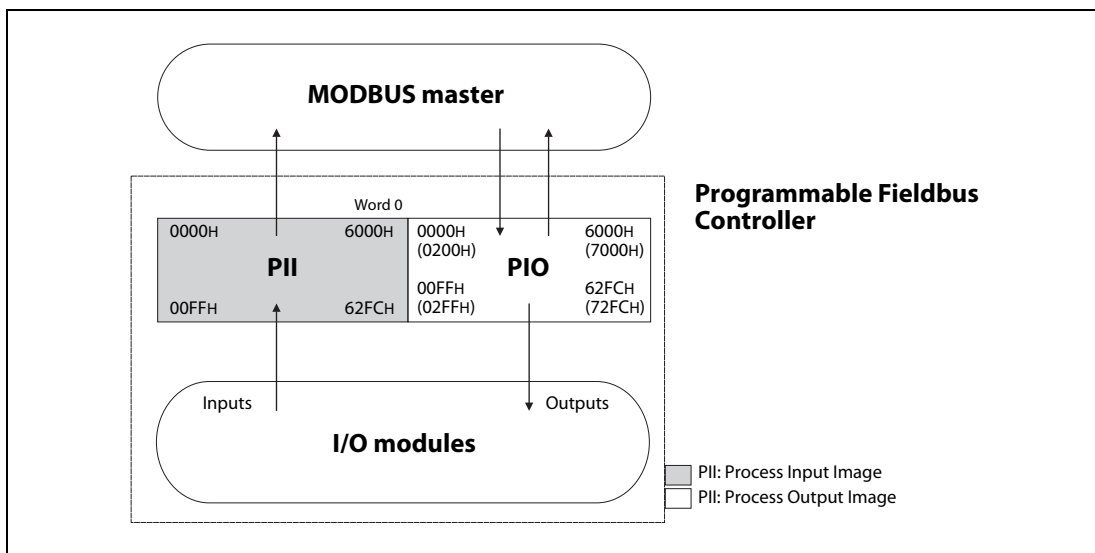
| Digital Inputs/Outputs | 16.          | 15.    | 14.    | 13.    | 12.    | 11.    | 10.   | 9.    | 8.    | 7.    | 6.          | 5.    | 4.    | 3.    | 2.    | 1.    |
|------------------------|--------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------------|-------|-------|-------|-------|-------|
| Process data word      | Bit 15       | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5       | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Byte                   | High byte D1 |        |        |        |        |        |       |       |       |       | Low byte D0 |       |       |       |       |       |

**Tab. 4-3:** Allocation of digital inputs and outputs to process data words

Output can be read back in by adding an offset of 0200H to the MODBUS address.

**NOTE**

Data > 256 words can be read back by using the cumulative offset!  
 All output data greater than 256 words and, therefore located in the memory range 6000H to 62FCH, can be read back by adding an offset of 1000H to the MODBUS address.



**Fig. 4-9:** Data exchange between MODBUS Master and I/O modules

Register functions start at address 1000H. These functions can be addressed in a similar manner with the MODBUS function codes that are implemented (read/write).

The specific register address is then specified instead of the address for a module channel.

## Allocation of the Input and Output Data

### NOTE

For the meaning of input and output bits or bytes of the connected STLite modules please refer to the corresponding I/O module description in the appendix of this manual.

#### ● Digital input modules

Digital input modules supply one bit of data per input to specify the signal state for the corresponding input. These bits are mapped into the Input Process Image.

When analog input modules are also present in the node, the digital data is always appended after the analog data in the Input Process Image, grouped into bytes.

| Type of module        | Name       | ID number | Description                               | Process Image [Bit] |        |
|-----------------------|------------|-----------|---|---------------------|--------|
|                       |            |           |   | Input               | Output |
| Digital input modules | STL-DI8-V1 | 51205052  | 8 inputs for source type sensors, 24 V DC | 8                   | 0      |
|                       | STL-DI8-V2 | 51205053  | 8 inputs for source type sensors, 24 V DC | 8                   | 0      |

**Tab. 4-4:** Process data of digital input modules

| Input Process Image |          |          |          |          |          |          |          |
|---------------------|----------|----------|----------|----------|----------|----------|----------|
| Bit 7               | Bit 6    | Bit 5    | Bit 4    | Bit 3    | Bit 2    | Bit 1    | Bit 0    |
| Input X7            | Input X6 | Input X5 | Input X4 | Input X3 | Input X2 | Input X1 | Input X0 |

**Tab. 4-5:** Input process image of digital input modules with 8 inputs

#### ● Digital output modules

Digital output modules use one bit of data per output. These bits are mapped into the Output Process Image.

When analog output modules are also present in the node, the digital image data is always appended after the analog data in the Output Process Image, grouped into bytes.

| Type of module         | Name    | ID number | Description                                       | Process Image [Bit] |        |
|------------------------|---------|-----------|---|---------------------|--------|
|                        |         |           |   | Input               | Output |
| Digital output modules | STL-DO4 | 51205045  | 4 transistor outputs, 24 V DC, 0.5 A, source type | 0                   | 4      |
|                        | STL-DO8 | 51205043  | 8 transistor outputs, 24 V DC, 0.5 A, source type | 0                   | 8      |
|                        | STL-RO2 | 51205044  | 2 relay outputs 230 V AC / 30V DC, 500 VA/60 W    | 0                   | 2      |

**Tab. 4-6:** Process data of digital output modules

| Output Process Image |       |       |       |           |           |           |           |
|----------------------|-------|-------|-------|-----------|-----------|-----------|-----------|
| Bit 7                | Bit 6 | Bit 5 | Bit 4 | Bit 3     | Bit 2     | Bit 1     | Bit 0     |
|                      |       |       |       | Output Y3 | Output Y2 | Output Y1 | Output Y0 |

**Tab. 4-7:** Allocation of data for the digital output module STL-DO4

| Output Process Image |           |           |           |           |           |           |           |
|----------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit 7                | Bit 6     | Bit 5     | Bit 4     | Bit 3     | Bit 2     | Bit 1     | Bit 0     |
| Output Y7            | Output Y6 | Output Y5 | Output Y4 | Output Y3 | Output Y2 | Output Y1 | Output Y0 |

**Tab. 4-8:** Allocation of data for the digital output module STL-DO8

| Output Process Image |       |       |       |       |       |           |           |
|----------------------|-------|-------|-------|-------|-------|-----------|-----------|
| Bit 7                | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1     | Bit 0     |
|                      |       |       |       |       |       | Output Y1 | Output Y0 |

**Tab. 4-9:** Allocation of data for the relay output module STL-RO2

● Analog input modules

The hardware of an analog input module has 16 bits of measured analog data per channel and 8 bits of control/status. However, the head station/controller with MODBUS/TCP does not have access to the 8 control/status bits. The 16 bits of analog data per channel are grouped as words and mapped in Intel format in the Input Process Image.

When digital input modules are also present in the node, the analog input data is always mapped into the Input Process Image in front of the digital data.

- Two-channel analog input modules

| Type of module       |             | Name      | ID number | Description                                | Process Image [Byte] |        |
|----------------------|-------------|-----------|-----------|--|----------------------|--------|
|                      |             |           |           |  | Input                | Output |
| Analog input modules | Voltage     | STL-AD2-V | 51205046  | 2 inputs 0 to 10 V                         | 4                    | 0      |
|                      | Current     | STL-AD2-I | 51205047  | 2 inputs 4 to 20 mA                        |                      |        |
|                      | Temperature | STL-TI2   | 51205048  | 2 inputs for Pt100 resistance thermometers |                      |        |

**Tab. 4-10:** Process data of two-channel analog input modules

| Input Process Image |                  |          |          | Description            |
|---------------------|------------------|----------|----------|------------------------|
| Offset              | Byte Destination |          | Low Byte |                        |
|                     | High Byte        | Low Byte |          |                        |
| 0                   | D1               | D0       |          | Analog input Channel 1 |
| 1                   | D3               | D2       |          | Analog input Channel 2 |

**Tab. 4-11:** Allocation of data for two-channel analog input modules

- Four-channel analog input modules

| Type of module       |         | Name       | ID number | Description          | Process Image [Byte] |        |
|----------------------|---------|------------|-----------|----------------------|----------------------|--------|
|                      |         |            |           |                      | Input                | Output |
| Analog input modules | Voltage | STL-AD4-V1 | 51205049  | 4 inputs 0 to 10 V   | 8                    | 0      |
|                      |         | STL-AD4-V2 | 51205050  | 4 inputs -10 to 10 V |                      |        |
|                      | Current | STL-AD4-I  | 51205051  | 4 inputs 4 to 20 mA  |                      |        |

**Tab. 4-12:** Process data of four-channel analog input modules

| Input Process Image |                  |          |          | Description            |
|---------------------|------------------|----------|----------|------------------------|
| Offset              | Byte Destination |          | Low Byte |                        |
|                     | High Byte        | Low Byte |          |                        |
| 0                   | D1               | D0       |          | Analog input Channel 1 |
| 1                   | D3               | D2       |          | Analog input Channel 2 |
| 2                   | D5               | D4       |          | Analog input Channel 3 |
| 3                   | D7               | D6       |          | Analog input Channel 4 |

**Tab. 4-13:** Allocation of data for four-channel analog input modules

- Analog output modules

The hardware of an analog output module has 16 bits of analog data per channel and 8 bits of control/status. However, the head station/controller with MODBUS/TCP does not have access to the 8 control/status bits. The 16 bits of analog data per channel are grouped as words and mapped in Intel format in the Output Process Image.

When digital output modules are also present in the node, the analog output data is always mapped into the Output Process Image in front of the digital data.

- Two-channel analog output modules

| Type of module        | Name    | ID number | Description | Process Image [Byte] |        |   |
|-----------------------|---------|-----------|-------------|----------------------|--------|---|
|                       |         |           |             | Input                | Output |   |
| Analog output modules | Voltage | STL-DA2-V | 51205042    | 2 outputs 0 to 10 V  | 0      | 4 |
|                       | Current | STL-DA2-I | 51205041    | 2 outputs 4 to 20 mA |        |   |

**Tab. 4-14:** Process data of two-channel analog output modules

| Output Process Image |                  |          | Description             |
|----------------------|------------------|----------|-------------------------|
| Offset               | Byte Destination |          |                         |
|                      | High Byte        | Low Byte |                         |
| 0                    | D1               | D0       | Analog output Channel 1 |
| 1                    | D3               | D2       | Analog output Channel 2 |

**Tab. 4-15:** Allocation of data for two-channel analog output modules

- Four-channel analog output modules

| Type of module        | Name    | ID number  | Description | Process Image [Byte]  |        |   |
|-----------------------|---------|------------|-------------|-----------------------|--------|---|
|                       |         |            |             | Input                 | Output |   |
| Analog output modules | Voltage | STL-DA4-V1 | 51205038    | 4 outputs 0 to 10 V   | 0      | 8 |
|                       |         | STL-DA4-V2 | 51205039    | 4 outputs -10 to 10 V |        |   |
|                       | Current | STL-DA4-I  | 51205040    | 4 outputs 4 to 20 mA  |        |   |

**Tab. 4-16:** Process data of four-channel analog output modules

| Output Process Image |                  |          | Description             |
|----------------------|------------------|----------|-------------------------|
| Offset               | Byte Destination |          |                         |
|                      | High Byte        | Low Byte |                         |
| 0                    | D1               | D0       | Analog output Channel 1 |
| 1                    | D3               | D2       | Analog output Channel 2 |
| 2                    | D5               | D4       | Analog output Channel 3 |
| 3                    | D7               | D6       | Analog output Channel 4 |

**Tab. 4-17:** Allocation of data for four-channel analog output modules



● Encoder module STL-ENC

| Type of module | Name    | ID number | Description                          | Process Image [Byte] |        |
|----------------|---------|-----------|--------------------------------------|----------------------|--------|
|                |         |           |                                      | Input                | Output |
| Encoder module | STL-ENC | 51205116  | Input module for incremental encoder | 6                    | 6      |

**Tab. 4-18:** Process data of the encoder module

The Incremental Encoder Interface Module has a total of 6 bytes of user data in both the Input and Output Process Image (4 bytes of encoder data and 2 bytes of control/status). The following table illustrates the Input and Output Process Image, which have 4 words mapped into each image. Word alignment is applied.

| Input and Output Process Image |                  |          | Description                      |
|--------------------------------|------------------|----------|----------------------------------|
| Offset                         | Byte Destination |          |                                  |
|                                | High Byte        | Low Byte |                                  |
| 0                              | —                | C0/S0    | Control/Status byte of Channel 1 |
| 1                              | D2               | D1       | Data value of Channel 1          |
| 2                              | —                | C1/S1    | Control/Status byte of Channel 2 |
| 3                              | D3               | D2       | Data value of Channel 2          |

**Tab. 4-19:** Allocation of data for the encoder module STL-ENC

● Counter module STL-C100

| Type of module | Name     | ID number | Description                                     | Process Image [Byte] |        |
|----------------|----------|-----------|---|----------------------|--------|
|                |          |           |   | Input                | Output |
| Counter module | STL-C100 | 51244881  | Forward/reverse counter, max. frequency 100 kHz | 5                    | 5      |

**Tab. 4-20:** Process data of the counter module

The above counter module has a total of 5 bytes of user data in both the Input and Output Process Image (4 bytes of counter data and 1 byte of control/status). The counter value is supplied as 32 bits. The following tables illustrate the Input and Output Process Image, which has a total of 3 words mapped into each image. Word alignment is applied.

| Input Process Image |                  |          | Description   |
|---------------------|------------------|----------|---------------|
| Offset              | Byte Destination |          |               |
|                     | High Byte        | Low Byte |               |
| 0                   | —                | S        | Status byte   |
| 1                   | D1               | D0       | Counter value |
| 2                   | D3               | D2       |               |

**Tab. 4-21:** Input Process Image of the counter module

| Output Process Image |                  |          | Description           |
|----------------------|------------------|----------|-----------------------|
| Offset               | Byte Destination |          |                       |
|                      | High Byte        | Low Byte |                       |
| 0                    | —                | C        | Control byte          |
| 1                    | D1               | D0       | Counter setting value |
| 2                    | D3               | D2       |                       |

**Tab. 4-22:** Output Process Image of the counter module

- SSI interface module

| Type of module   | Name    | ID number | Description                  | Process Image [Byte] |        |
|------------------|---------|-----------|------------------------------|----------------------|--------|
|                  |         |           |                              | Input                | Output |
| Interface module | STL-SSI | 51205057  | Input module for SSI encoder | 4                    | 0      |

**Tab. 4-23:** Process data of the interface module STL-SSI

The SSI Interface module has a total of 4 bytes of user data in the Input Process Image, which has 2 words mapped into the image. Word alignment is applied.

| Input Process Image |                  |          | Description |
|---------------------|------------------|----------|-------------|
| Offset              | Byte Destination |          |             |
|                     | High Byte        | Low Byte |             |
| 0                   | D1               | D0       | Data bytes  |
| 1                   | D3               | D2       |             |

**Tab. 4-24:** Allocation of data for the SSI interface module STL-SSI

### 4.3 Configuration Example for MELSEC System Q

For this example, a MODBUS/TCP slave consisting of the following STLite modules is used:

- Head station STL-BT1
- Power supply module STL-BPS (with bus power supply)
- Digital input module STL-DI8-V1 (8 inputs)
- Digital output module STL-DO4 (4 outputs)
- Analog output module STL-DA4-V1 (4 channels, 0 to 10 V)
- Analog input module STL-AD2-V (2 channels, 0 to 10 V)
- End module STL-ET

**NOTE**

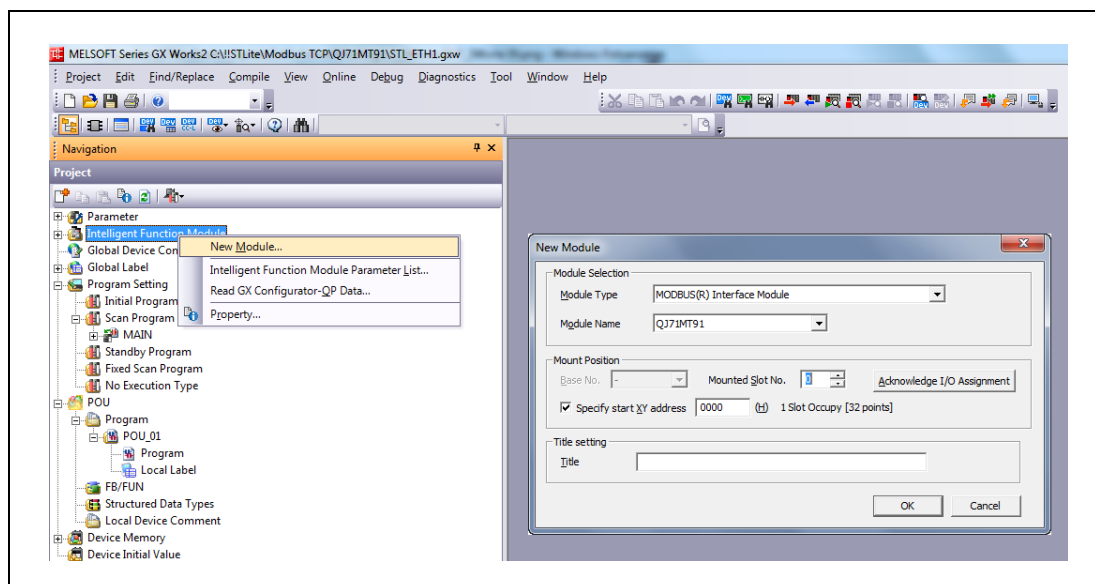
For the specifications of the modules and the installation procedures please refer to the installation manual of the STLite series.

STLite modules with power contacts (male contacts) cannot be linked to bus modules with fewer power contacts. In this case install a power supply module between the two relevant modules.

#### 4.3.1 Settings for the Master Station

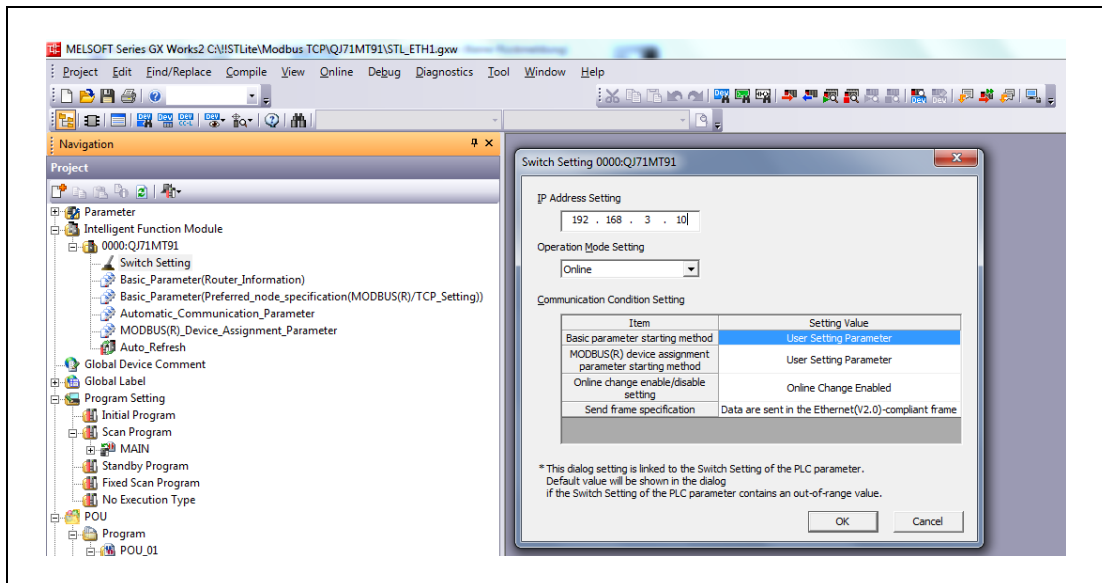
Start GX Works2. In the project navigator window, select **Intelligent Function module**. Right click and select **New module**.

Select the MODBUS Interface Module QJ71MT91 and click **OK**.



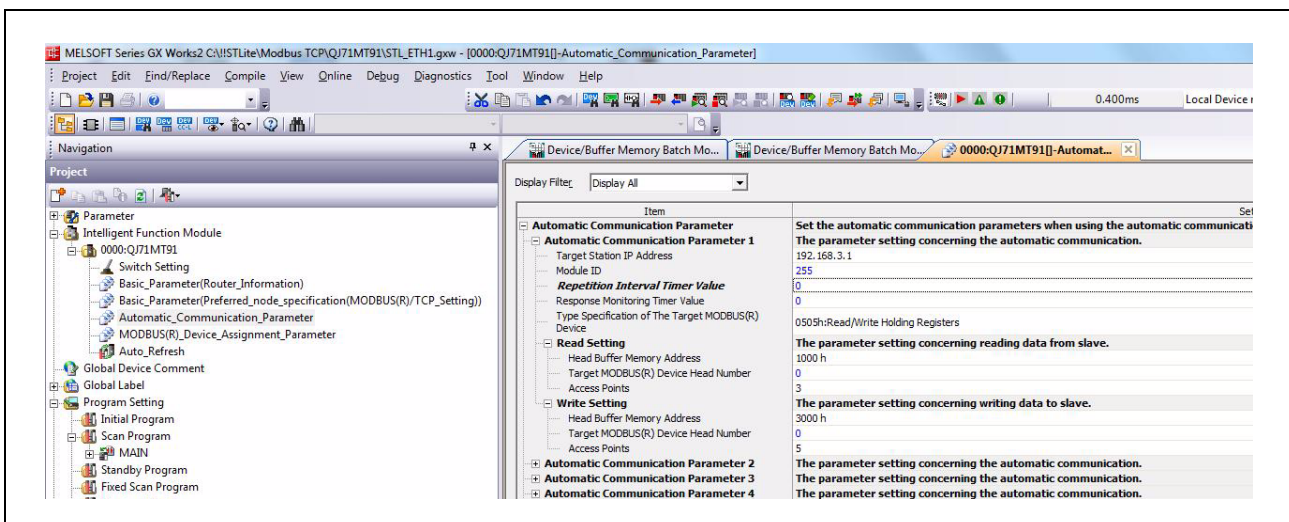
**Fig. 4-10:** In this example, the QJ71MT91 is mounted to slot 0.

Then, in the project navigator window, select **Intelligent Function module** -> **QJ71MT91** and double click on **Switch Setting**. Enter the IP Address of the QJ71MT91 (see illustration on the next page).



**Fig. 4-11:** Setting the IP address of the MODBUS master.

Still in the project navigator window, select **Intelligent Function module -> QJ71MT91** and double click on **Automatic\_Communication\_Parameter**.



**Abb. 4-12:** Setting the automatic communication parameter

Enter the following:

- the IP-Address of the head station STL-ETH1
- the Module ID
- the number of read access points (input words; "3" in this example)
- the number of write access points (output words; "5" in this example)
- the values for the Repetition Interval Timer and the Response Monitoring Timer (set both values to "0" for an update as fast as possible)

Double click on **Auto\_Refresh** in the selection tree for the **QJ71MT91** in the project navigator window and enter the PLC devices for input and output data.

In this example, 3 data registers from D1000 onward are reserved for input data from the MODBUS/TCP node and 5 registers, starting with D2000, serve as output buffer holding data for the STL-ETH1.

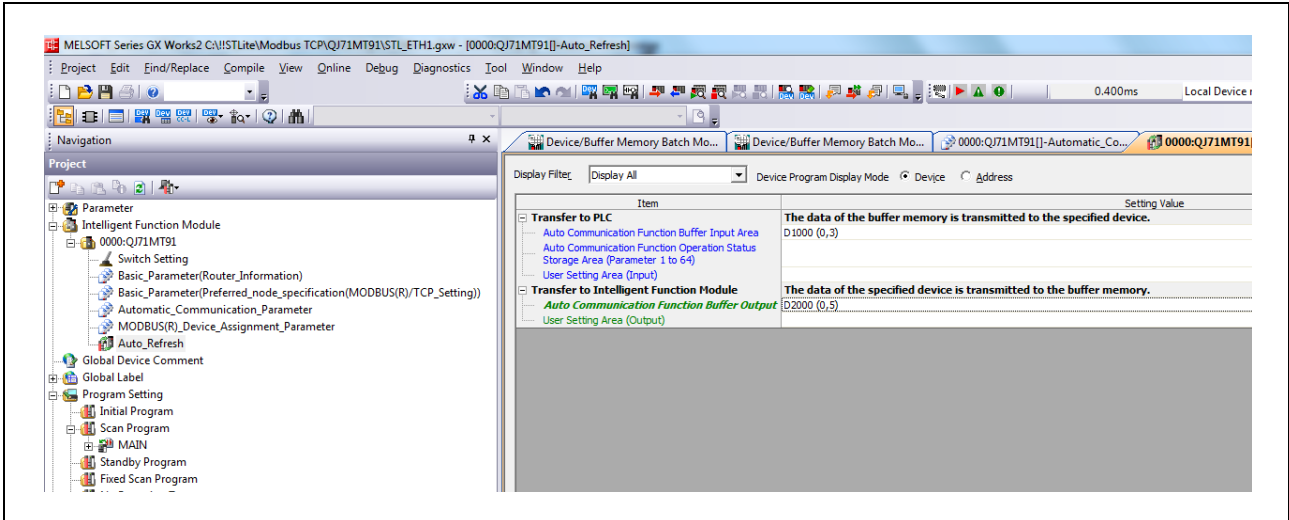


Abb. 4-13: Auto refresh settings for the QJ71MT91

### 4.3.2 Monitoring the Data Transfer

Set the host ID of the STL-ETH1 with the address selection switch (refer to section 4.2.4) according to the automatic communication parameter settings.

After connecting the Ethernet interface of the QJ71MT91 with the head station's fieldbus interface, downloading the parameters to the PLC and powering ON the system, you can monitor the data transfer in the Device Monitor of GX Works2.

#### Input data

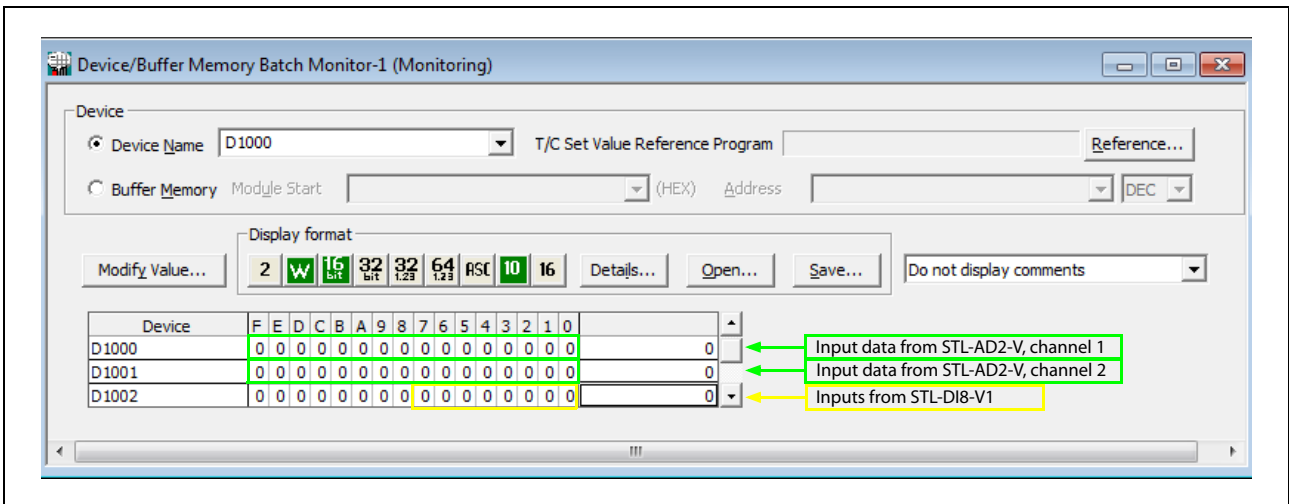
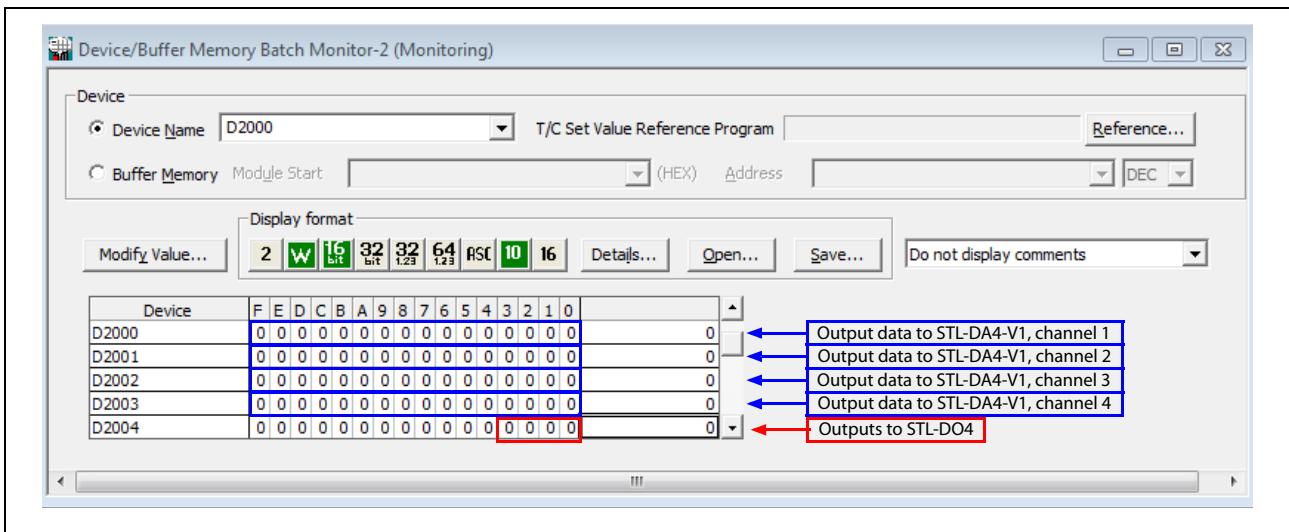


Abb. 4-14: Input data from the MODBUS/TCP node

Please note that the data from the digital input module is appended after the data from the analog input module.

For the process images of the individual STLite modules please refer to the appendix, section A.1. For example, reading a value of 16384 (4000H) from D1000 means that a voltage of 5.00 V is applied to channel 1 of the STL-AD2-V.

**Output data**



**Abb. 4-15:** Output data to the MODBUS/TCP node

Please note that the data for the digital output module is appended after the data for the analog output module.

If you want to output 10 V on channel 1 of the STL-DA4-V1, write 32760 (7FF8H) to D2000.

**4.3.3 The Web-Based Management System (WBM)**

An internal file system and an integrated Web server can be used for configuration and administration of the system. Together, they are referred to as the Web-Based Management System (WBM).

The HTML pages saved internally provide you with information about the configuration and status of the fieldbus node. In addition, you can also change the configuration of the device here.

You can also save HTML pages created yourself via the implemented file system.

**NOTE**

Always restart after making changes to the configuration!  
The system must always be restarted for the changed configuration settings to take effect.

- ① To open the WBM, launch a Web browser (e.g., Microsoft Internet Explorer or Mozilla Firefox).
- ② Enter the IP address of the fieldbus coupler/controller in the address bar (192.168.1.1 by default or as previously configured).
- ③ Click **Enter** to confirm. The start page of WBM loads.
- ④ Select the link to the desired HTML page in the left navigation bar. A query dialog appears.
- ⑤ Enter your user name and password in the query dialog (default: user = "admin", password = "user" or user = "guest", password = "guest").
- ⑥ The corresponding HTML page is loaded.
- ⑦ Make the desired settings.
- ⑧ Press **SUBMIT** to confirm your changes or press **UNDO** to discard the changes.
- ⑨ Restart the system to apply the settings.

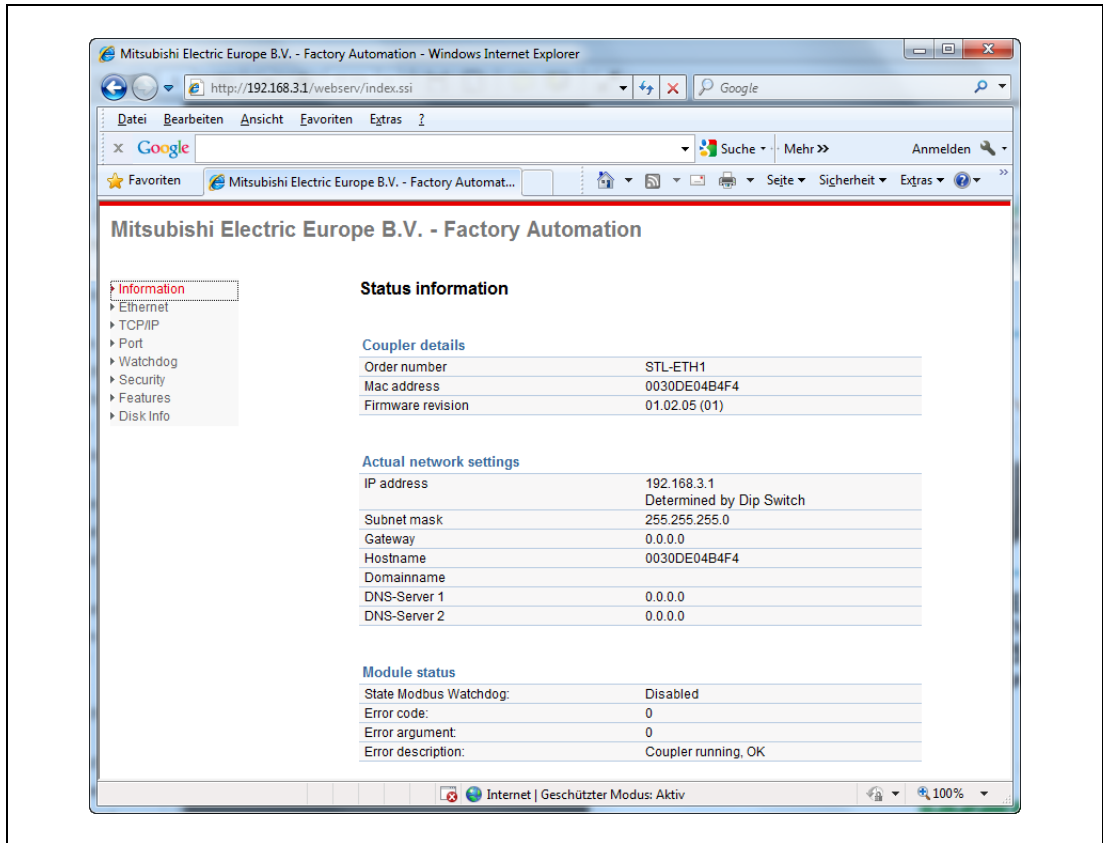


Fig. 4-16: Information screen of the Web-Based Management System

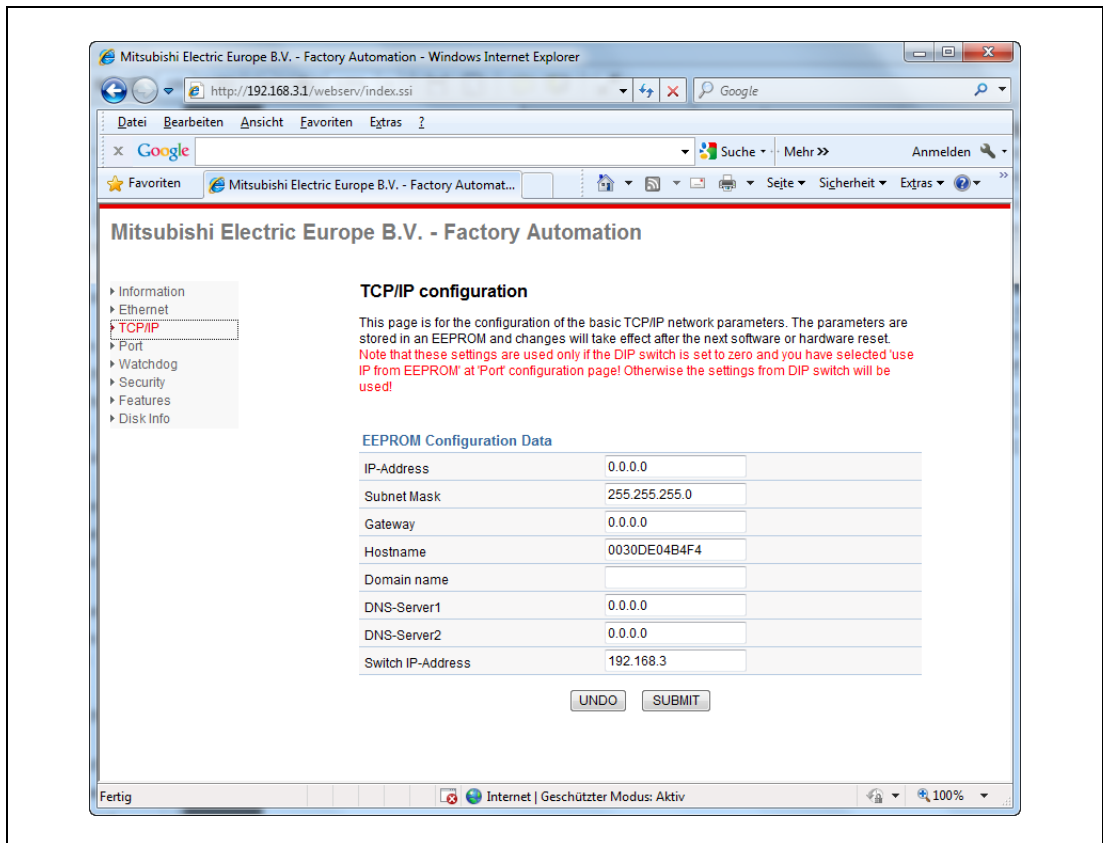


Fig. 4-17: Screen "TCP/IP" of the Web-Based Management System



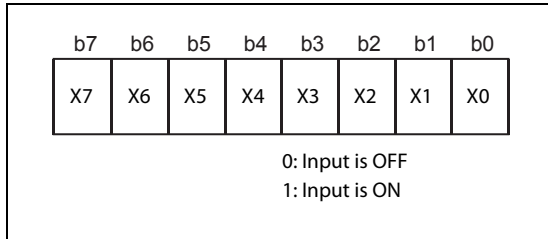


# A Appendix

## A.1 Process Images

### A.1.1 Digital Input Modules

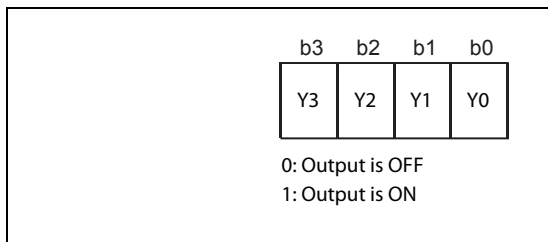
**STL-DI8-V1 (ID number 51205052) and STL-DI8-V2 (ID number 51205053)**



**Fig. A-1:**  
The signal status of the digital input modules is reflected in one byte.

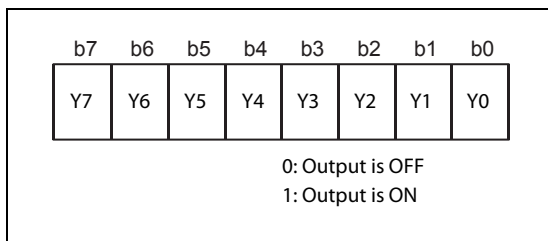
### A.1.2 Digital Output Modules

**STL-DO4 (ID number 51205045)**



**Fig. A-2:**  
Process image of the digital output module STL-DO4

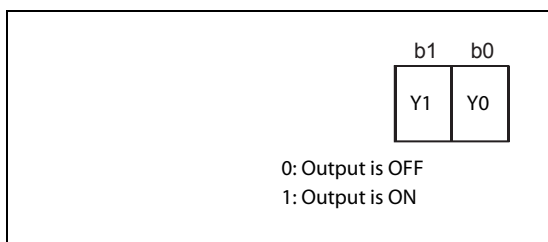
**STL-DO8 (ID number 51205043)**



**Fig. A-3:**  
Process image of the digital output module STL-DO8

### A.1.3 Relay Output Module

**STL-RO2 (ID number 51205044)**



**Fig. A-4:**  
The process image of the relay output module STL-RO2 occupies two bits

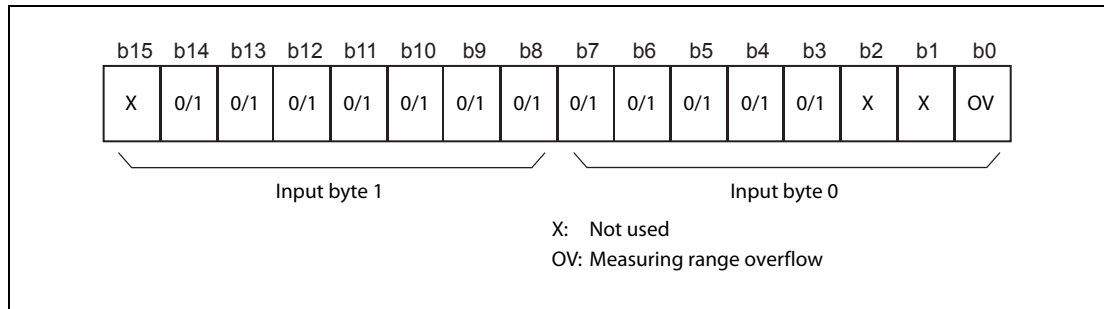
### A.1.4 Analog Input Modules

#### STL-AD2-V (ID number 51205046)

The two-channel analog input module STL-AD2-V (for voltages from 0 to 10 V) transmits a 16-bit measured value and 8 status bits per channel. Accessing the status byte depends on the fieldbus system being used.

The digitalized measured value is transmitted in a data word (16 bits) as input byte 0 (low) and input byte 1 (high) into the process image of the head station/controller.

This value is represented with a 12 bit resolution on bit b3 to b14. The least significant bit b0 is set (1) when the range of measurement is overranged.



**Fig. A-5:** Process image of the analog input module STL-AD2-V

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

| Input [V] | Numerical value |                |    |    |    |    |   |   |   |   |   |   |   |   |    |   | Hexa-decimal | Decimal | Status byte (Hex.) |
|-----------|-----------------|----------------|----|----|----|----|---|---|---|---|---|---|---|---|----|---|--------------|---------|--------------------|
|           | Binary          |                |    |    |    |    |   |   |   |   |   |   |   |   |    |   |              |         |                    |
|           | 15              | 14             | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1  | 0 |              |         |                    |
| <0.00     | X               | Measured value |    |    |    |    |   |   |   |   |   |   | X | X | OV |   |              |         |                    |
| 0.00      | 0               | 0              | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0000H        | 0       | 00H                |
| 1.25      | 0               | 0              | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 1000H        | 4096    | 00H                |
| 2.50      | 0               | 0              | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 2000H        | 8192    | 00H                |
| 3.75      | 0               | 0              | 1  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 3000H        | 12288   | 00H                |
| 5.00      | 0               | 1              | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 4000H        | 16384   | 00H                |
| 6.25      | 0               | 1              | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 5000H        | 20480   | 00H                |
| 7.50      | 0               | 1              | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 6000H        | 24576   | 00H                |
| 8.75      | 0               | 1              | 1  | 1  | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 7000H        | 28672   | 00H                |
| 10.00     | 0               | 1              | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0  | 0 | 7FF8H        | 32760   | 00H                |
| >10.00    | 0               | 1              | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1  | 1 | 7FF9H        | 32761   | 42H                |

**Tab. A-1:** Input values and corresponding process values for the STL-AD2-V

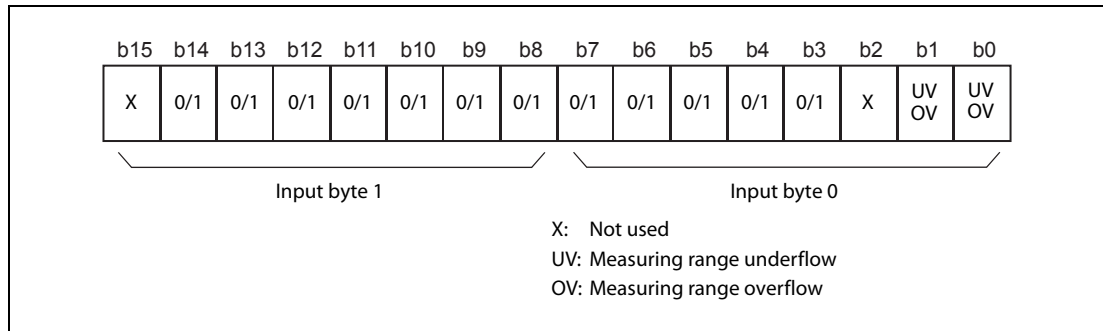
X: Not used; OV: Measuring range overflow

**STL-AD4-V1 (ID number 51205049)**

The four-channel analog input module STL-AD4-V1 (for voltages from 0 to 10 V) transmits a 16-bit measured value and 8 status bits per channel. Accessing the status byte depends on the fieldbus system being used.

The digitalized measured value is transmitted in a data word (16 bits) as input byte 0 (low) and input byte 1 (high) into the process image of the head station/controller.

This value is represented with a 12 bit resolution on bit b3 to b14. Both bits b0 and b1 are set in case of measurement range overflow or underflow.



**Fig. A-6:** Process image of the analog input module STL-AD4-V1

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

| Input [V] | Numerical value |                |    |    |    |    |   |   |   |   |   |   |   |   |       |   |              | Status byte (Hex.) |         |
|-----------|-----------------|----------------|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|--------------|--------------------|---------|
|           | Binary          |                |    |    |    |    |   |   |   |   |   |   |   |   |       |   |              |                    |         |
|           | 15              | 14             | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 | Hexa-decimal |                    | Decimal |
|           | X               | Measured value |    |    |    |    |   |   |   |   |   |   |   | X | UV/OV |   |              |                    |         |
| <0        | 0               | 0              | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1     | 1 | 0003H        | 3                  | 41H*    |
| 0         | 0               | 0              | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 0 | 0000H        | 0                  | 00H     |
| 1         | 0               | 0              | 0  | 1  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | X | 0     | 0 | 0CCCH        | 3276               | 00H     |
| 2         | 0               | 0              | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0     | 0 | 1998H        | 6552               | 00H     |
| 3         | 0               | 0              | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | X | 0     | 0 | 2664H        | 9828               | 00H     |
| 4         | 0               | 0              | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0     | 0 | 3330H        | 13104              | 00H     |
| 5         | 0               | 1              | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 0 | 4000H        | 16384              | 00H     |
| 6         | 0               | 1              | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | 0     | 0 | 4CCCH        | 19660              | 00H     |
| 7         | 0               | 1              | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0     | 0 | 5998H        | 22936              | 00H     |
| 8         | 0               | 1              | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0     | 0 | 6660H        | 26208              | 00H     |
| 9         | 0               | 1              | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0     | 0 | 7330H        | 29488              | 00H     |
| 10.00     | 0               | 1              | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 0     | 0 | 7FFCH        | 32764              | 00H     |
| >10.00    | 0               | 1              | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 1     | 1 | 7FFFH        | 32767              | 42H*    |

**Tab. A-2:** Input values and corresponding process values for the STL-AD4-V1

X: Not used; UV: Measuring range underflow, OV: Measuring range overflow

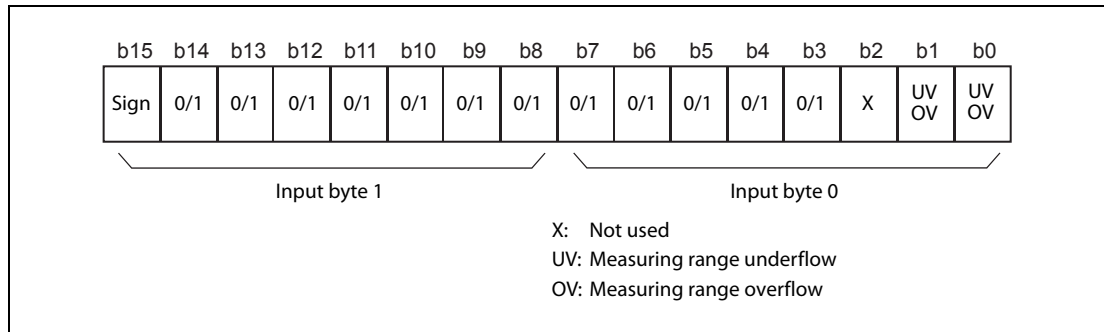
\* In this cases the ERROR-LED of the corresponding channel is lit.

**STL-AD4-V2 (ID number 51205050)**

The four-channel analog input module STL-AD4-V2 (for voltages from -10 V to 10 V) transmits a 16-bit measured value and 8 status bits per channel. Accessing the status byte depends on the fieldbus system being used.

The digitalized measured value is transmitted in a data word (16 bits) as input byte 0 (low) and input byte 1 (high) into the process image of the head station/controller.

This value is represented with a 12 bit resolution on bit b3 to b14. Bit b15 is set when the measured value is negative. Both bits b0 and b1 are set in case of measurement range overflow or underflow.



**Fig. A-7:** Process image of the analog input module STL-AD4-V2

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

| Input [V] | Numerical value |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |              | Status byte (Hex.) |         |
|-----------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|--------------|--------------------|---------|
|           | Binary          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       | Hexa-decimal |                    | Decimal |
|           | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |              |                    |         |
|           | Measured value  |    |    |    |    |    |   |   |   |   |   |   |   |   | X | UV/OV |              |                    |         |
| <-10      | 1               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1     | 8003H        | -32765             | 41H*    |
| -10       | 1               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 8000H        | -32768             | 00H     |
| -8        | 1               | 0  | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0     | 9998H        | -26214             | 00H     |
| -6        | 1               | 0  | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | X | 0 | 0     | B334H        | -19660             | 00H     |
| -4        | 1               | 1  | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | 0 | 0     | CCCCH        | -13107             | 00H     |
| -2        | 1               | 1  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | X | 0 | 0     | E664H        | -6552              | 00H     |
| 0         | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 0000H        | 0                  | 00H     |
| 2         | 0               | 0  | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0     | 1998H        | 6552               | 00H     |
| 4         | 0               | 0  | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0     | 3330H        | 13104              | 00H     |
| 6         | 0               | 1  | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | 0 | 0     | 4CCCH        | 19660              | 00H     |
| 8         | 0               | 1  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0     | 6660H        | 26208              | 00H     |
| 10        | 0               | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 0 | 0     | 7FFCH        | 32764              | 00H     |
| >10       | 0               | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | X | 1 | 1     | 7FFFH        | 32767              | 42H*    |

**Tab. A-3:** Input values and corresponding process values for the STL-AD4-V2

X: Not used; UV: Measuring range underflow, OV: Measuring range overflow

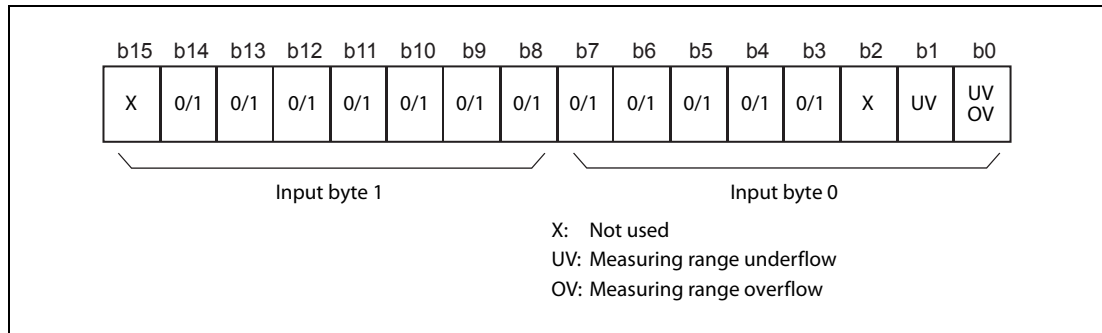
\* In this cases the ERROR-LED of the corresponding channel is lit.

**STL-AD2-I (ID number 51205047)**

The two-channel analog input module STL-AD2-I (for currents from 4 to 20 mA) transmits a 16-bit measured value and 8 status bits per channel. Accessing the status byte depends on the fieldbus system being used.

The digitalized measured value is transmitted in a data word (16 bits) as input byte 0 (low) and input byte 1 (high) into the process image of the head station/controller.

This value is represented with a 12 bit resolution on bit b3 to b14. The least significant bit b0 is set (1) when the range of measurement is overranged. Both bits b0 and b1 are set in case of measurement range underflow or broken wire.



**Fig. A-8:** Process image of the analog input module STL-AD2-I

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

| Input [mA] | Numerical value                           |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Hexa-decimal | Decimal | Status byte (Hex.) |
|------------|---|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------------|---------|--------------------|
|            | Binary                                    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |              |         |                    |
|            | 15  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |              |         |                    |
| <0         | Not possible (Reverse voltage protection) |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |              |         |                    |
| 2 to 3.9   | 0   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0003H        | 3       | 41H*               |
| <4         | 0   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000H        | 0       | 00H                |
| 4          | 0   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000H        | 0       | 00H                |
| 6          | 0   | 0  | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000H        | 4096    | 00H                |
| 8          | 0   | 0  | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2000H        | 8192    | 00H                |
| 10         | 0   | 0  | 1  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3000H        | 12288   | 00H                |
| 12         | 0   | 1  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4000H        | 16384   | 00H                |
| 14         | 0   | 1  | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5000H        | 20480   | 00H                |
| 16         | 0   | 1  | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 6000H        | 24576   | 00H                |
| 18         | 0   | 1  | 1  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7000H        | 28672   | 00H                |
| 20         | 0   | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 7FF8H        | 32760   | 00H                |
| >20        | 0   | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 7FF9H        | 32761   | 42H                |
| 20.1 to 22 | 0   | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 7FF9H        | 32761   | 42H*               |

**Tab. A-4:** Input values and corresponding process values for the STL-AD2-I

X: Not used; UV: Measuring range underflow, OV: Measuring range overflow

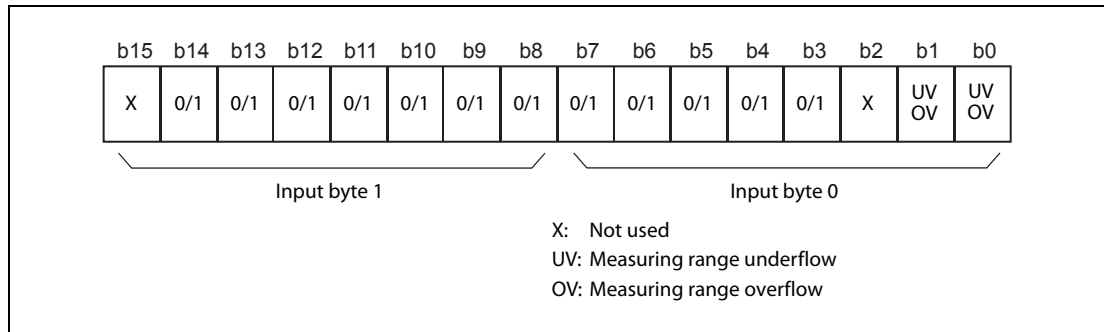
\* In this cases the ERROR-LED of the corresponding channel is lit.

**STL-AD4-I (ID number 51205051)**

The four-channel analog input module STL-AD4-I (for currents from 4 to 20 mA) transmits a 16-bit measured value and 8 status bits per channel. Accessing the status byte depends on the fieldbus system being used.

The digitalized measured value is transmitted in a data word (16 bits) as input byte 0 (low) and input byte 1 (high) into the process image of the head station/controller.

This value is represented with a 12 bit resolution on bit b3 to b14. Both bits b0 and b1 are set in case of measurement range underflow, overflow or broken wire.



**Fig. A-9:** Process image of the analog input module STL-AD4-I

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

| Input [mA] | Numerical value |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |              | Status byte (Hex.) |         |
|------------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|--------------|--------------------|---------|
|            | Binary          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       | Hexa-decimal |                    | Decimal |
|            | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |              |                    |         |
|            | Measured value  |    |    |    |    |    |   |   |   |   |   |   |   |   | X | UV/OV |              |                    |         |
| <4.0       | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1     | 0003H        | 3                  | 41H*    |
| 4.0        | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 0000H        | 0                  | 00H     |
| 5.6        | 0               | 0  | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | 0 | 0     | 0CCCH        | 3276               | 00H     |
| 7.2        | 0               | 0  | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0     | 1998H        | 6552               | 00H     |
| 8.8        | 0               | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | X | 0 | 0     | 2664H        | 9828               | 00H     |
| 10.4       | 0               | 0  | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0     | 3330H        | 13104              | 00H     |
| 12.0       | 0               | 1  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 4000H        | 16384              | 00H     |
| 13.6       | 0               | 1  | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | X | 0 | 0     | 4CCCH        | 19660              | 00H     |
| 15.2       | 0               | 1  | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0     | 5998H        | 22936              | 00H     |
| 16.8       | 0               | 1  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0     | 6660H        | 26208              | 00H     |
| 18.4       | 0               | 1  | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0     | 7330H        | 29488              | 00H     |
| 20         | 0               | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0     | 7FF8H        | 32760              | 00H     |
| >20        | 0               | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1     | 7FBH         | 32761              | 42H*    |

**Tab. A-5:** Input values and corresponding process values for the STL-AD4-I

X: Not used; UV: Measuring range underflow, OV: Measuring range overflow

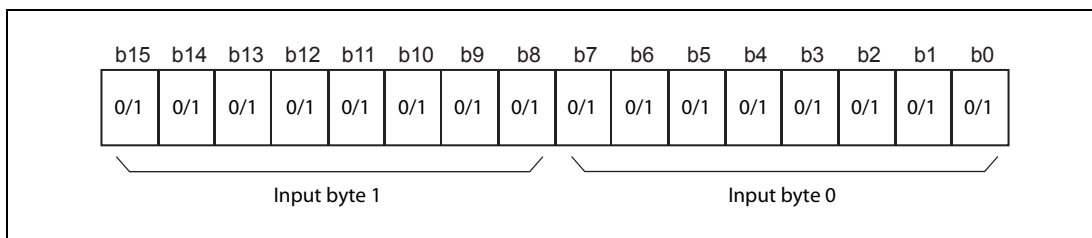
\* In this cases the ERROR-LED of the corresponding channel is lit.

**STL-TI2 (ID number 51205048)**

The two-channel analog input module STL-TI2 for temperature acquisition transmits 16-bit measured values per channel as well as 8 optional status bits to the head station. Accessing the status byte depends on the fieldbus system being used.

To evaluate the platinum resistance sensors the measured values of the resistance are converted and sent as temperature values. All temperature values are represented in a standard numeric format.

The possible numerical range matches the defined temperature range of the Pt100 sensors from -200 °C to +850 °C. The temperature values of the sensors are represented with a resolution of 1 digit per 0.1 °C within a word (16 bits). Thus, 0.0 °C corresponds to the numeric value 0000H and 100.0 °C to 03E8H (decimal 1000). Temperature values below 0 °C are represented in two's complement binary form.



**Fig. A-10:** Process image of analog module STL-TI2 for temperature acquisition

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

| Temperature [°C]                   | Resistance [Ω] | Numerical value |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       | Hexa-decimal | Decimal | Status byte (Hex.) |
|------------------------------------|----------------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|--------------|---------|--------------------|
|                                    |                | Binary          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |              |         |                    |
|                                    |                | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |              |         |                    |
| <-200.0                            | 10.00          | 1               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 8001H | -32767       | 41H*    |                    |
| -200.0                             | 18.49          | 1               | 1  | 1  | 1  | 1  | 0  | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | F830H | -2000        | 00H     |                    |
| -100.0                             | 60.25          | 1               | 1  | 1  | 1  | 1  | 1  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | FC18H | -1000        | 00H     |                    |
| 0.0                                | 100.00         | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000H | 0            | 00H     |                    |
| 100.0                              | 138.50         | 0               | 0  | 0  | 0  | 0  | 0  | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 03E8H | 1000         | 00H     |                    |
| 200.0                              | 175.84         | 0               | 0  | 0  | 0  | 0  | 1  | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 07D0H | 2000         | 00H     |                    |
| 500.0                              | 280.90         | 0               | 0  | 0  | 1  | 0  | 0  | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1388H | 5000         | 00H     |                    |
| 750.0                              | 360.47         | 0               | 0  | 0  | 1  | 1  | 1  | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1D4CH | 7500         | 00H     |                    |
| 800.0                              | 375.51         | 0               | 0  | 0  | 1  | 1  | 1  | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1F40H | 8000         | 00H     |                    |
| 850.0                              | 390.26         | 0               | 0  | 1  | 0  | 0  | 0  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 2134H | 8500         | 00H     |                    |
| >850.0                             | >390.26        | 0               | 0  | 1  | 0  | 0  | 0  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |       |              | 42H*    |                    |
| Broken wire against R <sub>L</sub> |                | 0               | 0  | 1  | 0  | 0  | 0  | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |       |              | 42H*    |                    |

**Tab. A-6:** Input values and corresponding process values for the STL-TI2

\* In this cases the red ERROR-LED of the corresponding channel is lit.

**NOTE**

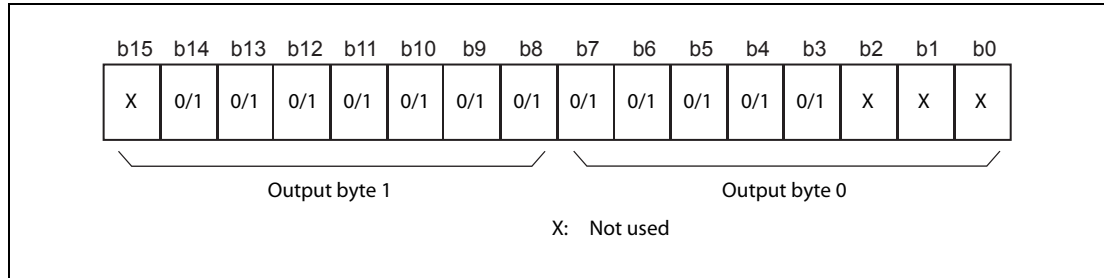
The measured value can exceed the range from decimal -2000 to 8500 until the limitation applies.

### A.1.5 Analog Output Modules

#### STL-DA2-V (ID number 51205042) and STL-DA4-V1 (ID number 51205038)

The analog output modules STL-DA2-V (two channels, 0 to 10 V) and STL-DA4-V1 (four channels, 0 to 10 V) require 16-bit data and 8 status bits per channel.

The digitalized output value is transmitted in a data word (16 bits) as output byte 0 (low) and output byte 1 (high) via the process image of the head station. This value is represented with a 12 bit resolution on the bits b3 to b14. The three least significant bits (b0 to b2) are not parsed.



**Fig. A-11:** Process image of the analog output modules STL-DA2-V and STL-DA4-V1

Some fieldbus systems can process status information by means of a status byte. As the returned status byte of this output module is always zero, it will not be parsed.

| Output [V] | Numerical value |              |    |    |    |    |   |   |   |   |   |   |   |   |   |              |         | Hexa-decimal | Decimal | Status byte (Hex.) |     |
|------------|-----------------|--------------|----|----|----|----|---|---|---|---|---|---|---|---|---|--------------|---------|--------------|---------|--------------------|-----|
|            | Binary          |              |    |    |    |    |   |   |   |   |   |   |   |   |   | Hexa-decimal | Decimal |              |         |                    |     |
|            | 15              | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |              |         |              |         |                    | 0   |
| 0.00       | X               | Output value |    |    |    |    |   |   |   |   |   |   |   |   |   | X            | X       | X            | 0000H   | 0                  | 00H |
| 1.25       | 0               | 0            | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 1000H   | 4096         | 00H     |                    |     |
| 2.50       | 0               | 0            | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 2000H   | 8192         | 00H     |                    |     |
| 3.75       | 0               | 0            | 1  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 3000H   | 12288        | 00H     |                    |     |
| 5.00       | 0               | 1            | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 4000H   | 16384        | 00H     |                    |     |
| 6.25       | 0               | 1            | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 5000H   | 20480        | 00H     |                    |     |
| 7.50       | 0               | 1            | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 6000H   | 24576        | 00H     |                    |     |
| 8.75       | 0               | 1            | 1  | 1  | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 7000H   | 28672        | 00H     |                    |     |
| 10.00      | 0               | 1            | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0            | 7FF8H   | 32760        | 00H     |                    |     |

**Tab. A-7:** Process values and corresponding output values for the STL-DA2-V and STL-DA4-V1

X: Not relevant



**STL-DA4-V2 (ID number 51205039)**

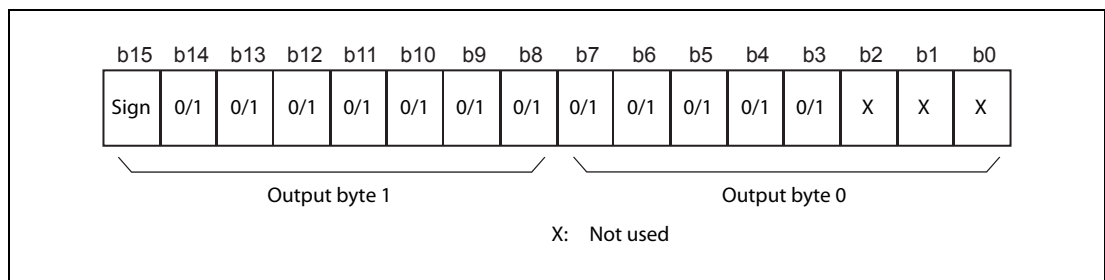
The analog output module STL-DA4-V2 (four channels, -10 to 10 V) requires 16-bit data and 8 status bits per channel.

The digitalized output value is transmitted in a data word (16 bits) as output byte 0 (low) and output byte 1 (high) via the process image of the head station. This value is represented with a 12 bit resolution on the bits b3 to b14. Bit b15 serves as sign bit. The three least significant bits (b0 to b2) are not parsed.

Negative voltages are output when the output value is specified in two's complement binary form.

**NOTE**

Although the bits b0 to b2 are not relevant, they can be used for the ease of programming (see table below). The resulting output error will only be marginal.



**Fig. A-12:** Process image of the analog output module STL-DA4-V2

Some fieldbus systems can process status information by means of a status byte. As the returned status byte of this output module is always zero, it will not be parsed.

| Output [V] | Numerical value |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       | Hexa-decimal | Decimal | Status byte (Hex.) |
|------------|-----------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|--------------|---------|--------------------|
|            | Binary          |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |              |         |                    |
|            | 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |              |         |                    |
|            | Output value    |    |    |    |    |    |   |   |   |   |   |   |   | X | X | X     |              |         |                    |
| -10        | 1               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1     | 8001H        | -32767  | 00H                |
| -8         | 1               | 0  | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0     | 999AH        | -26214  | 00H                |
| -6         | 1               | 0  | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0     | B334H        | -19660  | 00H                |
| -4         | 1               | 1  | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1     | CCCDH        | -13107  | 00H                |
| -2         | 1               | 1  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1     | E667H        | -6552   | 00H                |
| 0          | 0               | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     | 0000H        | 0       | 00H                |
| 2          | 0               | 0  | 0  | 1  | 1  | 0  | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1     | 1999H        | 6553    | 00H                |
| 4          | 0               | 0  | 1  | 1  | 0  | 0  | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1     | 3333H        | 13107   | 00H                |
| 6          | 0               | 1  | 0  | 0  | 1  | 1  | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0     | 4CCCH        | 19660   | 00H                |
| 8          | 0               | 1  | 1  | 0  | 0  | 1  | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0     | 6666H        | 26214   | 00H                |
| 10         | 0               | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 7FFCH | 32767        | 00H     |                    |

**Tab. A-8:** Process values and corresponding output values for the STL-DA4-V2

X: Not relevant

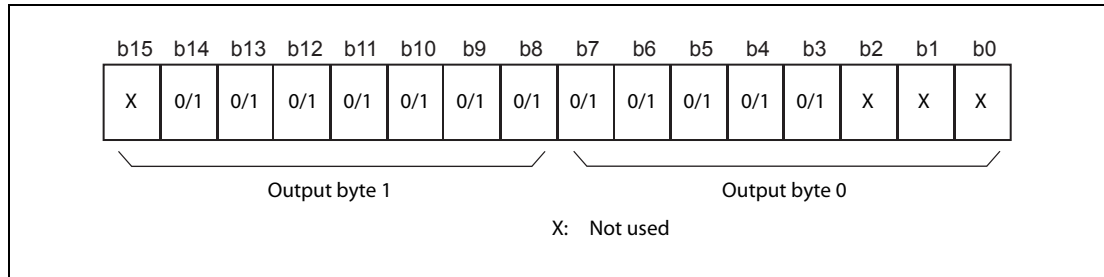
**STL-DA2-I (ID number 51205041)**

The analog output module STL-DA2-I (two channels, 4 to 20 mA) requires 16-bit data and 8 status bits per channel.

The digitalized output value is transmitted in a data word (16 bits) as output byte 0 (low) and output byte 1 (high) via the process image of the head station. This value is represented with a 12 bit resolution on the bits b3 to b14. The three least significant bits (b0 to b2) are not parsed.

**NOTE**

Although the bits b0 to b2 are not relevant, they can be used for the ease of programming (see table below). The resulting output error will only be marginal.



**Fig. A-13:** Process image of the analog output module STL-DA2-I

Some fieldbus systems can process status information by means of a status byte. As the returned status byte of this output module is always zero, it will not be parsed.

| Output [mA] | Numerical value |              |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       | Hexa-decimal | Decimal | Status byte (Hex.) |
|-------------|-----------------|--------------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|--------------|---------|--------------------|
|             | Binary          |              |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |              |         |                    |
|             | 15              | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |              |         |                    |
|             | X               | Output value |    |    |    |    |   |   |   |   |   |   |   |   | X | X | X     |              |         |                    |
| 4           | 0               | 0            | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000H | 0            | 00H     |                    |
| 6           | 0               | 0            | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000H | 4096         | 00H     |                    |
| 8           | 0               | 0            | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 2000H | 8192         | 00H     |                    |
| 10          | 0               | 0            | 1  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3000H | 12288        | 00H     |                    |
| 12          | 0               | 1            | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4000H | 16384        | 00H     |                    |
| 14          | 0               | 1            | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 5000H | 20480        | 00H     |                    |
| 16          | 0               | 1            | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 6000H | 24576        | 00H     |                    |
| 18          | 0               | 1            | 1  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7000H | 28672        | 00H     |                    |
| 20          | 0               | 1            | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7FFFH | 32767        | 00H     |                    |

**Tab. A-9:** Process values and corresponding output values for the STL-DA2-I

X: Not relevant

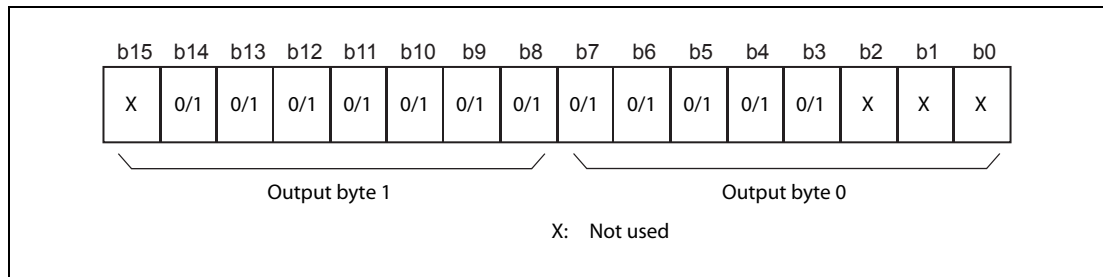
**STL-DA4-I (ID number 51205040)**

The analog output module STL-DA4-I (four channels, 4 to 20 mA) requires 16-bit data and 8 status bits per channel.

The digitalized output value is transmitted in a data word (16 bits) as output byte 0 (low) and output byte 1 (high) via the process image of the head station. This value is represented with a 12 bit resolution on the bits b3 to b14. The three least significant bits (b0 to b2) are not parsed.

**NOTE**

Although the bits b0 to b2 are not relevant, they can be used for the ease of programming (see table below). The resulting output error will only be marginal.



**Fig. A-14:** Process image of the analog output module STL-DA4-I

Some fieldbus systems can process the status information using by means of a status byte. However, processing of the status byte via the head station is optional, which means that accessing or parsing the status information depends on the fieldbus system.

| Output [mA] | Numerical value |              |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       | Hexa-decimal | Decimal | Status byte (Hex.) |
|-------------|-----------------|--------------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|--------------|---------|--------------------|
|             | Binary          |              |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |              |         |                    |
|             | 15              | 14           | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |              |         |                    |
|             | X               | Output value |    |    |    |    |   |   |   |   |   |   |   | X | X | X |       |              |         |                    |
| 4           | 0               | 0            | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000H | 0            | 00H     |                    |
| 8           | 0               | 0            | 0  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FFFH | 8191         | 00H     |                    |
| 12          | 0               | 0            | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3FFFH | 16383        | 00H     |                    |
| 16          | 0               | 1            | 0  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 5FFFH | 24575        | 00H     |                    |
| 20          | 0               | 1            | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 7FFFH | 32767        | 00H     |                    |
| Error ①     | Undefined       |              |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |              |         | 40H ②              |

**Tab. A-10:** Process values and corresponding output values for the STL-DA4-I

X: Not relevant

- ① Broken wire or inadmissible load combination
- ② The ERROR-LED will also be ON.

### A.1.6 Encoder module STL-ENC (ID number 51205116)

Using the encoder module STL-ENC, a 6 byte input and output process image can be transferred to the head station via two logical channels.

The set values are stored in four output bytes (D0 to D3) and the process data are stored in four input bytes (D0 to D3). Two control bytes (C0, C1) and two status bytes (S0, S1) are used to select process data and set values as well as to control the data flow.

| Input data |                            | Output data |                         |
|------------|----------------------------|-------------|-------------------------|
| S0         | Status byte S0             | C0          | Control byte C0         |
| D0         | Process data, byte 0 (LSB) | D0          | Set value, byte 0 (LSB) |
| D1         | Process data, byte 1       | D1          | Set value, byte 1       |
| S1         | Status byte S1             | C1          | Control byte C1         |
| D2         | Process data, byte 2       | D2          | Set value, byte 2       |
| D3         | Process data, byte 3 (MSB) | D3          | Set value, byte 3 (MSB) |

**Tab. A-11:** Input and output bytes of the STL-ENC

#### NOTE

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

The process data is determined by the bits 0 and 1 in the control byte C1:

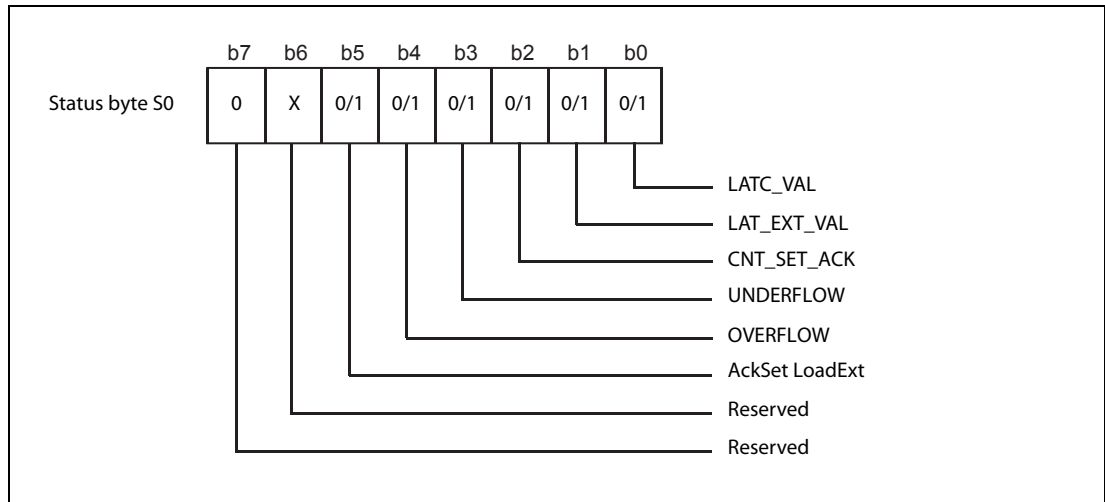
- Counter value
- Latch value
- Velocity
- Set value

The setting is mirrored in status byte S1 in bit 0 and bit 1.

| MapPZD (Control Byte C1 / Status Byte S1, bits 0 and 1) |       |  |
|---|-------|--|
| Bit 1   | Bit 0 | Coding of the process data             |
| 0   | 0     | Counter value                          |
| 0   | 1     | Latch value                            |
| 1   | 0     | Velocity (increments per milliseconds) |
| 1   | 1     | Set value                              |

**Tab. A-12:** Meaning of the bits 1 and 0 in C1/S1

**Status byte S0**

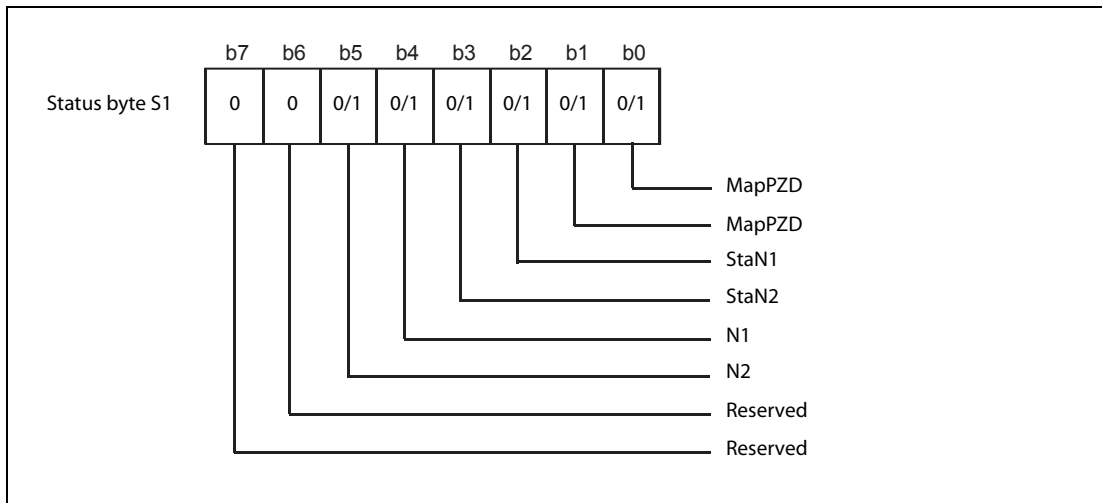


**Fig. A-15:** Status byte S0 of the STL-ENC

| Bit | Name           | Description  |
|-----|----------------|--|
| 0   | LATC_VAL       | Acknowledge bit for EN_LATC (control byte C0, bit 0)<br><ul style="list-style-type: none"> <li>Latch Mode:<br/>This bit is set with a positive edge at input C. It is reset when EN_LATC is reset.</li> <li>Preload Mode:<br/>This bit is set with a positive edge at C. It is reset when EN_LATC is reset.</li> </ul>                                 |
| 1   | LAT_EXT_VAL    | Acknowledge bit for EN_LAT_EXT (control byte C0, bit 1).<br><ul style="list-style-type: none"> <li>Latch Mode:<br/>This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset.</li> <li>Preload Mode:<br/>This bit is set with a positive edge at the input Latch. It is reset when EN_LAT_EXT is reset.</li> </ul> |
| 2   | CNT_SET_ACK    | Acknowledge bit for CNT_SET (control byte C0, bit 2).<br>Reset if CNT_SET = 0  |
| 3   | UNDERFLOW      | This bit is set (1) with a counter underflow of 00000000H to FFFFFFFFH.<br>This bit is reset (0)<br>– if counter < AAAAAAAH<br>– with the positive edge of ResetUnderflow (control byte C0, bit 3)<br>– if OVERFLOW = 1  |
| 4   | OVERFLOW       | This bit is set (1) with a counter overflow of FFFFFFFFH to 00000000H.<br>This bit is reset (0)<br>– if counter > 55555555H<br>– with the positive edge of ResetOverflow (control byte C0, bit 4)<br>– if UNDERFLOW = 1  |
| 5   | AckSet LoadExt | Acknowledge bit for SetLoadExt.<br>Reset if SetLoadExt = 0 (control byte C0, bit 5)  |

**Tab. A-13:** Description of the status byte S0 of the STL-ENC

**Status byte S1**

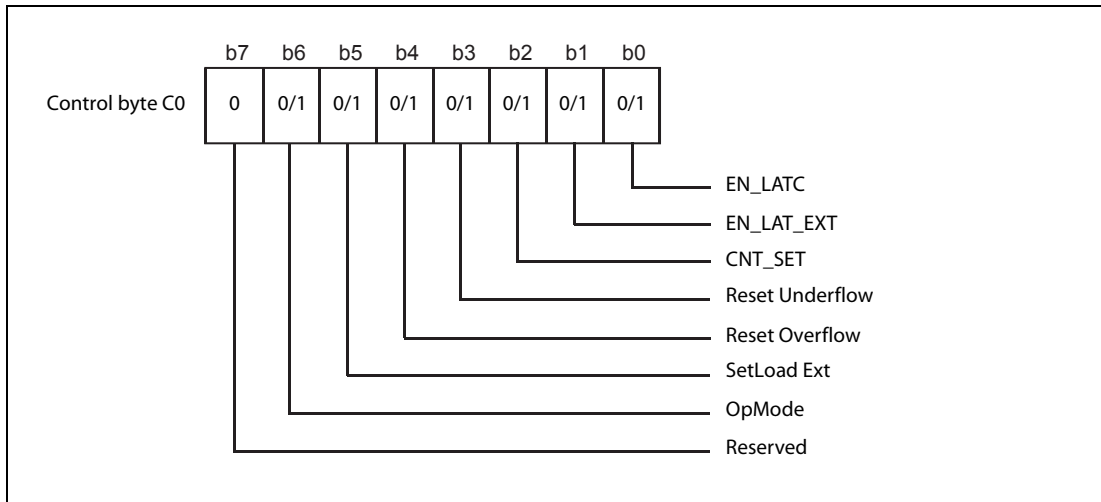


**Fig. A-16:** Status byte S1 of the STL-ENC

| Bit | Name   | Description  |
|-----|--------|--|
| 0   | MapPZD | • Software version < XXXX03XX: reserved / not used (0)   |
| 1   |        | • Software version ≥ XXXX03XX: coding of process data (2 Bits), refer to table A-12  |
| 2   | StaN1  | • Software version < XXXX03XX: reserved / not used (0)<br>• Software version ≥ XXXX03XX: state of cam output 1<br>0 = cam output 1 reset<br>1 = cam output 1 set |
| 3   | StaN2  | • Software version < XXXX03XX: reserved / not used (0)<br>• Software version ≥ XXXX03XX: state of cam output 2<br>0 = cam output 2 reset<br>1 = cam output 2 set |
| 4   | N1     | Cam window 1st bit<br>This bit is set, if:<br>bottom comparative value N1 ≤ counter reading ≤ top comparative value N1   |
| 5   | N2     | Cam window 2nd bit<br>This bit is set, if:<br>bottom comparative value N2 ≤ counter reading ≤ top comparative value N2   |

**Tab. A-14:** Description of the status byte S1 of the STL-ENC

**Control byte C0**

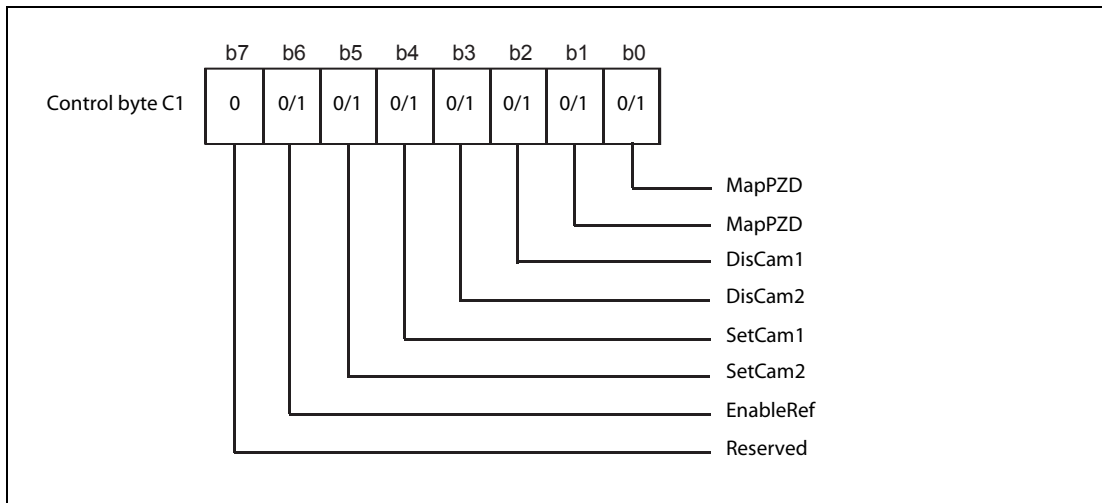


**Fig. A-17:** Control byte C0 of the STL-ENC

| Bit | Name            | Description   |
|-----|-----------------|---|
| 0   | EN_LATC         | The encoder zero mark is released.<br><ul style="list-style-type: none"> <li>• Capture Mode:<br/>With a positive edge at input C the counter reading is transferred to the latch register.</li> <li>• Preload Mode:<br/>With a positive edge at input C the counter reading is transferred to the latch register. The counter is loaded with the set value.</li> </ul> The confirmation is de-selected for the negative edge of EN_LATC.<br>EN_LATC is dominant against EN_LAT_EXT. |
| 1   | EN_LAT_EXT      | The external latch input is released.<br><ul style="list-style-type: none"> <li>• Capture Mode:<br/>With a positive edge at the input LATCH, the counter reading is transferred to the latch register.</li> <li>• Preload Mode:<br/>With a positive edge at the input LATCH, the counter reading is transferred to the Latch register. The counter is loaded with the set value.</li> </ul> The confirmation is de-selected for the negative edge of EN_LAT_EXT.                    |
| 2   | CNT_SET         | With a positive edge of this bit the counter is initialized on the set value.   |
| 3   | Reset Underflow | With a positive edge of this bit the status bit UNDERFLOW (status byte 0, bit 3) is reset.  |
| 4   | Reset Overflow  | With a positive edge of this bit the status bit OVERFLOW (status byte 0, bit 4) is reset.   |
| 5   | SetLoad Ext     | With a positive edge of this bit, the set value to which the counter is to be set in the case of an external event, will be transferred to the process data.  |
| 6   | OpMode          | 0 = Capture Mode (The counter is latched by a trigger signal.)<br>1 = Preload Mode (The counter is latched by a trigger signal. Subsequently, the counter is loaded with the set value.)  |

**Tab. A-15:** Description of the control byte C0 of the STL-ENC

**Control byte C1**



**Fig. A-18:** Control byte C1 of the STL-ENC

| Bit | Name      | Description  |
|-----|-----------|--|
| 0   | MapPZD    | Coding of process data (2 Bits), please refer to table A-12  |
| 1   |           |  |
| 2   | DisCam1   | <ul style="list-style-type: none"> <li>Software version &lt; XXXX03XX: reserved / not used (0)</li> <li>Software version ≥ XXXX03XX: disable cam output 1<br/>0 = cam output 1 enabled<br/>1 = cam output 1 disabled</li> </ul>  |
| 3   | DisCam2   | <ul style="list-style-type: none"> <li>Software version &lt; XXXX03XX: reserved / not used (0)</li> <li>Software version ≥ XXXX03XX: disable cam output 2<br/>0 = cam output 2 enabled<br/>1 = cam output 2 disabled</li> </ul>  |
| 4   | SetCam1   | <ul style="list-style-type: none"> <li>With a positive edge, the set value is taken over as the bottom comparative value for output 1 (N1).</li> <li>With a negative edge, the set value is taken over as the top comparative value for output 1 (N1).</li> </ul>  |
| 5   | SetCam2   | <ul style="list-style-type: none"> <li>With a positive edge, the set value is taken over as the bottom comparative value for output 2 (N2).</li> <li>With a negative edge, the set value is taken over as the top comparative value for output 2 (N2).</li> </ul>  |
| 6   | EnableRef | Input REF released. <ul style="list-style-type: none"> <li>The controls set Bit EnableRef.</li> <li>The controls must release EN_LATC (control byte C0, bit 0) or EN_LAT_EXT (control byte C0, bit 1) with a positive edge.</li> <li>A positive edge is created at input REF.</li> <li>Subsequently, the next positive edge at input C or input Latch leads to a Capture or Preload event</li> </ul> |

**Tab. A-16:** Description of the control byte C1 of the STL-ENC



### A.1.7 Counter module STL-C100 (ID number 51244881)

Using the counter module STL-C100, a 5 byte input and output process image can be transferred to the head station via two logical channels.

The transfer of the setting counter value in binary format is made via 4 output bytes (D0 to D3) and the transfer of the counter reading in binary format is made via 4 input bytes (D0 to D3). The control byte C0 serves for setting the counter and the outputs. The status byte S0 shows the status of the counter and the inputs and outputs.

| Input data |                             | Output data |                         |
|------------|-----------------------------|-------------|-------------------------|
| S0         | Status byte S0              | C0          | Control byte C0         |
| D0         | Counter value, byte 0 (LSB) | D0          | Set value, byte 0 (LSB) |
| D1         | Counter value, byte 1       | D1          | Set value, byte 1       |
| D2         | Counter value, byte 2       | D2          | Set value, byte 2       |
| D3         | Counter value, byte 3 (MSB) | D3          | Set value, byte 3 (MSB) |

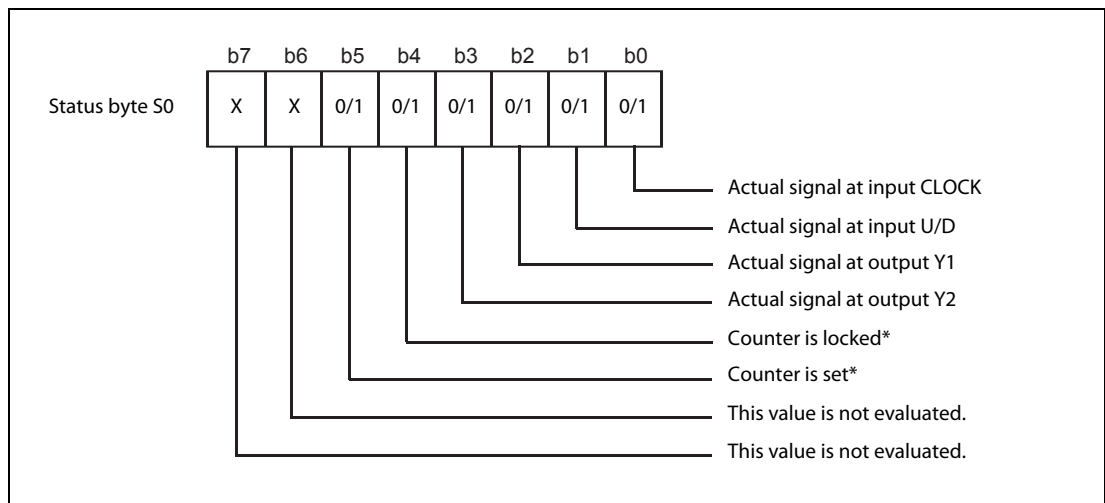
**Tab. A-17:** Input and output bytes of the STL-C100

**NOTE**

The representation of the process data of some I/O modules in the process image depends on the fieldbus head station used.

Please take this information as well as the particular design of the respective control/status bytes included in the description concerning the process image of the corresponding head station.

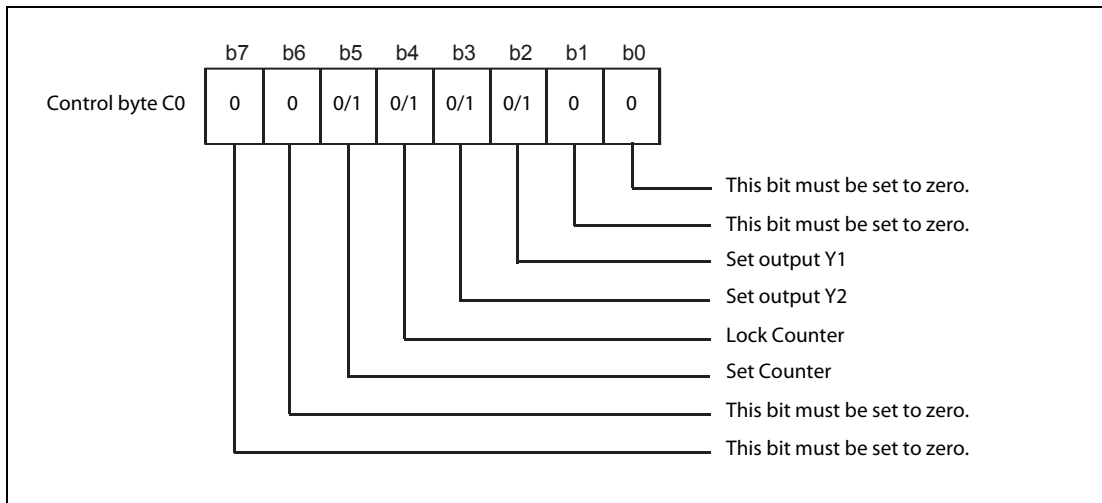
#### Status byte S0



**Fig. A-19:** Status byte S0 of the STL-C100

\* For a description of bits 4 and 5 of the status byte, please refer to the description of the bits 4 and 5 of the control byte on the next page.

**Control byte C0**



**Fig. A-20:** Control byte C0 of the STL-C100

| Bit | Name          | Description   |
|-----|---------------|---|
| 2   | Set output Y1 | This bit sets the additional output Y1 of the counter module.<br>0: Output OFF<br>1: Output ON  |
| 3   | Set output Y2 | This bit sets the additional output Y2 of the counter module.<br>0: Output OFF<br>1: Output ON  |
| 4   | Lock Counter  | When this bit is set, the count process is suppressed.<br>Bit 4 in the status byte S0 indicates the suppression of the counter.   |
| 5   | Set Counter   | When this bit is set, the counter is loaded with the 32 bit value of the output bytes 0 to 3. As long as the bit is set, the counter is stopped and the loaded value is latched. The successful loading of the counter is indicated by bit 5 of the status byte S0. |

**Tab. A-18:** Description of the control byte C0 of the STL-C100

**A.1.8 SSI Transmitter Interface STL-SSI (ID number 51205057)**

Using the SSI Transmitter Interface STL-SSI, a 5 byte input and output process image can be transferred to the head station via one logical channel.

The data received by the transmitter are stored in 3 input bytes (D0 to D2). Neither the input byte (D3) and the four output bytes (D0 to D3) nor the control byte (C0) and status byte (S0) are used.

| Input data |                            | Output data |                            |
|------------|----------------------------|-------------|----------------------------|
| S0         | Status byte S0 (Not used)  | C0          | Control byte C0 (Not used) |
| D0         | Process data, byte 0 (LSB) | D0          | Set to 0. (Not used)       |
| D1         | Process data, byte 1       | D1          |                            |
| D2         | Process data, byte 2 (MSB) | D2          |                            |
| D3         | Set to 0. (Not used)       | D3          |                            |

**Tab. A-19:** Input and output bytes of the STL-SSI

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**HEADQUARTERS**

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