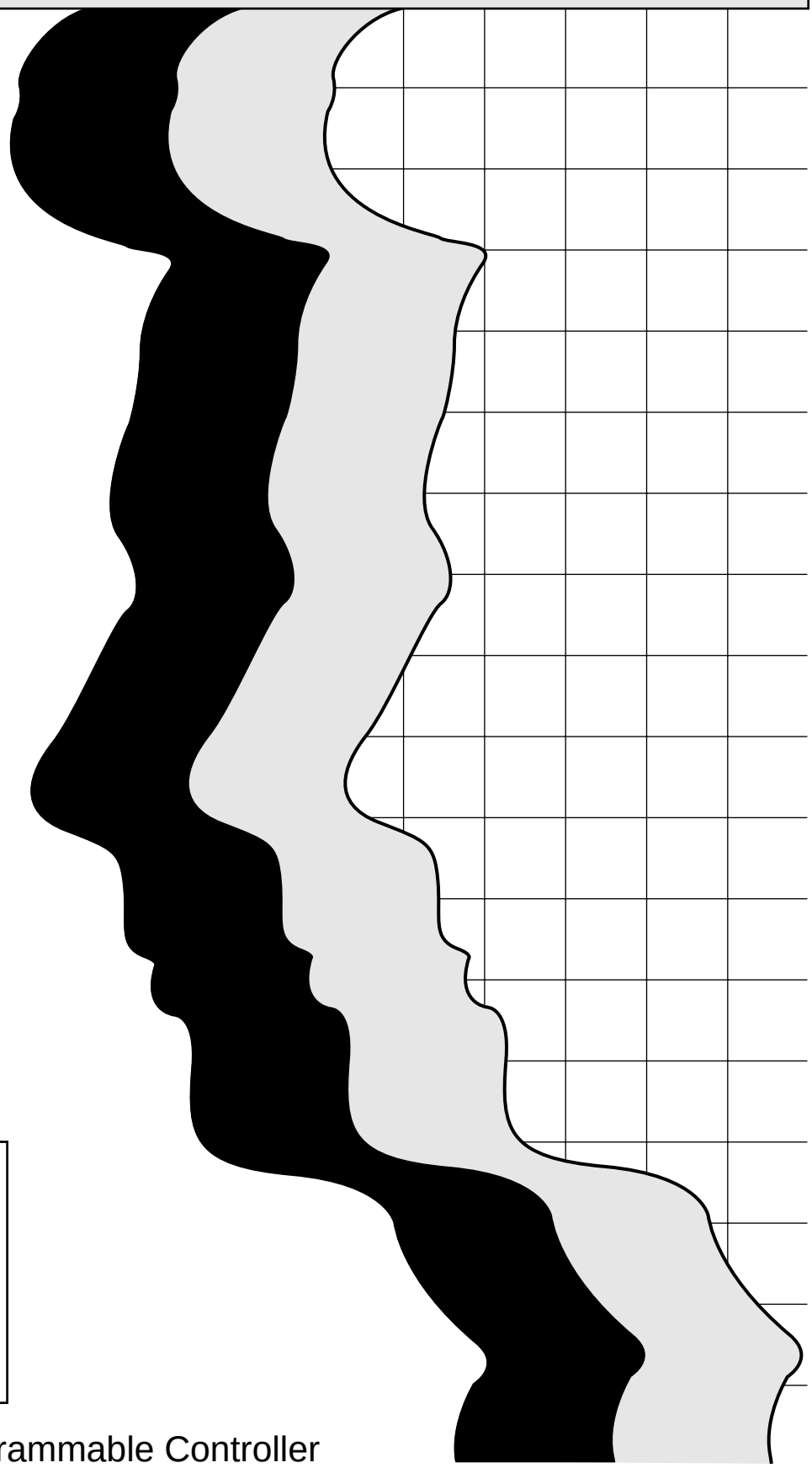
MITSUBISHI

Multiplex system type A3VTS

User's Manual



A

MELSEC

Mitsubishi Programmable Controller

REVISIONS

※The manual number is given on the bottom left of the back cover.

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

1. INTRODUCTION

This manual describes the functions and operation of the highly reliable A3VTS multiplex system programmable controller (hereafter referred to as A3VTS).

The A3VTS system is equipped with dual power supply modules and three CPU modules. The CPU contains one majority A3VTU and three A3VCPU multiplex CPU modules.

Various modules in the A3VTS system can be replaced without stopping the system even if the power supply or CPU malfunctions. This system features improved functions, performance and reliability compared to systems using previous programmable controller CPU modules.

Any previous sequence program written by the ACPU can be used with the A3VTS.

The improved features, performance and functions of the A3VTS are described on the following page.

The following abbreviations are used to indicate the A6GPP, A6PHP, A6HGP or A7PU peripheral device.

A6GPP → GPP
A6PHP → PHP
A6HGP → HGP
A7PU → PU

The A6GPP, A6PHP, A6HGP and A7PU are also referred to as peripheral device when related expression is common to all of them.

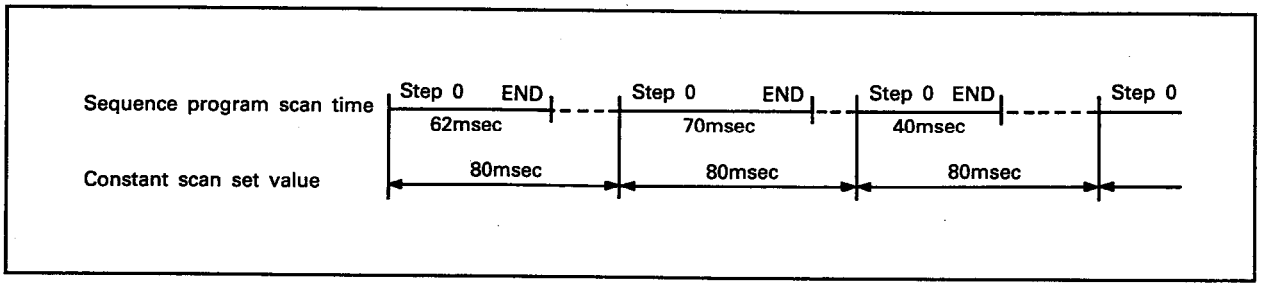
1.1 Features

The A3VTS is an integrated system configured of modules featuring the characteristics described below. This section describes the representative features.

(1) Improved reliability and operating ratio through the adoption of multiple power supply and CPU modules.
The A3VTS system uses a dual power supply and three CPU modules to perform system operations in the multiple-module, majority operation.
If there is a malfunction in either the power supply or the CPU, operation automatically switches to another power supply module or CPU module which is functioning normally. Majority operation results are obtained for the output (Y) from the three A3VCPU modules and then are output.

(2) Module installation in the online mode
A malfunctioning power supply module or CPU can be replaced during operation without having to terminate the current operation.
An I/O module can also be replaced without terminating the current output module system operations by setting the control offline only for the I/O module which is to be replaced.
The operation ratio and reliability of the A3VTS system are improved by replacing any power supply module or CPU module which malfunctions during operation within 24 hours.

(3) Constant scan function
The constant scan function sets the activation cycle of the sequence program scan and can execute the program at specified intervals.
Program scan time normally varies depending on the execution instruction conditions or the presence of subroutine programs.
If the control scan function is used the program scan time is set to a regular interval. This allows the control of external devices without variation in control intervals caused by scan time variation.



(4) Compatibility with A3(E)CPU, A3NCPU and A3HCPU systems
The compatibility of I/O modules (special function modules) and programs for A3CPU, A3NCPU and A3HCPU based systems is described below.

(a) I/O module (special function module) compatibility
I/O modules can be basically used in the A3VTS system. However some modules cannot be used.
Refer to section 2.2 or Appendices 2 to 4 for details.

(b) Sequence program compatibility
Generally, previously written sequence programs can be used in the A3VTS system.
However, some instructions cannot be used, and some instructions differ in terms of devices and specifications.
Refer to Appendices 2 to 4 for further details.

(5) Peripheral device (software package) compatibility

The following peripheral devices can be used with the A3VTS without modification.

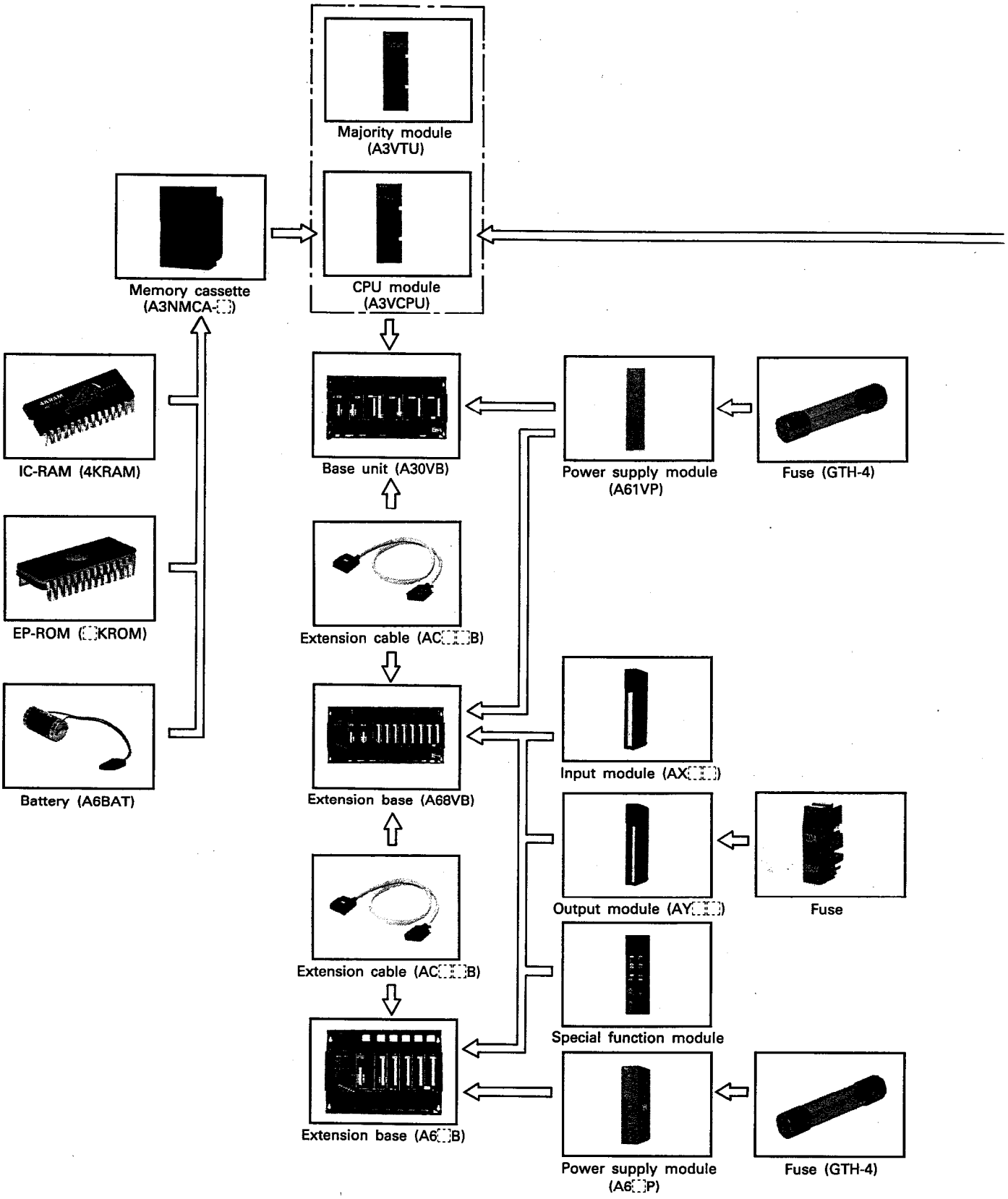
A6GPP
A6PHP
A6HGP
A7PU
A6WU

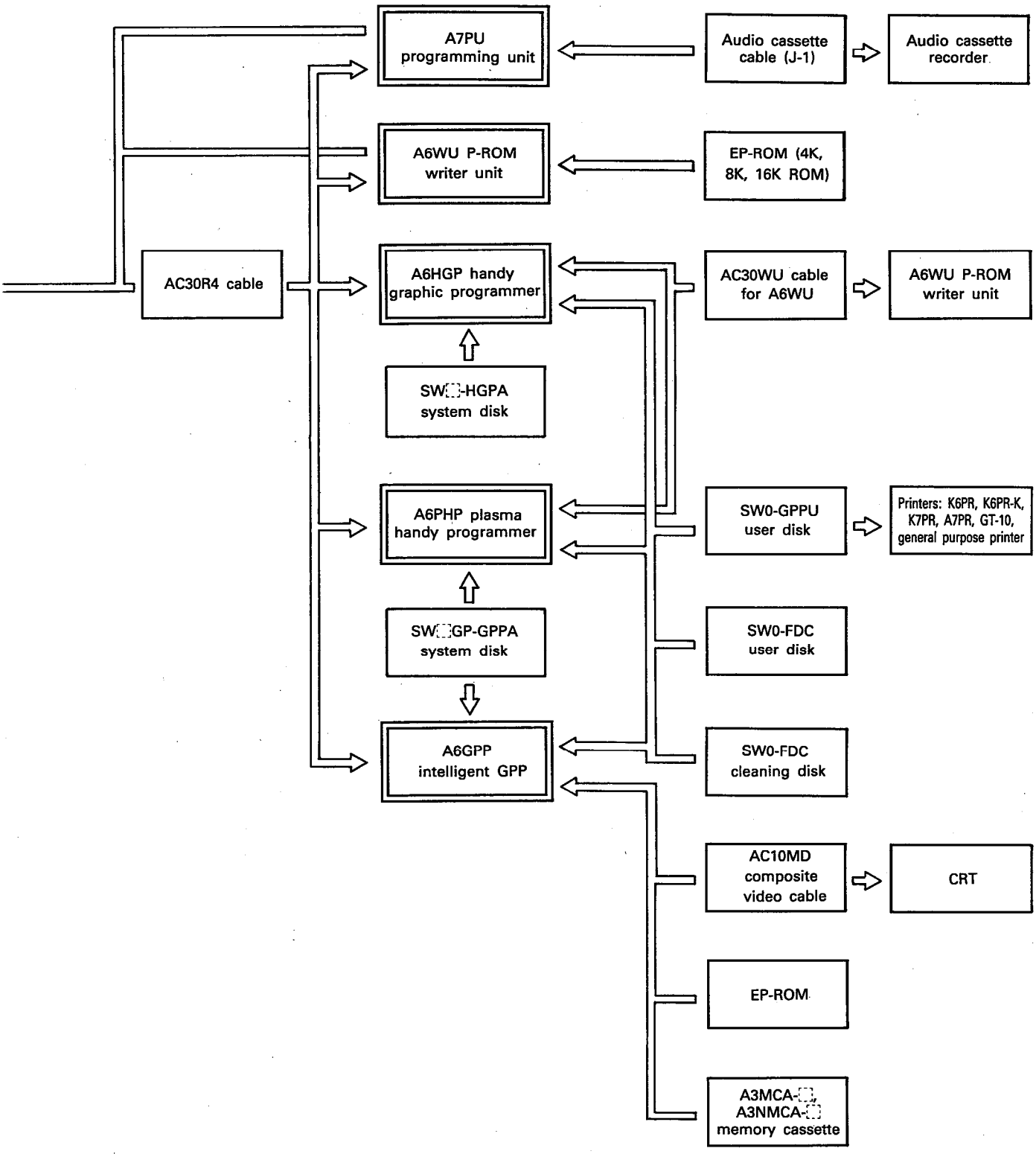
The floppy disks described below can be used to boot the A6GPP, A6PHP or A6HGP systems.

SW0-GPPA to SW3-GPPA (A6GPP system disk)
SW3GP-GPPA (A6GPP/A6PHP system disk)
SW0-HGPA to SW3-HGPA (A6GPP system disk)

2. SYSTEM CONFIGURATION

2.1 Overall Configuration




A7PU programming unit
Audio cassette cable (J-1)
Audio cassette recorder
A6WU P-ROM writer unit
EP-ROM (4K, 8K, 16K ROM)
AC30R4 cable
A6HGP handy graphic programmer
AC30WU cable for A6WU
A6WU P-ROM writer unit
SW□-HGPA system disk
A6PHP plasma handy programmer
SW0-GPPU user disk
Printers: K6PR, K6PR-K, K7PR, A7PR, GT-10, general purpose printer
SW□GP-GPPA system disk
SW0-FDC user disk
A6GPP intelligent GPP
SW0-FDC cleaning disk
AC10MD composite video cable
CRT
EP-ROM
A3MCA-□, A3NMCA-□ memory cassette

2.2 A3VTS System Usage Precautions

This section describes precautions for the A3VTS architecture and usage.

(1) The A3VTS system is a multiplex system that uses two power supply modules and three CPU modules.
The multiplex system architecture enables continuous system operations even if a power supply module or CPU module malfunctions. As a result, the system operates with high operation ratio and reliability.
Although system operations using a power supply module and one or two CPU modules is possible, multiplex system operation is not possible in such a configuration because system operation stops of an error occurs.

(2) System operation will stop if a power supply module malfunctions when an extension base using the conventional power supply module (A61P to A65P) is installed in the system using the dual power supply modules. (The same conditions exist for A81CPU PID control CPU modules when installed.)
All the extension base units used in the system with dual power supply modules should use an extension base module for dual power supply modules to ensure improved operation ratio and reliability.

(3) Extension base units (A55B and A58B) cannot be used in the A3VTS system. The A3VTS system cannot supply them with 5 VDC.

(4) The combinations of base units and power supply modules is shown in the table. ("○" symbol indicates possible combinations and "×" symbol indicates combinations which are not possible). Do not make any of the combinations indicated by an "×" since this may damage the power supply modules.

Base Type \ Power Supply Module Type	A61VP	A61P	A62P	A63P	A65P
A30VB A68VB	○	×	×	×	×
A65B	×	○	○	○	○
A68B	×	○	○	○	○

(5) Special function modules which cannot be used
(a) AD57(S1) CRT controller module
(b) AD58 LCD controller module
(c) AI61 interrupt module
(d) AJ71C24(S3) computer link module
(e) AD51 intelligent communication module
*AD51 modules can be used under the following conditions. No other functions are usable in the A3VTS system.

AD51 ····· The AD51 buffer memory can be accessed by the FROM / TO instruction.
Refer to Appendix 9 for details regarding possible functions (commands).

(6) Software packages which cannot be used
SW□GHP-UTLPC-PID utility package
SW□GP-AD57P system disk
SW□GHP-UTLPC-FN1 utility package

(7) There are some peripheral device functions which cannot be used during A3VTS system majority operation.
These functions are described below.

(a) Writing cannot be performed during a RUN operation.
If a write operation is performed during a RUN operation, the A3VCPU generates an error and drops from system operation.

(b) Forced output cannot be used.
If forced output is performed, the A3VCPU generates an error and drops from system operation.

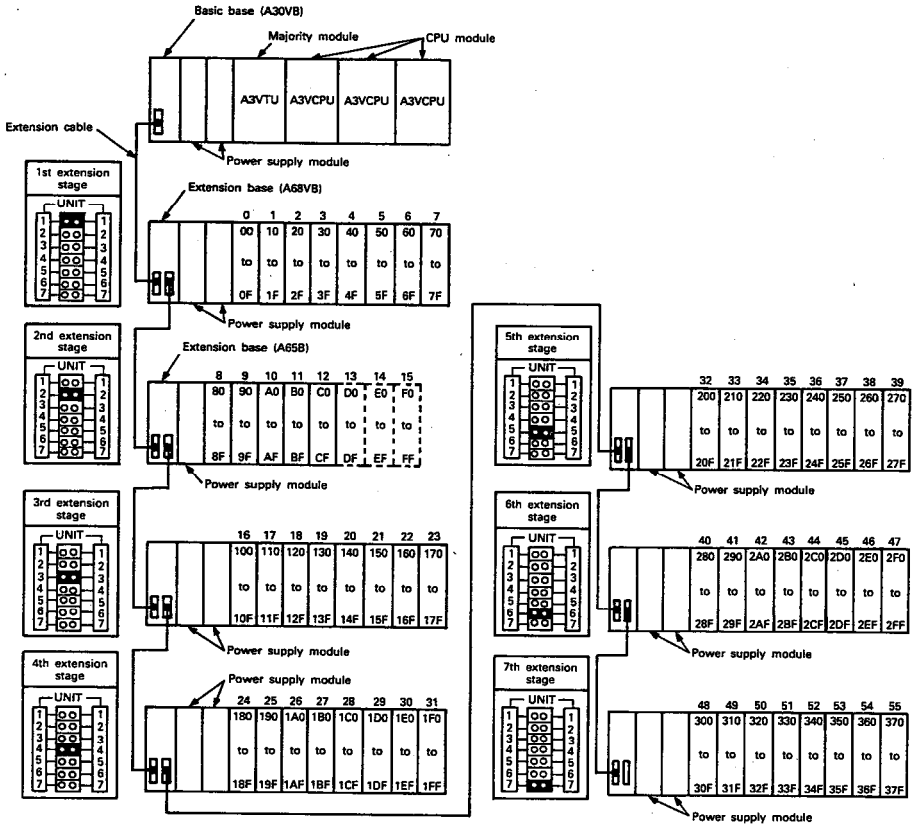
When data is written to a data register during test operation, an error occurs when output (Y) is executed if the data influences the output (Y) and the A3VCPU drops from system operation.

(c) The offline switch cannot be used.
If the offline switch is used the A3VCPU generates an error and drops from operation.

(8) When the A3VCPU has dropped from system operation due to an error during majority operation, normal operation can be restored by correcting the error or replacing the malfunctioning module.
400ms is necessary for restore processing and the scan time for restore processing is extended 400ms. Consequently, when majority operation is performed, set the WDT to a value equal to the normal scan time +400ms.
If the setting value is small, an error will be generated by all A3VCPUs when the A3VCPU restores operation and system operations stop.
When an error has been remedied or an A3VCPU has been replaced and the A3VCPU's operation in the system is to be restored, restore A3VCPU operation at a point which will not have an effect even if control is delayed due to increased scan time as described above.

(9) Refer to the A3VTS Multiplex Data Link System User's Manual for details about precautions for systems used with the multiplex link system.

(10) A3VTS system configuration

System configuration	 (In this case, each slot is loaded with 16-point unit.)
Maximum number of extension stages	7
Maximum number of loaded I/O modules	56
Maximum number of I/O points	2048
Basic base/extension base types	A30VB/A68VB, A65B, A68B
Extension cable types	AC06B, AC12B, AC30B
Restrictions	(1) Any extension base (A55B, A58B) cannot be connected to the A3VTS system. (2) The extension cable may be used for distances up to 6.6m (21.65ft).
Assignment of I/O numbers	(1) Assign I/O numbers in order of the stage setting numbers of extension bases without regard to the connection order of extension cables. (2) Assign I/O numbers on the assumption that the extension base have 8 slots each. Therefore, assign 16 points/slot to the slot with dotted line the extension base on the assumption that the A35B has 3 more slots (48 points). (3) Assign 16 points to an empty slot. (4) When the setting of extension stages has been omitted, make assignment on the assumption that 16 points are occupied per slot for all the number of stages × 8 slots. (5) For items (2) and (4), the assignment can be changed according to Section 4.6.3 "Assignment of I/O numbers".

2.3 System Configuration

Table 2.1 show the system equipment consisting of various modules and units which can be used.

M station: Master station, L station: Local station,
○: Indicates that it is usable.

Module		Type	Description	Occupied Points	Applicable System							Remarks
					Independent	Coaxial data link			Optical data link			
						M station	L station		M station	L station	Computer link	
Majority system		A3VTS	Consist of the following models: A3VTU·····1 A3VCPU·····3 A61VP·····2 A30VB·····1		○						○	
CPU module		A3VCPU	Program capacity: 30K steps, I/O points: 2048 M, L, S total: 2048, T: 256, C: 256, D: 1024	—	○	○	○		○		○	Memory cassette to be arranged separately.
Majority module		A3VTU	For independent system	—	○	○	○		○	○	○	
Memory cassette		A3NMCA-0	Without IC-RAM memory	—	○	○	○		○	○	○	• With two memory sockets • A3NMAC-0 can be loaded with IC-RAM or EP-ROM memory. • A3NMCA-2 to -24 can be loaded with only EP-ROM memory.
		A3NMCA-2	With IC-RAM memory 16K bytes									
		A3NMCA-4	With IC-RAM memory 32K bytes									
		A3NMCA-8	With IC-RAM memory 64K bytes									
		A3NMCA-16	With IC-RAM memory 128K bytes									
		A3NMCA-24	With IC-RAM memory 192K bytes									
Memory	IC-RAM	4KRAM	8K bytes (max. 3K steps)	—	○	○	○		○	○	○	
	EP-ROM	4KROM	8K bytes (max. 3K steps)									
		8KROM	16K bytes (max. 7K steps)									
		16KROM	32K bytes (max. 15K steps)									
Input module		AX10	16 points, 100-120V AC	16	○	○	○		○	○	○	
		AX11	32 points, 100-120V AC	32								
		AX20	16 points, 200-240V AC	16								
		AX21	32 points, 200-240V AC	32								
		AX40	16 points, 12/24V DC	16								
		AX41	32 points, 12/24V DC	32								
		AX41-S1	32 points, 12/24V DC, fast response type	32								
		AX42	64 points, 12/24V DC	64								
		AX42-S1	64 points, 12/24V DC, fast response type	64								

Table. 2.1 List of Equipment (Continue)

Module	Type	Description	Occupied Points	Applicable System							Remarks
				Independent	Coaxial data link			Optical data link			
					M station	L station		M station	L station	Computer link	
Input module	AX50	16 points, 48V AC	16	○	○	○		○	○	○	▭ indicates source loading. The other modules are of sink loading with the exception of the AX50-S1 and AX60-S1 which may be used as both a sink and a source loading module.
	AX50-S1	16 points, 48V DC, sink/source selectable	16								
	AX60	16 points, 100/110/125V DC	16								
	AX60-S1	16 points, 100/110/125 DC, sink/source selectable	16								
	AX70	16 points for sensor	16								
	AX71	32 points for sensor	32								
	AX80	16 points, 12/24V DC source loading	16								
	AX80E	16 points, 12/24V DC source loading	16								
	AX81	32 points, 12/24V DC source loading	32								
	AX81-S1	32 points, 12/24V DC, source, low on/off response threshold	32								
	AX82	64 points, 12/24V DC source loading	64								

Table. 2.1 List of Equipment (Continue)

POINT

(1) Although memory cassette capacity is 128KB for A3NMCA-16 and 192KB for A3NMCA-24, maximum memory area usable for parameters is 96KB and 144KB, respectively.

(2) Any conventional memory cassette A3MCA-□ may be used.

Module	Type	Description	Occupied Points	Applicable System							Remarks
				Independent	Coaxial data link			Optical data link			Computer link	
					M station	L station		M station	L station			
Output module	AY10	16 points, relay contact	16	○	○	○		○	○		○	▭ indicates source loading.
	AY10A	16 points, relay contact, for independent contact output	16									
	AY11	16 points, relay contact, with surge suppression	16									
	AY11A	16 points, relay contact, for independent contact output, with surge suppression	16									
	AY11E	16 points, relay contact, (with fuse)	16									
	AY13	32 points, relay contact	32									
	AY13E	32 points, relay contact, (with fuse)	32									
	AY22	16 points, triac for 2A (with fuse)	16									The other modules are of sink loading. The short and overheat protection functions of the AY60EP, AY80EP, AY81EP, AY82EP are as follows:
	AY23	32 points, triac for 0.6A (with fuse)	32									
	AY40	16 points, 12/24V DC transistor for 0.1A	16									
	AY40A	16 points 12/24V DC transistor for independent contact output, 0.3A	16									Short protection function Protects the transistor from overcurrent due to external wiring short, etc.
	AY41	32 points, 12/24V DC transistor output for 0.1A	32									
	AY42	64 points, 12/24V DC transistor for 0.1A	64									Overheat protection function Protects the transistor from abnormally high temperature due to any external factor.
	AY42-S1	64 points, 12/24V DC transistor, 0.1A fast response type	64									
	AY50	16 points, 12/24V DC transistor for 0.5A (with fuse)	16									
	AY51	32 points, 12/24V DC transistor for 0.5A (with fuse)	32									
	AY60	16 points, 12/24/48V DC transistor for 2A (with fuse)	16									
	AY60S	16 points, 12/24/48V DC transistor, 2A (6.4A/common)	16									
	AY60E	16 points, 12/24/48V DC transistor for 2A (with fuse)	16									
	AY60EP	16 points 12/24V DC transistor for 2A with short and overheat protection functions	16									

Table 2.1 List of Equipment (Continue)

Module	Type	Description	Occupied Points	Applicable System								Remarks
				Independent	Coaxial data link			Optical data link			Computer link	
					M station	L station		M station	L station			
Output module	AY70	16 points (5/12V DC) for TTL, CMOS	16	○	○	○		○	○		○	▭ indicates source loading.
	AY71	32 points (5/12V DC) for TTL, CMOS	32									
	AY80	16 points, 12/24/48V DC transistor for 0.5A (with fuse)	16									
	AY80EP	16 points, 12/24V DC transistor 0.8A with short and overheat protection functions	16									
	AY81	32 points, 12/24V DC transistor for 0.5A	32									
	AY81EP	32 points, 12/24V DC transistor for 0.8A with short and overheat protection functions	32									
	AY82EP	64 points, 12/24V DC transistor for 0.1A with short and overheat protection functions	64									
Dynamic combined I/O module	A42XY	64 inputs, 64 outputs Dynamic scanning mode	64	○	○	○		○	○		○	I/O are processed with scanning made in groups of 8 points independently of the CPU module.

Table 2.1 List of Equipment (Continue)

	Module	Type	Description	Occupied Points	Applicable System								Remarks
					Independent	Coaxial data link			Optical data link			Computer link	
						M station	L station		M station	L station			
Special function module	Positioning	AD71	For positioning control Pulse chain output, 2 axes (independent, simultaneous 2 axes, linear interpolation) A stepping motor can be used when AD76 module is used in conjunction with this module.	32	○	○	○		○	○		○	
		AD71S1	For positioning control For MELDAS-S1 servo driver (dedicated) Pulse chain output, 2 axes (independent, simultaneous 2 axes, linear interpolation)	32	○	○	○		○	○		○	
		AD72	For positioning control Analog voltage output (0 to ± 10V DC) 2 axes (independent, simultaneous 2 axes, linear interpolation)	48	○	○	○		○	○		○	
	High-speed counter	AD61	Binary 24 bits, 1/2 phase input, reversible counter 50KPPS, 2 channels	32	○	○	○		○	○		○	
		AD61S1	Binary 24 bits, 1/2 phase input, reversible counter 1 phase·····10KPPS, 2 phases··· ···7KPPS 2 channels	32	○	○	○		○	○		○	
	A/D converter	A68AD(S3)	4 to 20mA/0 to ±10V Analog input 12 bits, 8 channels	32	○	○	○		○	○		○	
	D/A converter	A62DA(S1)	4 to 20mA/0 to ±10V Analog output 12 bits, 2 channels	32	○	○	○		○	○		○	
	A/D, D/A converter	A84AD	4 to 20mA/0 to ±10V Analog I/O 15 bits, 4 channels	48	○	○	○		○	○		○	
	Memory card/ Centronics interface	AD59	32K bytes memory, battery backed May be connected with any printer conforming to Centronics Standards.	32	○	○	○		○	○		○	
	Voice output	A11VC	Messages can be recorded/replayed on max. 60 channels. 1, 2, 4 or 8 seconds may be selected per channel. Total recording time 64 seconds.	16	○	○	○		○	○		○	

Table 2.1 List of Equipment (Continue)

	Module	Type	Description	Occupied Points	Applicable System: Independent	Coaxial data link: M station	Coaxial data link: L station	Coaxial data link:	Optical data link: M station	Optical data link: L station	Optical data link:	Computer link	Remarks	
Special function module	Intelligent communication module	AD51E	Allows max. 8 multitaskings of GPC-BASIC programs for data transfer between the PC and computer and control status monitoring. Data communication with the computer in free format. Two RS-232C, two RS-422 channels.	48								○	Refer to POINT	Up to two of any modules may be used with one CPU.
	Multidrop data link module and units	AJ71C22	Multidropped with max. 8 slave stations to make bit data transfer. For multidrop link master station. Transmission speed: 38.4KBPS One RS-422 channel	32	○	○	○		○	○		○		
		A0J2C25	For multidrop link remote I/O station	___									AJ71C22 connection device	
		A0J2C214	For multidrop link local station (May be used as the computer link or multidrop link master station in an A0J2CPU system)	64										
	PID control CPU module	A81CPU	CPU module for process PID control PID operation for up to 64 loops and 32 programs can be made. (max. 8000 memory steps)	128	○	○	○		○	○		○	Can be connected to the A3VTS, master station or local station.	
	Dummy module	AG62	16, 32, 48 or 64 points may be selected.	Number of set points	○	○	○		○	○		○	With 16 simulation switches	
	Blank cover	AG60	Dustproof cover for use in vacant slot	16	○	○	○		○	○		○		

Table 2.1 List of Equipment (Continue)

POINT

Refer to Appendix 9 when the AD51E is used with the A3VTS system since there are restrictions on the functions to be used.

<table>
<tr><th rowspan="2">Module</th><th rowspan="2">Type</th><th rowspan="2">Description</th><th rowspan="2">Occupied Points</th><th colspan="8">Applicable System</th><th rowspan="2">Remarks</th></tr>
<tr><th>Independent</th><th colspan="2">Coaxial data link</th><th colspan="3">Optical data link</th><th>Computer link</th></tr>
<tr><td rowspan="4">Multiplex data link system</td><td>A3VTS -VP21</td><td>Consists of the following modules:
<table><tr><th>Type</th><th>Number of modules</th></tr><tr><td>A3VTU</td><td>1</td></tr><tr><td>A3VCPU</td><td>3</td></tr><tr><td>AJ71VP21</td><td>2</td></tr><tr><td>A30LVB</td><td>1</td></tr><tr><td>A61VP</td><td>2</td></tr></table></td><td>—</td><td></td><td></td><td></td><td></td><td>○</td><td>○</td><td></td><td>○</td><td></td></tr>
<tr><td>A3VTS -VR21</td><td>Consists of the following modules:
<table><tr><th>Type</th><th>Number of modules</th></tr><tr><td>A3VTU</td><td>1</td></tr><tr><td>A3VCPU</td><td>3</td></tr><tr><td>AJ71VR21</td><td>2</td></tr><tr><td>A30LVB</td><td>1</td></tr><tr><td>A61VP</td><td>2</td></tr></table></td><td>—</td><td></td><td>○</td><td>○</td><td></td><td></td><td></td><td></td><td>○</td><td></td></tr>
<tr><td>A3CPU -VP21</td><td>Consists of the following modules:
<table><tr><th>Type</th><th>Number of modules</th></tr><tr><td>A3VTU</td><td>1</td></tr><tr><td>A3VCPU</td><td>1</td></tr><tr><td>AJ71VP21</td><td>2</td></tr><tr><td>A20LVB</td><td>1</td></tr><tr><td>A61VP</td><td>2</td></tr></table></td><td>—</td><td></td><td></td><td></td><td></td><td>○</td><td>○</td><td></td><td>○</td><td></td></tr>
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<tr><td>Data link module: Coaxial data link module</td><td>AJ71VR21</td><td>For master station or local stations. For high-reliability, coaxial cable data link.</td><td>—</td><td></td><td>○</td><td>○</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Data link module: Optical data link module</td><td>AJ71VP21</td><td>For master station or local stations. For high-reliability, optical data link.</td><td>—</td><td></td><td></td><td></td><td></td><td>○</td><td>○</td><td></td><td></td><td></td></tr>
<tr><td rowspan="6">Power supply module</td><td>A61VP</td><td>Input: 110/220V AC; Output: 5V DC 5A, 24V DC 0.8A; For use in power supply slot</td><td>—</td><td>○</td><td>○</td><td>○</td><td></td><td>○</td><td>○</td><td></td><td>○</td><td>May be used with main base unit (A30VB, A30LVB, A20LVB) and extension base unit (A68VB).</td></tr>
<tr><td>A61P</td><td>Input: 110/220V AC; Output: 5V DC 8A; For use in power supply slot</td><td rowspan="5">—</td><td rowspan="5">○</td><td rowspan="5">○</td><td rowspan="5">○</td><td rowspan="5"></td><td rowspan="5">○</td><td rowspan="5">○</td><td rowspan="5"></td><td rowspan="5">○</td><td rowspan="3">May be used with extension base unit (A65B, A68B).</td></tr>
<tr><td>A62P</td><td>Input: 110/220V AC; Output: 5V DC 5A, 24V DC 0.8A; For use in power supply slot</td></tr>
<tr><td>A63P</td><td>Input: 24V DC; Output: 5V DC 8A; For use in power supply slot</td></tr>
<tr><td>A65P</td><td>Input: 110/220V AC; Output: 5V DC 2A, 24V DC 1.5A; For use in power supply slot</td><td rowspan="2">May be used with extension base unit (A68VB, A65B, A68B).</td></tr>
<tr><td>A66P</td><td>Input: 110/220V AC; Output: 24V DC 1.2A; For use in I/O slot</td><td>16</td></tr>
</table>

Table 2.1 List of Equipment (Continue)

Module		Type	Description	Occupied Points	Applicable System							Remarks
					Independent	Coaxial data link			Optical data link			
						M station	L station		M station	L station	Computer link	
Base unit	Main base unit	A30VB	Main base for A3VTS The following number of modules can be installed. A3VTU: 1 module, AV3CPU: 3 modules, A61VP: 2 modules	—	○						○	
		A30LVB	Base for A3VTS-VP21/VR21 The following number of modules can be installed. A3VLU-L: 1 module, AV3CPU: 3 modules, A61VP: 2 modules, AJ71VP21/VR21: 2 modules			○	○		○	○		
		A20LVB	Base for A3VTS-VP21/VR21 The following number of modules can be installed. A3VLU-L: 1 module, AV3CPU: 1 module, A61VP: 2 modules, AJ71VP21/VR21: 2 modules			○	○		○	○		
		A68VB	Extension base for A3VTS The following number of modules can be installed. I/O module: 8 modules, A61VP: 2 modules	—	○	○	○		○	○	○	
		A68B	Can accommodate 8 I/O modules.									
		A65B	Can accommodate 5 I/O modules.									
Extension cable		AC06B	600mm long	For use between base units	—	○	○	○		○	○	○	
		AC12B	1200mm long									
		AC30B	3000mm long									
Simulation switch		A6SW16	16 points simulation switch		—	○	○	○		○	○	○	Used with an input module.
		A6SW32	32 points simulation switch									
Others	Battery	A6BAT	IC-RAM backup		—	○	○	○		○	○	○	
	Fuse For AY22	HP-70K	Plug type 7A		—	○	○	○		○	○	○	
	Fuse For AY23	HP-32	Plug type 3.2A										
	Fuse For AY50, AY80	MP-20	Plug type 2A										
	Fuse For AY60	MP-32	Plug type 3.2A										
	Fuse For AY60E	MP-50	Plug type 5A										
	Fuse For power supply	GTH-4	Cartridge type 4A										

Table. 2.1 List of Equipment

<table>
<tr><th>Unit</th><th>Description</th><th>Type</th><th>Remarks</th></tr>
<tr><td rowspan="2">Programming unit with CRT</td><td>Intelligent GPP</td><td>A6GPPE-SET</td><td>○ Consists of the following models:
<table>
<tr><th>Type</th><th>Remarks</th></tr>
<tr><td>A6GPPE</td><td>○ Programming unit with CRT
○ Equipped with ROM writer, FDD and printer interface functions.</td></tr>
<tr><td>SW□GP-GPPAEE</td><td>A series system disk</td></tr>
<tr><td>SW□GP-GPPKEE</td><td>K series system disk</td></tr>
<tr><td>SW0-GPPU</td><td>User disk (3.5 inch, formatted)</td></tr>
<tr><td>AC30R4</td><td>Cable for connection of CPU and A6GPP
3m/9.84ft length</td></tr>
</table></td></tr>
<tr><td>Composite video cable</td><td>AC10MD</td><td>Cable for connection of GPP and expanded monitor display. 1m/3.28ft length.</td></tr>
<tr><td>Programming unit with LCD</td><td>Handy graphic programmer</td><td>A6HGPE-SET</td><td>○ Consists of the following models:
<table>
<tr><th>Type</th><th>Remarks</th></tr>
<tr><td>A6HGPE</td><td>○ Programming unit with LCD
○ Equipped with FDD, printer interface and memory card interface functions.</td></tr>
<tr><td>SW□-HGPAEE</td><td>A series system disk</td></tr>
<tr><td>SW□-HGPKEE</td><td>K series system disk</td></tr>
<tr><td>SW0-GPPU</td><td>User disk (3.5 inch, formatted)</td></tr>
<tr><td>AC30R4</td><td>Cable for connection of CPU and A6HGP
3m/9.84ft length</td></tr>
</table></td></tr>
<tr><td>Programming unit with plasma display</td><td>Plasma handy programmer</td><td>A6PHPE-SET</td><td>○ Consists of the following models:
<table>
<tr><th>Type</th><th>Remarks</th></tr>
<tr><td>A6PHPE</td><td>○ Programming unit with plasma display
○ Equipped with FDD, printer interface and memory card interface functions.</td></tr>
<tr><td>SW□GP-GPPAEE</td><td>A series system disk</td></tr>
<tr><td>SW□GP-GPPKEE</td><td>K series system disk</td></tr>
<tr><td>SW0-GPPU</td><td>User disk (3.5 inch, formatted)</td></tr>
<tr><td>AC30R4</td><td>Cable for connection of CPU and A6PHP
3m/9.84ft length</td></tr>
</table></td></tr>
<tr><td rowspan="4">Common to programming units with CRT and LCD</td><td rowspan="2">RS-422 cable</td><td>AC30R4</td><td rowspan="2">Cable for connection of CPU and A6GPP/A6HGP/A6PHP</td><td>3m (9.84ft) length</td></tr>
<tr><td>AC300R4</td><td>30m (98.4ft) length</td></tr>
<tr><td>User disk</td><td>SW0-GPPU</td><td colspan="2">User disk (3.5 inch, formatted) for storing programs</td></tr>
<tr><td>Cleaning disk</td><td>SW0-FDC</td><td colspan="2">Cleaning disk for disk drive</td></tr>
</table>

Table. 2.2 Configuration Expansion (Continue)

Unit	Description	Type	Remarks
Printer	Printer	K6PRE K7PRE	○ For print out of program ladder diagrams and lists.
	RS-232C cable	AC30R2	Cable for connection of A6GPP/A6PHP/A6HGP and printer. 3m/9.84ft length.
	Printer paper	K6PR-Y	Paper for K6PRE. 9 inch. Available in units of 2000.
	K6PR Ink ribbon	K6PR-R	Replacement ink ribbon for A6PRE
Programming unit	Programming unit	A7PU	○ Connected to the CPU directly or via cable to read and write programs. Equipped with MT function. ○ The A7PU is supplied with a cable for connection of the A7PU and audio cassette recorder.
	RS-422 cable	AC30R4 AC300R4	Cable for connection of CPU and A7PU. 3m(9.84ft)/30m(98.4ft) length.
P-ROM writer unit	P-ROM writer unit	A6WU	○ Used to store programs onto ROM and read programs from ROM to the CPU. ○ Connected to the CPU directly or via the AC30R4 cable.
	RS-422 cable	AC30R4 AC300R4	Cable for connection of CPU and A6WU. 3m(9.84ft)/30m(98.4ft) length.
Software Package	GPP-BASIC package	SW□GHP -BAS	Software package for creating and executing BASIC programs by A6GPP, A6PHP or A6HPG.
	Functional operation package	SW□GHP-UTLPC-FN0	Software package for calculating trigonometric functions, square roots, etc.

Table 2.2 Configuration Expansion

3. GENERAL SPECIFICATIONS

Table 3.1 shows the common specifications of various modules used.

<table>
<tr><th>Item</th><th colspan="5">Specifications</th></tr>
<tr><td>Operating ambient temperature</td><td colspan="5">0 to 55℃</td></tr>
<tr><td>Storage ambient temperature</td><td colspan="5">−20 to 75℃</td></tr>
<tr><td>Operating ambient humidity</td><td colspan="5">10 to 90%RH, non-condensing</td></tr>
<tr><td>Storage ambient humidity</td><td colspan="5">10 to 90%RH, non-condensing</td></tr>
<tr><td rowspan="3">Vibration resistance</td><td rowspan="3">Conforms to * JIS C 0911</td><td>Frequency</td><td>Acceleration</td><td>Amplitude</td><td>Sweep Count</td></tr>
<tr><td>10 to 55Hz</td><td>——</td><td>0.075mm (0.003inch)</td><td rowspan="2">10 times
*(1 octave/minute)</td></tr>
<tr><td>55 to 150Hz</td><td>1G</td><td>——</td></tr>
<tr><td>Shock resistance</td><td colspan="5">Conforms to JIS C 0912 (10g × 3 times in 3 directions)</td></tr>
<tr><td>Noise durability</td><td colspan="5">By noise simulator of 1000Vpp noise voltage,
1 μs noise width and 25 to 60Hz noise frequency</td></tr>
<tr><td>Dielectric withstand voltage</td><td colspan="5">1500V AC for 1 minute across AC external terminals and ground
500V AC for 1 minute across DC external terminals and ground</td></tr>
<tr><td>Insulation resistance</td><td colspan="5">5MΩ or larger by 500V DC insulation resistance tester across
AC external terminals and ground</td></tr>
<tr><td>Grounding</td><td colspan="5">Class 3 grounding; grounding is not required when it is impossible.</td></tr>
<tr><td>Operating ambience</td><td colspan="5">Free of corrosive gases. Dust should be minimal.</td></tr>
<tr><td>Cooling method</td><td colspan="5">Self-cooling</td></tr>
</table>

Table 3.1 General Specifications

REMARKS

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10Hz to 20Hz, from 20Hz to 40Hz, from 40Hz to 20Hz, and 20Hz to 10Hz are referred to as one octave.

Note: * JIS: Japanese Industrial Standard

4. A3VTU AND A3VCPU MODULES

This section describes the specifications, performance, function, memory capacity, and devices of the A3VTU and A3VCPU modules. Since these performance and functions cannot be demonstrated independently, the descriptions are given for the combination of the A3VTU and A3VCPU modules.

4.1 Specifications

The A3VTS and A3VCPU performance specifications are indicated in Table 4.1.

Item \ Type		A3VTU+A3VCPU		Refer to:
Control system		Repeated operation (using stored program)		4.2
I/O control method		I/O image refresh mode		4.3
Programming language		Language dedicated to sequence control (Combined use of relay symbol type, logic symbolic language, and Sequence Action Program language)		4.4
Number of instructions	Sequence instruction	22		For details, see the Programming Manual.
	Basic instruction	128		
	Application instruction	107		
Processing speed (sequence instruction) (μsec/step)		1.0		Appendix. 11
I/O points		2048		4.5
Watch dog timer (WDT) (msec)		10 to 2000		4.6
Memory capacity		Up to the capacity of the memory cassette loaded		4.7 9.2
Program capacity	Main sequence program (step)	Max. 30K		—
	Subsequence program (step)	Max. 30K		—
	Microcomputer program (byte)	Max. 58K		—
Device	Internal relay (M) (point)	1000 (M0 to 999)	The number of Ms + Ls + Ss = 2048 (set in parameters)	4.8
	Latch relay (L) (point)	1048 (L1000 to 2047)		
	Number of step relays (S) (point)	0 (Defaults to no value)		
	Link relay (B) (point)	1024 (B0 to 3FF)		
	Timer — Number of points	256		
	Timer — Specifications	100ms timer: setting time 0.1 to 3276.7sec 10ms timer: setting time 0.01 to 327.67sec 100ms retentive timer: Setting time 0.1 to 3276.7 sec	Set in parameters	
	Counter — Number of points	256		
	Counter — Specifications	Normal counter: setting range 1 to 32767 (C0 to C255)		
	Data register (D) (points)	1024 (D0 to 1023)		
	Link register (W) (points)	1024 (W0 to 3FF)		
	Annunciator (F) (points)	256 (F0 to 255)		

Table 4.1 Performance List (Continue)

Item \ Type		A3VTU+A3VCPU	Refer to:
Device	File register (R) (points)	Max. 8192 (R0 to 8191)	4.8
	Accumulator (A) (points)	2 (A0, A1)	
	Index register (V, Z) (points)	2 (V, Z)	
	Pointer (P) (points)	256 (P0 to 255)	
	Special relay (M) (points)	256 (M9000 to 9255)	
	Special register (D) (points)	256 (D9000 to 9255)	
Comment (points)		Max. 4032 (Specify in batches of 64 points)	—
Self-diagnostic functions		Watchdog error supervision, Memory error detection, CPU error detection, I/O error detection, battery error detection, etc.	4.9
Operation mode at the time of error		STOP/CONTINUE	—
STOP → RUN output mode		Output data at time of STOP restored/data output after operation execution	—
At power on, at power restoration after power failure		Automatic restart when "STOP/RUN" key switch is set to RUN. (Initial start)	—
IC-RAM back-up		Battery, lithium battery used (5 years of guarantee period. For total power failure guarantee time, refer to Section 12.3.1)	—
Allowable instantaneous power failure period (ms)		within 20	—
Internal current consumption (5V DC) (A)	A3VTU	1.0	—
	A3VCPU	2.2	
Weight kg(lb)	A3VTU	0.79(1.74)	—
	A3VCPU	0.84(1.85)	
Size mm(inch)	A3VTU	250(9.84) (H) × 79.5(3.13) (W) × 121(4.76) (D)	—
	A3VCPU		

Table 4.1 Performance List

POINT

The A3VTU and A3VCPU do not provide the interrupt processing function so realtime interrupts or sequence start interrupts from an interrupt module or a special function module are ignored and the interruption program is not executed. Consequently, interrupt pointer (I) and interrupt counter (C) cannot be used.

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4.2 Operation Processings

The operation processing for the A3VTU and A3VCPU is shown in Figure 4.1.
The operation processing operations are separated into those for the A3VTU and those for the A3VCPU. The operation processing is described in the summary below.

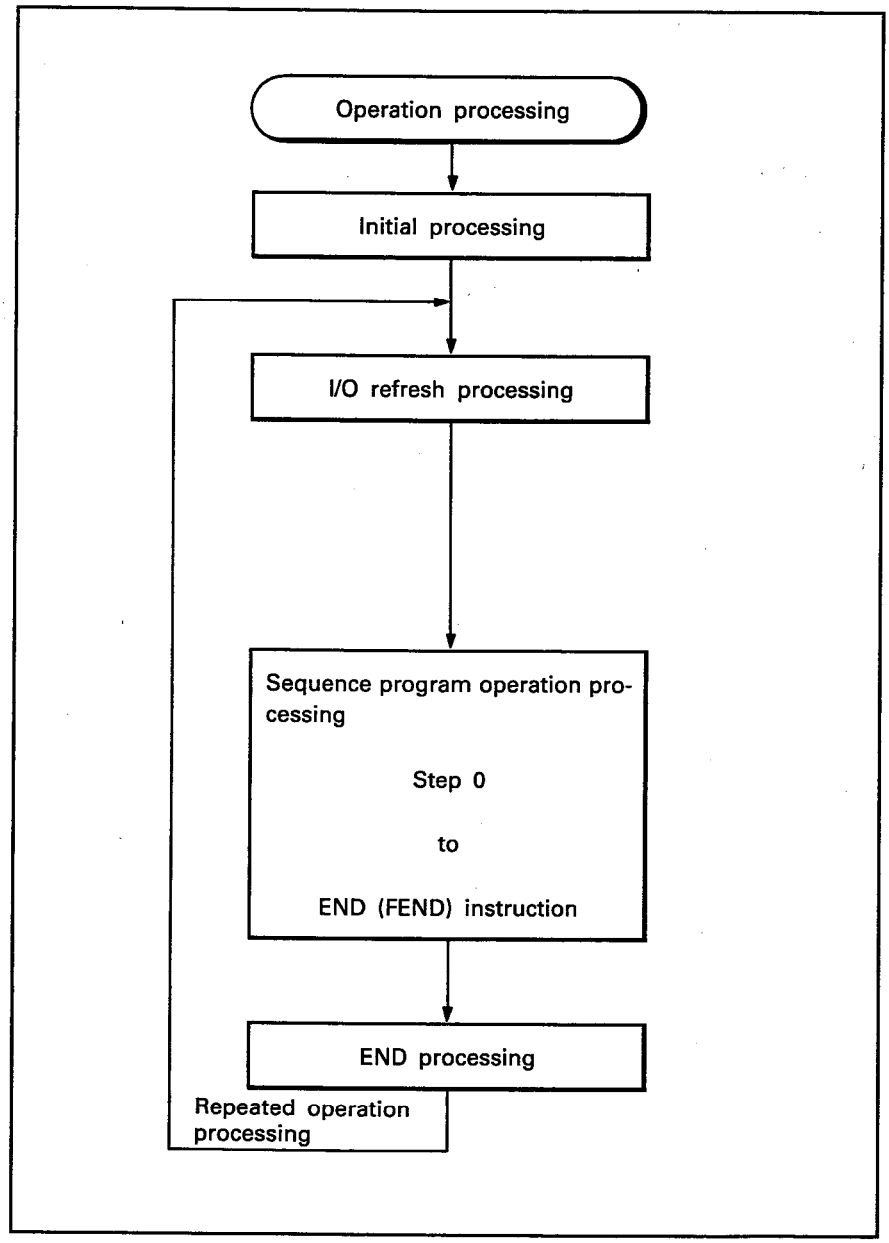

Fig. 4.1 Operation Processings

4.2.1 Repeated operation processing

Sequence programs are written by the peripheral and stored to the A3VCPU user program area. For the three A3VCPU modules, write the same sequence programs and parameters.

The A3VCPU reads the required program sequentially from the user program area and performs the repeated operation processing in order of step 0 to the END (FEND) instruction.

(1) Stored program system

Sequentially reads and operates the program stored in the user program area.

(2) Scanning

Operates the program in order of step numbers from step 0 to the END (FEND).

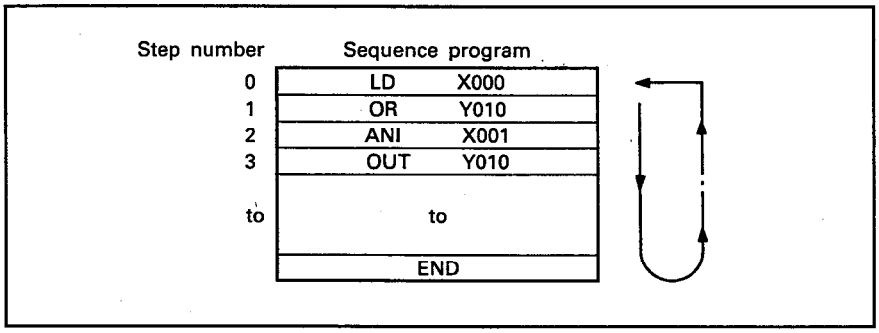

Fig. 4.2 Sequence Program Operation Processing

4.2.2 Initialization

Initialization indicates the processing which is required to begin sequence program operation processing.
Initialization performs the processing for the I/O module initialization, clears data memory, assigns I/O addresses, activates the self-diagnosis function and performs other similar operations when power is applied or a reset operation is performed by the RESET switch.
Note that resetting an A3VCPU during majority operation causes and alarm to be produced with that CPU; it is dropped from the system operation.

4.2.3 END processing

END processing indicates the processing which returns operations to step 0 in the repeat operation processing.
After the A3VCPU has executed the END (FEND) instruction, the END processing performs the processing for the update of the timer/counter current value and turning the contact ON, the self-diagnosis and constant scan processing, the sampling trace, and other processing operations. When these operations are completed, processing returns to step 0.
Refer to section 4.2.4 for more detailed description of the processing for the timer/counter, constant scan and self-diagnosis function.

4.2.4 Timer processing

The PC CPU uses up timers which increment their present values according to the duration of measurement.

- The 100ms timer timing can be set between 0.1 and 3276.7s in 100ms increments.
- The 100ms timer timing can be set between 0.01 and 327.67s in 10ms increments.
- The 100ms retentive timer retains its present value even if its coil is switched off. The timing can be set between 0.1 and 3276.7s in 100ms increments.

The timer processing method is described below.

(1) Timer present value and contact status update

With continuity in front of a timer coil, the timer present value and contact status are updated after the execution of the [END] (or FEND) instruction and the timer contacts close after the timer has timed out.

(a) 100ms, 10ms timers

When the continuity is removed from in front of the timer coil, the present value is reset to 0 and the timer contacts open.

(b) 100ms retentive timer

When the continuity is removed from in front of the timer coil, the present value update is stopped but the present value is retained.

(2) [RST] T[ ] instruction executed ([Rest] instruction)

When the timer is reset by the [RST] T[ ] instruction, the present value is reset to 0 and the timer contacts open. The retentive timers retain their present value and contact status, and are reset using the [RST] T[ ] command.

(3) [OUT] T[ ] jumped by [CJ] instruction, etc.

If the [OUT] T[ ] instruction is jumped after the timer has started timing, it continues to time. The contacts are closed when the timer times out.

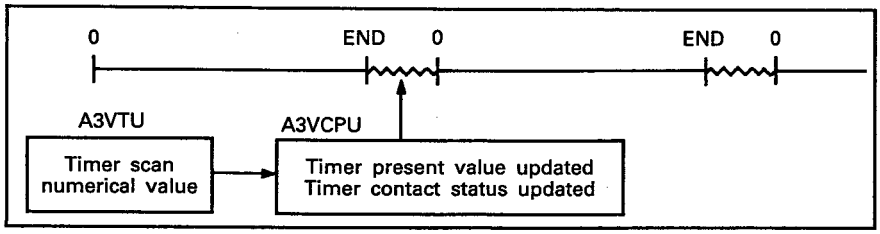

Fig. 4.3 Timer Processing

REMARKS

Timer accuracies are as follows. For further details, refer to the ACPU Programming Manual.

Timer	Scan Time T	Refresh Input
10ms	T < 10ms	+2 scan time to 0
10ms	T ≧ 10ms	
100ms, 100ms retentive	T < 100ms	
100ms, 100ms retentive	T ≧ 100ms	

(4) Present value update timing and accuracy

(a) The timer accuracy is equal to a value of +2 scan time and is unrelated to the timer and scan time.

(b) The diagram below shows the present value update timing and accuracy when a 10ms timer is used in a program in which the scan time is set to longer than 10ms.

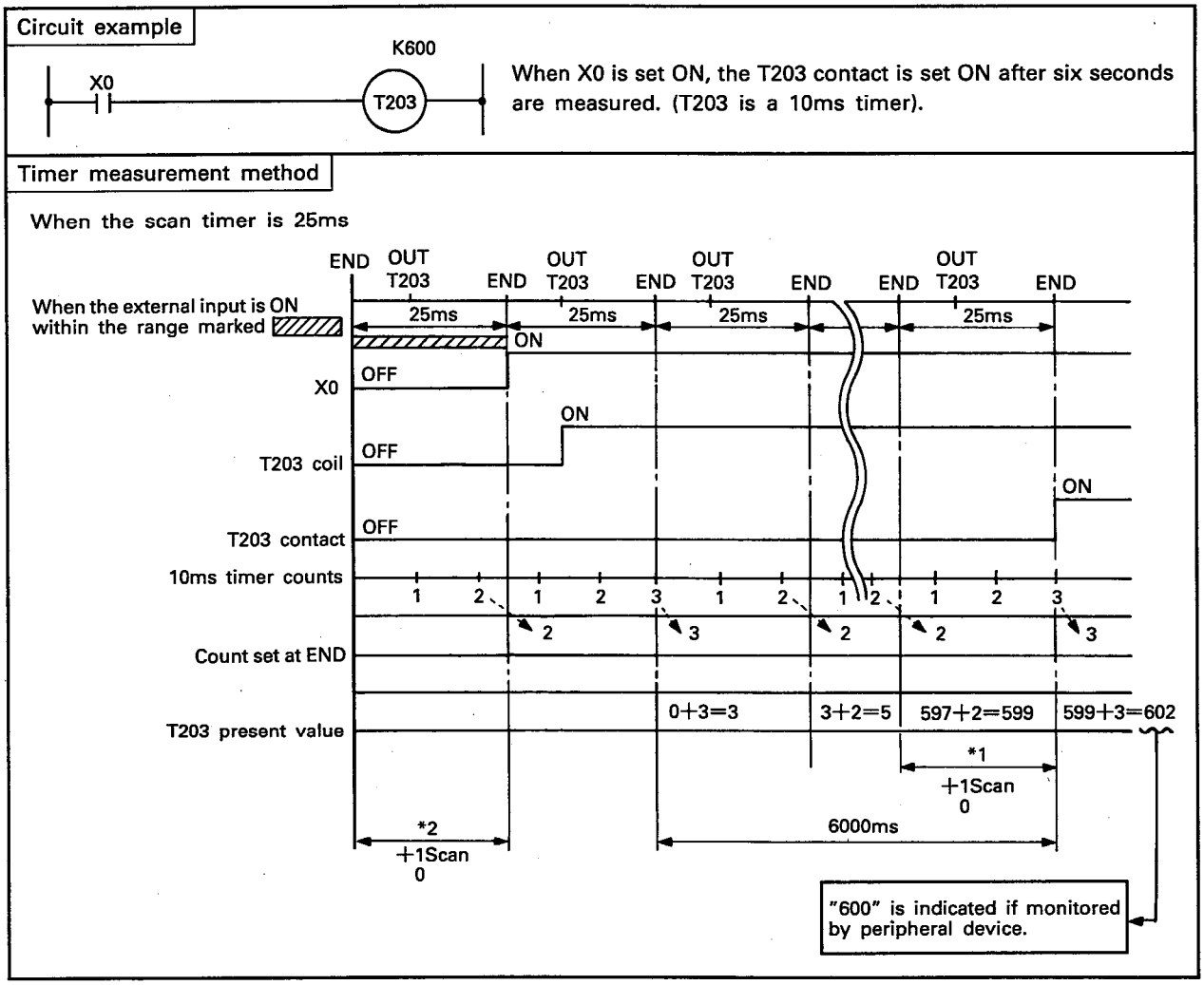

Fig. 4.4 Timer Measurement Method

The errors described below are present in the time-up time for the T203 10 ms timer as shown in Fig. 4.4.

*1 ··· The 10 ms timer counting error (+1 scan time)

*2 ··· The error resulting from timing that sets the timer input condition ON and the OUT T□ instruction position in the program (+1 scan time).

The accuracy is +2 scan time (+0.05 seconds in Fig. 4.4).

(c) The contacts of the "time-up" timer remain ON till the point the END instruction is executed, even if the coil of the timer is set OFF. It is set OFF when the END instruction is executed.

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4.2.5 Counter processing

The PC CPU uses up counters which increment their present values on the leading edge of an input signal.
Counting is performed by the three A3VCPU modules. The A3VTU does not contribute to the counting. The counter is used in the main routine program or sub-routine program. The counter processing is described below.

(1) The counter present value update and contact ON/OFF

(a) The counter coil is set ON or OFF by the OUT C□ instruction. The present value is updated when the coil rising edge is detected; when the count value is incremented to the same value as the set value, the counter contact is set ON.

(b) Counting is not executed while the coil stays ON.

(c) The count present value is updated and the counter contact is set ON/OFF after the END (FEND) instruction is executed.

(d) The counter value is not cleared even if the coil is set to OFF i.e., the input conditions, which turn the counter coil ON/OFF are set to OFF.

(2) RST C□ instruction executed

When the counter is reset by the RST C□ instruction, the present value is reset to 0 and the counter contacts open. The counters retain their present value and contact status even if the counter coil is switched off.

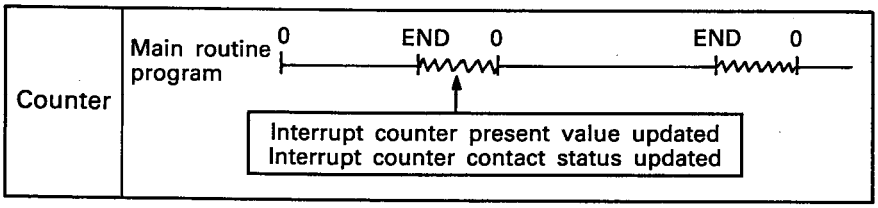


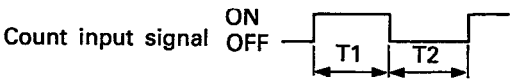
Fig. 4.5 Counter Processing

REMARKS

The maximum counting speed of the counter depends on the scan time. Counting is only possible if the input condition is on for more than one scan time. For further details, see the ACPU Programming Manual.

$$\text{Maximum counting speed } Cmax = \frac{n}{100} \times \frac{1}{ts} \text{ (times/sec)}$$

where, n = duty (%)
Duty is the ratio of the input signal's on time to off time as a percentage.



If $T1 \leqq T2$ $\quad n = \frac{T1}{T1+T2} \times 100$ (%)

If $T1 > T2$ $\quad n = \frac{T2}{T1+T2} \times 100$ (%)

ts: Program scan time (sec)

POINT

(1) Since the A3VTS does not have the interrupt program execution function, the interrupt counter cannot be used. Although parameter settings can be used to assign the interrupt counter, the interrupt counter, if used in the main routine program, cannot execute counting.
(An error will not be generated even if an interrupt counter is used in a program.)

(3) Count value update timing

An explanation of the count value update timing is given based on the circuit example shown in the following figure.

Circuit example

C3 is set ON when OFF to ON event of X5 is counted two times.

Counter operation

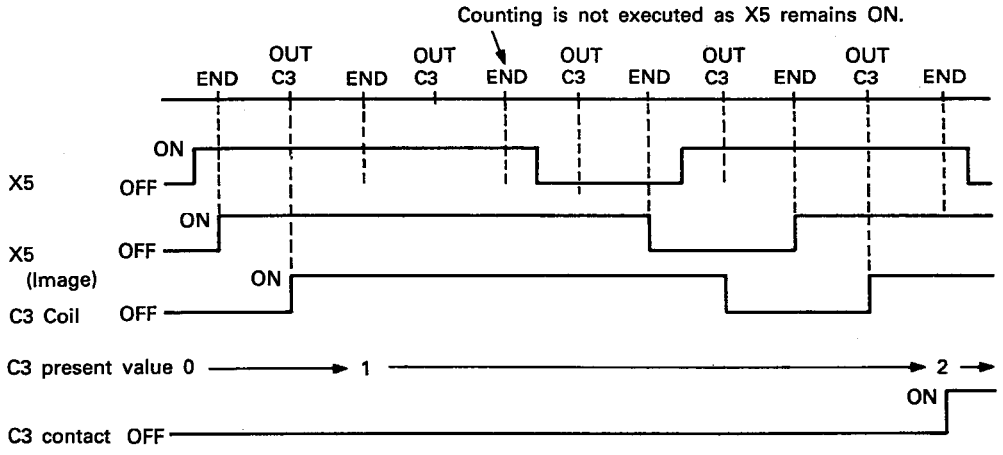


Fig. 4.6 Counter Operation

4.2.6 Operation processing at instantaneous power failure occurrence

The A3VTU or A3VCPU module detects any instantaneous power failure when the input line voltage to the power supply module falls below the defined value.
If the instantaneous power failure time is within the allowable value (20ms), the A3VTU or A3VCPU module performs instantaneous power failure processing as described below:

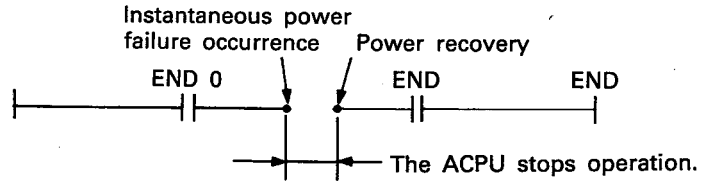
(1) Instantaneous power failure within 20ms

(a) The operation processing is stopped with the output retained.

(b) The operation processing is resumed when normal status is restored.

(c) The watch dog timer (WDT) keeps timing while the operation is at a stop. For instance, if the WDT and scan time settings are 200ms and 190ms respectively, an instantaneous power failure of 20ms will result in a WDT error.

Operation processing at occurrence of instantaneous power failure



(2) Instantaneous power failure over 20ms

The A3VTS system is activated at the initial start.
This is the same operation processing as performed when power is applied or when the RESET switch is used.

4.2.7 RUN, STOP, PAUSE operation processings

The A3VTS system is operated in either of the RUN, STOP and PAUSE states as described below.
The selection of each operating status is determined by the status received from the key switch settings of the A3VTU and each A3VCPU in combination with indications received from the peripheral device. Refer to Chapter 5 for further details regarding the operating status that arise from these combinations.
This section describes the contents of operation processing in each operation status.

(1) RUN operation processing

RUN indicates repeated operation of the sequence program in order of step 0 to END (FEND) instruction.
When the CPU is set to RUN, the output status at the time of STOP is provided in accordance with the STOP RUN output mode setting in the parameter.
The processing in Fig. 4.7 is repeated until RUN is switched to another state.

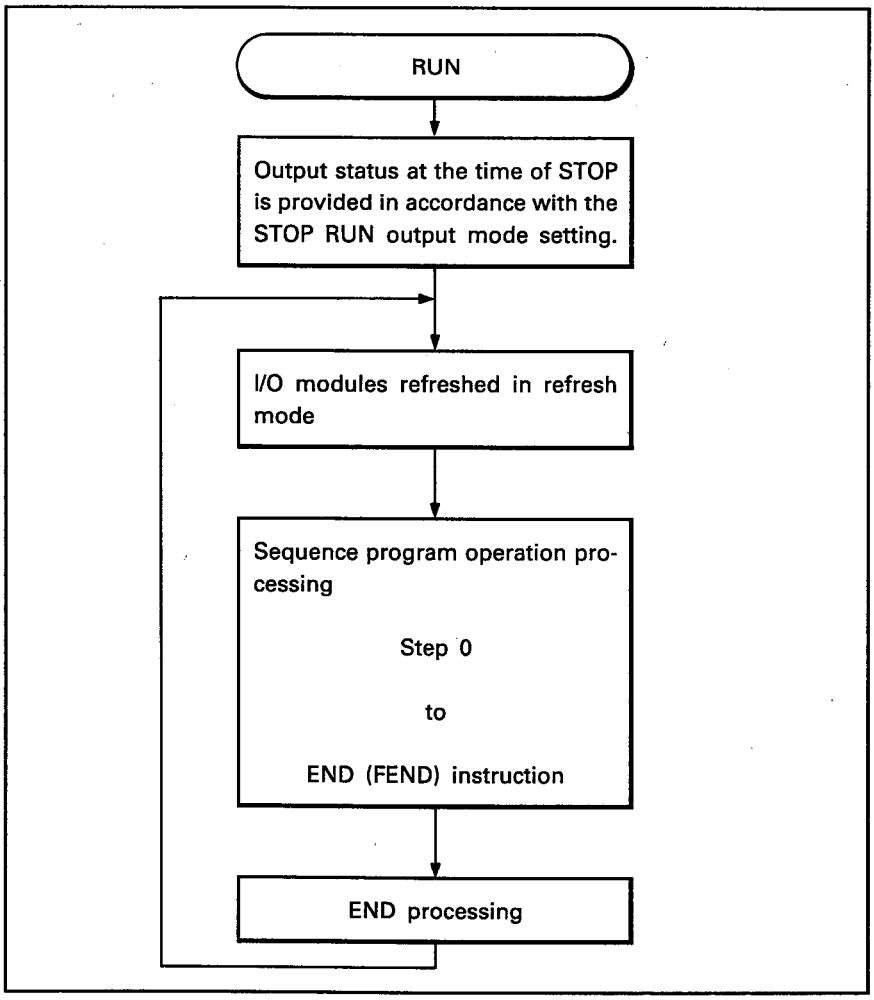


Fig. 4.7 RUN Operation Processing

(2) STOP operation processing

STOP indicates a stop of the sequence program operation by using the RUN/STOP switch or remote STOP (Section 4.11.5). When the CPU is set to STOP, the output status is saved and all outputs are switched off. Data other than the outputs (Y) is retained.
The processing in Fig. 4.8 is repeated until STOP is switched to another state.

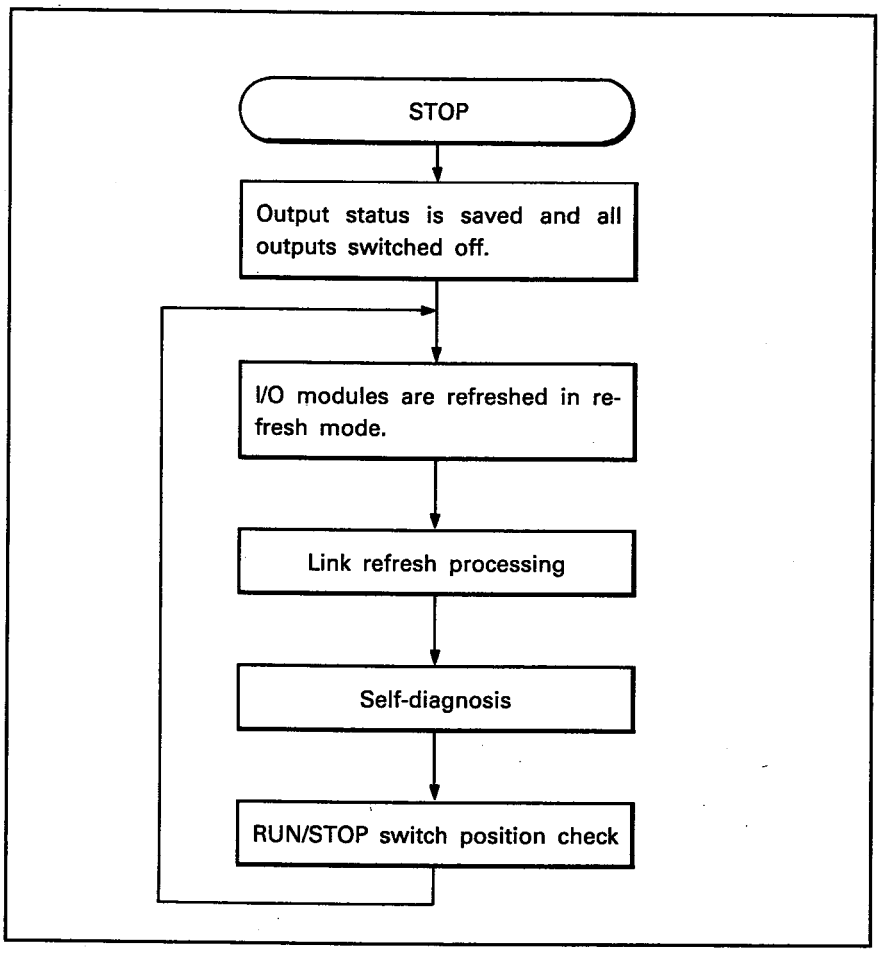


Fig. 4.8 STOP Operation Processing

REMARKS

When the Run/Stop key switch is placed in the STEP RUN position, the A3VCPU operates as though the switch is placed in the STOP position.

(3) PAUSE operation processing

PAUSE indicates a stop of the sequence program operation with the output and data memory statuses retained.
The PC CPU can set to PAUSE state in accordance with Section 4.9.
The processing in Fig. 4.11.6 is repeated until PAUSE is switched to another state.

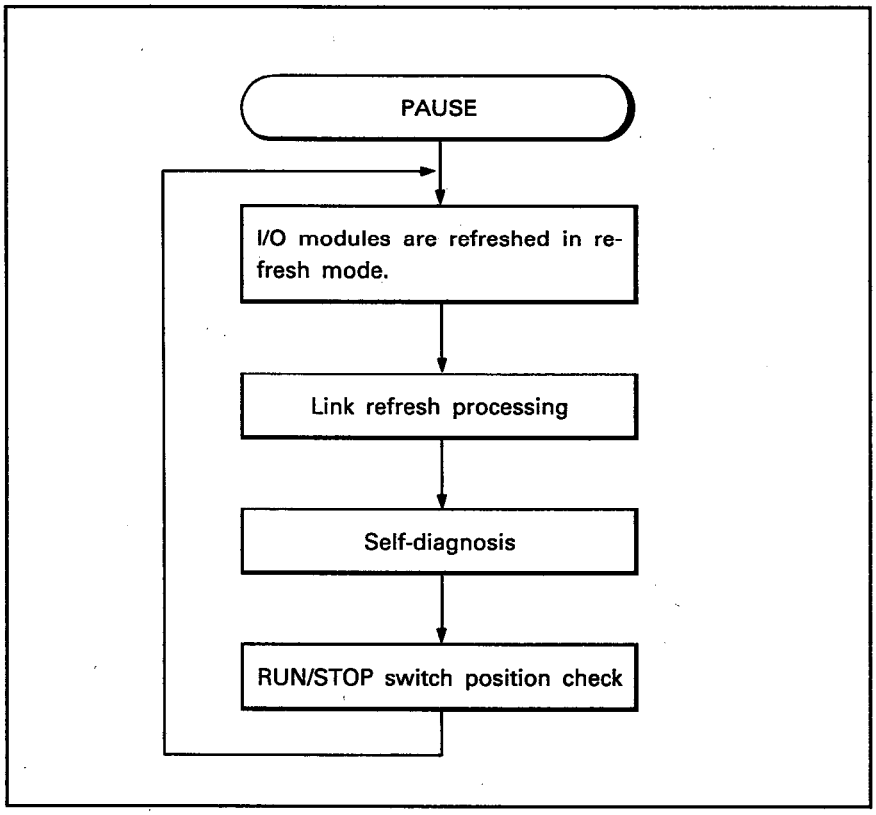


Fig. 4.9 PAUSE Operation Processing

(4) Each operation processing are shown in Table 4.2.

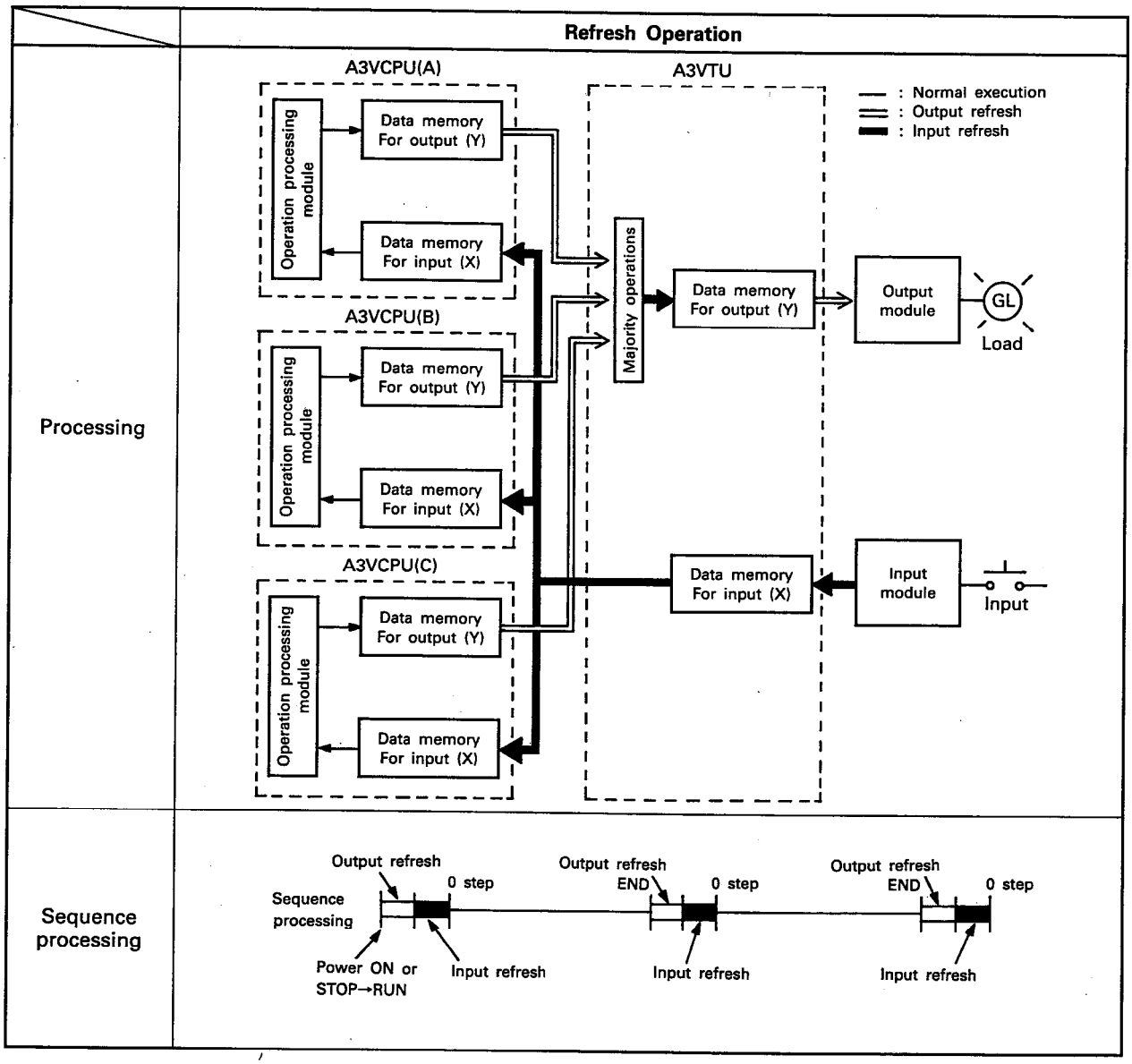
Processing / RUN /STOP Switch	I/O Refresh (in refresh mode)	Self-Diagnosis	Timer/ Counter Present Value and Contact Status Update	Constant Scan Processing (with constant scan set)	Link Refresh Processing	Sampling Trace Processing	RUN/ STOP Switch Position Check
RUN (END processing)	Executed	Executed	Executed	Executed	Allowed	Executed	Executed
STOP	Executed	Executed	—	—	Allowed	—	Executed
PAUSE	Executed	Executed	—	—	Allowed	—	Executed

Table 4.2 Processing During Program Operation Stop

4.3 I/O Control

The A3VTS system uses I/O image refresh for I/O processing. Refresh processing fetches external ON/OFF data (X input data) or outputs ON/OFF data (Y output data) in one batch after the END instruction has been executed.
Since the ON/OFF status of input (X) does not change during one scan of the sequence program, the program is executed throughout the scan under the same conditions.
A detailed explanation of the refresh processing operation is shown below.

Refresh processing operation



REMARKS

When majority operations are not performed, processing is performed between one of the operating A3VCPU modules and the A3VTU.

(1) Input refresh

The A3VTU reads the input data from the input module in one batch before executing the 0 step. The input data is stored in the A3VTU data memory for input (X), while the A3VTU stores the input data in the data memory for input (X) of each of the A3VCPUs at the same time.

(2) Output data refresh

The A3VTU reads the data from the data memory for output (Y) of each A3VCPU before executing the 0 stop. Majority operations are performed with the results stored in the A3VTU data memory for output (Y) while for output in one batch to the output module at the same time.

(3) Execution of input contact instruction

The input data is read from the A3VCPU data memory for input (X) and the sequence program is executed.

(4) Execution of output contact instruction
The output data is read from the A3VCPU data memory for output (Y) and the sequence program is executed.

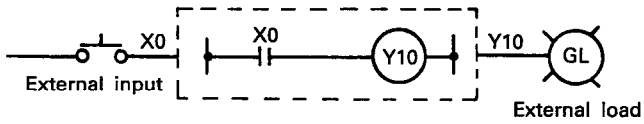
(5) Execution of output OUT instruction

The sequence program operation result is stored in the A3VCPU data memory for output (Y). When the Y of the rear of input (X) is used as an internal relay, processing becomes the same as that for internal relay M. Thus, when the coil is set ON by the program, the contact is set ON if used in the rest of the program. This is unrelated to refresh processing.

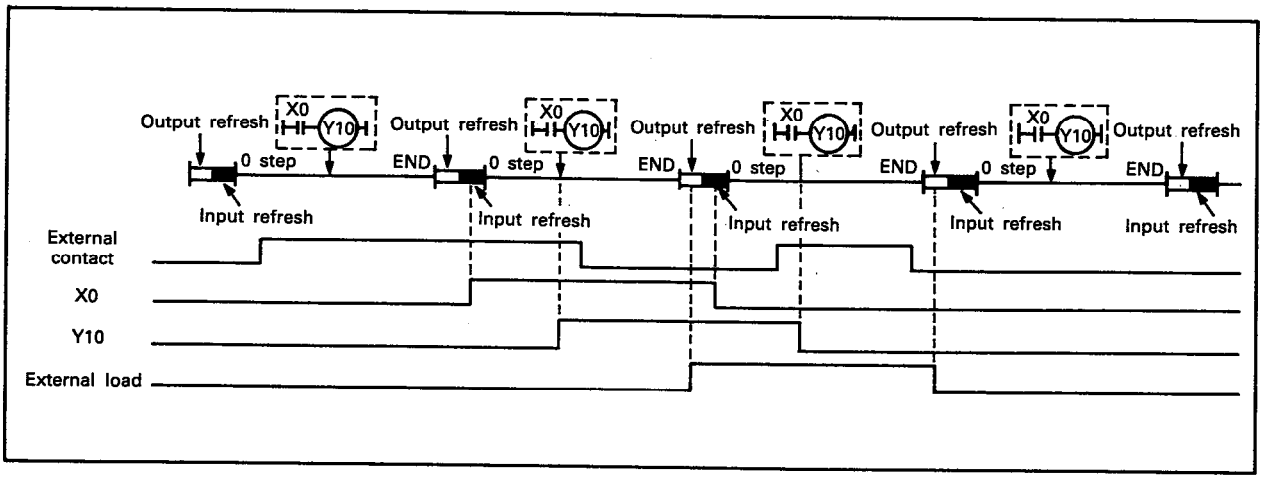
(6) Operation delay

Changes in the output modules are delayed 1 to 2 scans compared to changes in the input signal. Note that the delay is increased by 1 to 2 scans plus 400ms when operation is restored after repairing or replacing a malfunctioning A3VCPU.
I/O timing is described in the following example.

Circuit example



I/O timing



POINT

Some I/O modules may be directly accessed as in direct mode by using the SEG instruction (partial refresh). For details, refer to the ACPU Programming Manual.

4.4 Programming Languages

Any of the following languages may be used:

(1) Relay symbolic language

Used to represent relay symbols. Allows programming nearly in the form of relay control sequence ladders.

(2) Logic symbolic language

Used to write microcomputer programs based on the assembly language.
Program processing representations are separated into the instruction, source and destination parts.

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4.5 Number of Inputs/Outputs and I/O Addresses

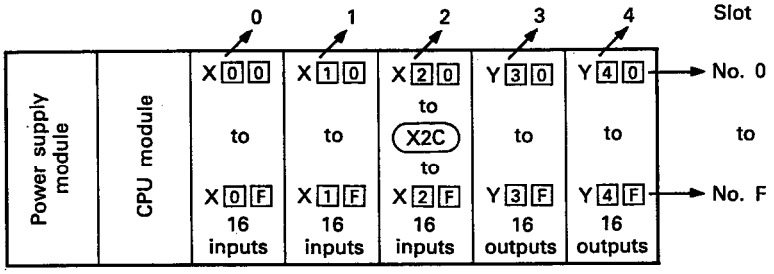
4.5.1 Number of inputs/outputs

The number of inputs/outputs indicates the number of I/O devices which can be connected to and controlled by the PC. The number of I/O depends on the CPU module used.
Inputs and outputs are devices used to transfer data between the PC and external equipment.
The input (X) is provided by an external device (e.g. limit switch, pushbutton) connected to the input module and is used in the sequence program with an ON/OFF signal.
The output (Y) is used to provide a program operation result to an external device (e.g. solenoid, magnetic switch) connected to the output module.

4.5.2 I/O addresses

I/O addresses indicate I/O module addresses for use in the sequence program and are represented in hexadecimal.
I/O addresses depend on the positions of I/O modules loaded on the base unit.

In the following example, X2C indicates that the corresponding input module is loaded in No. C, slot 2. (All I/O modules are 16 points.)



Correspondence between hexadecimal and decimal is as follows:

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

4.5.3 I/O assignment

I/O addresses are automatically allocated by the A3VTU in accordance with the I/O module positions on the base unit. User may define I/O assignment using the peripheral.

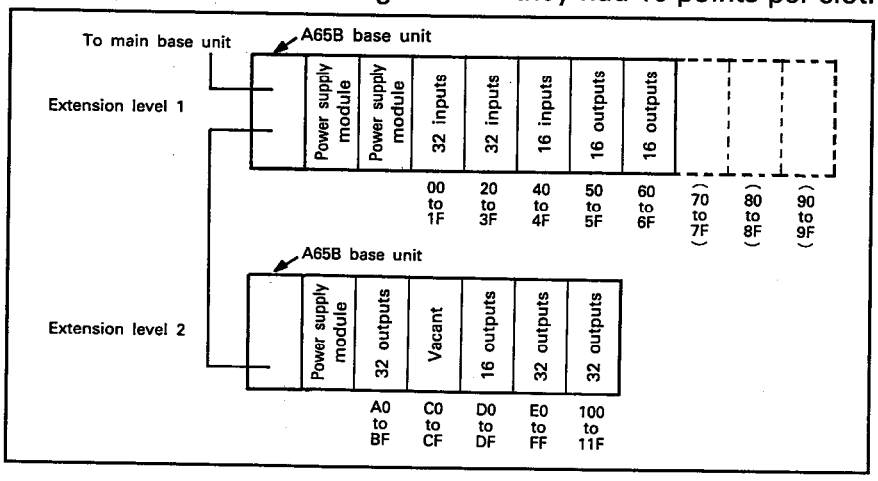
(1) No parameter I/O assignment

(a) Assign I/O numbers in order of extension base stage setting numbers (as opposed to order of extension cable connection).

(b) Assign I/O numbers to the main base and extension base(s) on the assumption that each base has 8 slots. (The final 3 slots on a 5 slot base must be accounted for and represent empty I/O slots).

(c) Assign 16 points to an empty slot.

(d) When a designated setting jumps expansion stage number settings, the "jumped number of stages × 8 slots portion" are all assigned as if they had 16 points per slot.

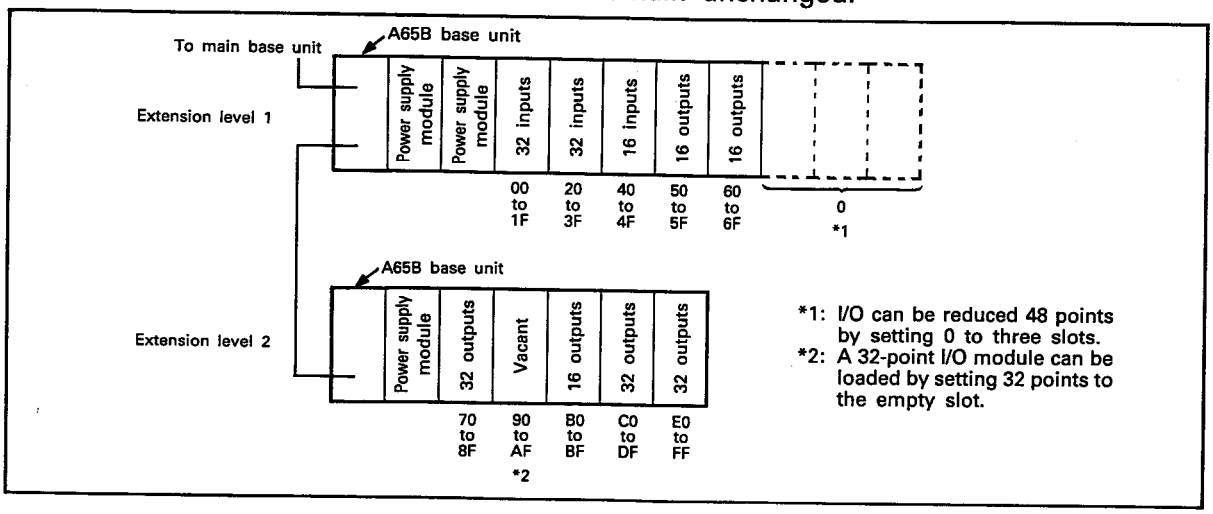


(2) I/O assignment has been made by the peripheral

I/O assignment by using the peripheral is optional. The following features can be achieved by this I/O assignment.

(a) Economization on I/O occupied by empty slot
Inputs/outputs occupied can be economized by setting 0 to empty slots, e.g. I/O occupied can be reduced 48 points by setting 0 to the three empty slots of the A35B base unit.

(b) I/O reservation
32, 48 or 64 points can be reserved for future system expansion. By this reservation, the sequence program can be easily added to or modified as the I/O module addresses remain unchanged.



4.6 Watch Dog Timer (WDT)

Internal timer used to detect any error of the PC's repeated operation function.
Two types of watchdog timers are employed in the system. One type is operated by the A3VTU and the other type by the A3VCPU. The two types of watchdog timers are described below.

(1) The A3VTS operated watchdog timer
  (a) Watchdog timer function
    The A3VTU monitors its own processing time. When a hardware malfunction occurs or noise causes malfunction or endless loop operation, the watchdog timer generates an error energizing an alarm and terminating computer processing.
  (b) System operation after watchdog timer error
    When the A3VTU watchdog timer generates an error, the operational status of the A3VTS system becomes the following.
    - The A3VTU and A3VCPU operation execution stops and all outputs are set OFF.
    - The message "WDT ERROR" is displayed on the LED display located on the front panel of the A3VTU. Nothing is displayed on the LED display located on the front panel of the A3VCPU.

(2) The A3VCPU operated watchdog timer
  (a) Watchdog timer function
    Default value of the A3VCPU watchdog timer setting is 200 ms. The value can be varied 10ms increments between 10 ms to 2,000ms using parameter settings.
    The watchdog timer functions in the following manner. The watchdog timer observes the execution time required for one scan of program. The watchdog timer generates an error if the A3VCPU hardware malfunctions, or the scan time of the sequence program exceeds a set value. An alarm is output and computer processing is terminated. However, when majority operations are performed, the A3VTS system continues to operate as long as one or more A3VCPU modules are operating normally.
  (b) Watchdog timer reset timing
    The watchdog timer is reset after the [END] instruction is executed when the A3VCPU operations are normal (the scan times are within the designated values).
  (c) Watchdog timer error
    The watchdog timer generates two error codes, "22" and "25". Error code "22" is generated if the [END] instruction is executed after the set time has elapsed.
    Error code "25" is generated if an endless loop (when an endless loop has been created in the [CJ] instruction, etc.) is performed and the set time has elapsed without execution of the [END] instruction.

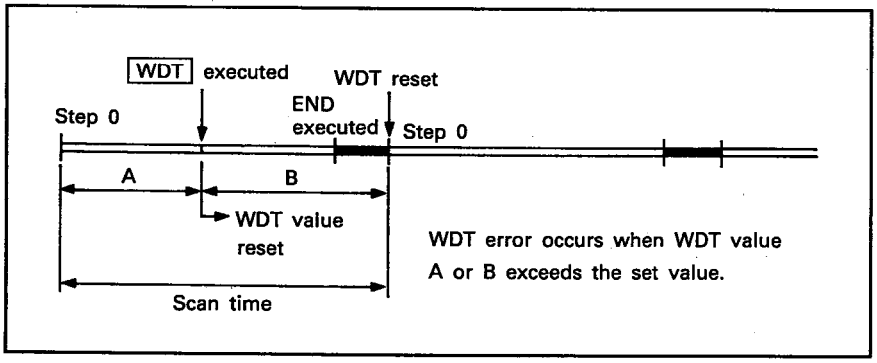
(d) Operation at WDT error occurrence

When the A3VCPU watchdog timer generates an error, the operational status of the A3VCPUs becomes the following.
- A3VCPU operation is stopped.
- The RUN LED on the A3VCPU front panel flickers.
- "WDT ERROR" is displayed on the LED in the A3VCPU front panel.

However, when majority operations (with two or three A3VCPU modules) are performed, the A3CPU system continues to operate as long as one or more A3VCPU modules are operating normally.
If a "WDT ERROR" is generated by all the A3VCPU modules, the operational status of the A3VTS system becomes the following.
- The A3VCPU enters the previously described status.
- The RUN LED display located on the front panel of the A3VTU module flickers but nothing is displayed on the LED display.
- System operation is stopped and all outputs are set to OFF.

(e) Resetting method

The WDT present value is reset when the WDT reset (WDT) instruction is executed in the sequence program.
The WDT restarts timing at 0.
Any scan time stored in D9017 to 9019 is not reset if the WDT instruction is executed.



POINT

Avoid setting scan time to values exceeding 2000ms, since a "WDT ERROR" is generated even if a WDT instruction is executed in the sequence program if it exceeds 2000ms.

(3) If the WDT error has occurred, check the error definition according to Section 13, reset the CPU, and remove the error cause.

4.7 Memory Capacity

The memory capacity indicates the memory capacity of the user memory which can be created by the user's sequence program, comments, etc.
The contents of data stored in the memory cassette are described below in item (1). The amount of memory to be used for each type of data and whether the data is to be used or not can be set by parameter settings.
(When no parameters are set, only parameters and the main sequence program can be created and stored.)
The capacity of the memory cassettes should be taken into account when setting the capacity of each memory. Refer to Section 4.11 "Parameters" and Section 9.2 for details regarding the maximum memory capacity that can set using each data parameter and the configuration of each data.

Two types of data are handled in the CPU module. One is data that is stored in the memory cassette and the other is data stored in the CPU module. These different types of data are described below.

1) Memory cassette data

- Parameter
- Main sequence program
- Main microcomputer program
- Sub sequence program
- Sub microcomputer program
- Sampling trace
- Status latch
- File register
- Comment

2) CPU data

- Input (X)
- Output (Y)
- Data register (D)
- Internal relay (M)
- Latch relay (L)
- Step relay (S)
- Timer (T)
- Counter (C)
- Link relay (B)
- Link register (W)
- Annunciator (F)
- Accumulator (A)
- Index (V, Z)
- Pointer (P)
- Special relay (M)
- Special register (D)

4.8 Devices

Devices indicate contacts, coils, timers, etc. used in the PC program operation.
Table 4.3 indicates the devices used with the PC.
For the devices indicated by an asterisk ✳, their use is enabled or usable range assignment can be changed by setting parameters with a peripheral device.
Set parameters corresponding to the system in which the device is used or contents of the program. (For parameters, see Section 4.10.)

Device			Application Range (Number of points)		Explanation
	X	Input	X, Y0 to 7FF (Number of Xs + Ys = 2048)		Provides PC command and data from external device, e.g. pushbutton, select switch, limit switch, digital switch.
	Y	Output			Provides program control result to external device, e.g. solenoid, magnetic switch, signal light, digital display.
	M	Special relay	M9000 to 9255 (256)		Predefined auxiliary relay for special purpose and for use in the PC.
✳		Internal relay	M0 to 999 (1000)	Number of Ms + Ls + Ss = 2048	Auxiliary relay in the PC which cannot be output directly.
✳	L	Latch relay	L1000 to 1024 (1024)		Auxiliary relay in the PC which cannot be output directly. Backed up during power failure.
✳	S	Step relay	Can be used by setting the parameter (0)		Used in the same manner as an internal relay (M), e.g. as a relay indicating the stage number of a step-by-step process operation program.
	B	Link relay	B0 to 3FF (1024)		Internal relay for data link which cannot be output. May be used as an internal relay if not set for link initial data.
	F	Annunciator	F0 to 255 (256)		Used to detect a fault. When switched on during RUN by a fault detection program, stores a corresponding number in special register D.
✳	T	100ms timer	T0 to 199 (200)		Up timers available in 100ms, 10ms and 100ms retentive types.
		10ms timer	T200 to 255 (56)		
		100ms retentive timer	Can be used by setting the parameter. (0)		
✳	C	Counter	C0 to 255 (256)		Up counters.
	D	Data register	D0 to 1023 (1024)		Memory for storing PC data.
		Special register	D9000 to 9255 (256)		Predefined data memory for special purpose.
	W	Link register	W0 to 3FF (1024)		Data register for use with data link.
✳	R	File register	Can be used by setting the parameter. (0)		Extends data register using user memory area.
	A	Accumulator	A0, A1 (2)		Data register for storing the operation results of basic and application instructions.
	Z	Index register	Z (1)		Used to modify devices (X, Y, M, L, B, F, T, C, D, W, R, K, H, P).
	V		V (1)		
	N	Nesting	N0 to 7 (8 levels)		Indicates the nesting of master controls.
	P	Pointer	P0 to 255 (256)		Indicates the destination of the branch instruction (CJ, SCJ, CALL, JMP).
	K	Decimal constant	K-32768 to 32767 (16-bit instruction)		Used to specify the timer/counter set value, pointer number, interrupt pointer number, the number of bit device digits, and basic and application instruction values.
			K-2147483648 to 2147483647 (32-bit instruction)		
	H	Hexadecimal constant	H0 to FFFF (16-bit instruction)		Used to specify the basic and application instruction values.
			H0 to FFFFFFFF (32-bit instruction)		

Table 4.3 Device List

REMARKS

The step relay (S) may be used in the same manner as the internal relay (M). For instance, the step relay comes in useful when writing a program which has two functions or applications, i.e. the step relay can be used specifically in accordance with the function or application, independently of the internal relay.

4.9 Self-Diagnosis

The CPU self-checks for error at power on and during run. When any error is detected, the CPU indicates the error and stops operation to prevent PC fault and ensure reliable operation. This section describes the two self-check functions of the A3VTS system. One is used for diagnosis of the A3VCPUs and the other of the A3VTUs.
Refer to the Error Code Table in Section 13.1 for details regarding the error processing in the CPU and error cancellation methods.

4.9.1 A3VCPU self-diagnosis

Each A3VCPU module independently performs self- diagnosis in relation to each A3VCPU and the A3VTU. The [redacted] in the table indicates the contents of what is being checked by the A3VCPU in relation to the A3VTU. The number shown in the No. column indicates the error priority level for the related check. Lower numbers indicate higher priority. Priority for errors having the same numerical value is determined by the timing of error generation with errors generated earlier having a higher priority than those generated later.

No.	Diagnosis	Diagnosis Timing	A3VCPU Operation Status	RUN LED Status	A3VCPU Error Display	Error Code (Contents of D9008)
1	A3VCPU executes endless loop	At any time	Stop	Exting-uishes	WDT ERROR	25
2	A3VTU check	At any time		Flickers	A3VTU ERROR	5
	DP RAM check	When power is turned on (A3VTU, A3VCPU) At reset (A3VTU, A3VCPU)			DPRAM ERROR	6
3	Instruction code check	When each instruction is executed			INSTRCT. CODE ERR.	10
	Parameter setting check	When power is turned on or at reset (A3VTU, A3VCPU) When STOP or PAUSE is switched to RUN			PARAMETER ERROR	11
	Missing END instruction check	When STOP or PAUSE is switched to RUN			MISSING END INS.	12
	Instruction execution not possible	When the [CJ], [SCJ], [JMP], [CALL (P)] and [CHG] instructions are executed. When STOP or PAUSE is switched to RUN			CAN'T EXCUTE (P)	13
	Instruction execution not possible	When the [IRET] instruction is executed			CAN'T EXCUTE (I)	15
	CHK instruction format check	When STOP or PAUSE is switched to RUN			CHK FORMAT ERR.	14
	Memory cassette presence check	When the power is turned on or at reset (A3VTU, A3VCPU)			CASSETTE ERROR	16
	RAM check	When the power is turned on or at reset (A3VTU, A3VCPU)			RAM ERROR	20
	Operation circuit check	When the power is turned on or at reset			OPE. CIRCUIT ERR.	21
	Watchdog timer	When the [END] instruction is executed			WDT ERROR	22
	END instruction not executed	When the program [END] step is executed			END NOT EXCUTE	24
4	Special function module error	When the [FROM] and [TO] instructions are executed	Run/Stop	Lights/Flickers	SP. UNIT ERROR	46
	Operation check error	When each instruction is executed	Run/Stop	Lights/Flickers	OPERATION ERROR	50
5	Low battery voltage check	At any time	Run	Lights	BATTERY ERROR	70

Table 4.4 A3VCPU Self-Diagnosis

REMARKS

When operating in the multiplex system, the system can continue operations as long as there is one or more A3VCPU module operating normally. The malfunctioning A3VCPU is dropped from system operation.

4.9.2 A3VTU self-diagnosis

There is self-diagnosis that is conducted by the A3VTU on itself and that which is based on error messages from the dual power supply modules. Self-diagnosis is conducted on the three A3VCPUs and A3VTUs. The contents of the diagnosis is shown in Table 4.5.

The [ ] in the table indicates the contents of what is being checked by the A3VTU in relation to the A3VCPU. The number shown in the No. column indicates the error priority level for the related check. Lower numbers indicate higher priority. Priority for errors having the same numerical value is determined by the timing of error generation with errors generated earlier having a higher priority than those generated later.

No.	Diagnosis	Diagnosis Timing	A3VCPU Operation Status	RUN LED Status	A3VCPU Error Display	Error Code (Contents of D9009)
1	RAM check	When the power supply is turned on or the A3VTU is reset	Stop	Flickers	RAM ERROR[ ] Any number from 1 to 5	100
	Control bus check	When the FROM and TO instructions are executed			CONTROL-BAS ERR.	40
	Special function module check	When the FROM and TO instructions are executed			SP. UNIT DOWN	41
	Link module check	When the power supply is turned on or the A3VTU is reset When STOP or PAUSE is switched to RUN			LINK UNIT ERROR	42
	I/O interrupt check	When the OS link interrupt program operates due to an A3VTU malfunction			I/O INT.ERROR	43
	Special function module assignment check	When the power supply is turned on or the A3VTU is reset When STOP or PAUSE is switched to RUN			SP. UNIT LAY. ERROR	44
	Majority circuit check	When the power supply is turned on or the A3VTU is reset			CIRCUIT ERROR	101
	Data transmission halt check	When the power supply is turned on or the A3VTU is reset When STOP or PAUSE is switched to RUN When the A3VCPU restore processing is performed			SOURCE CPU DOWN	102
	ROM check	When the power supply is turned on or the A3VTU is reset			ROM ERROR	——
	WDT check	At any time		Extinguishes	WDT ERROR	25
	Link station number setting check	When the power supply is turned on or the A3VTU is reset		Flickers	STATION No. [ ]*[ ]	190
2	Module check	At any time (other than during repair)	Run/Stop	Lights/ Flickers	UNIT VERIFY ERR.	31
	Output module fuse blown check	At any time (other than during repair)			FUSE BREAK OFF	32
	Link station number setting check	When the link module is booted after replacement	Run	Lights	STATION No. ERR	191
3	CPU A time check	When the instructions in Table 13.3 are executed	Operates if CPU switching is Possible/Stops if CPU switching is not possible	Lights/ Flickers	TIME OVER CPU A	110
	CPU B time check				TIME OVER CPU B	111
	CPU C time check				TIME OVER CPU C	112
	CPU A majority decision check	At any time when majority operations are performed			VOTE ERROR CPU A	120
	CPU B majority decision check				VOTE ERROR CPU B	121
	CPU C majority decision check				VOTE ERROR CPU C	122
	Dual module operation verify check	At any time when independent operations are performed	Operation	Lights	VERIFY ERROR	140
	CPU A handshake check	At any time	Operates if CPU switching is Possible/Stops if CPU switching is not possible	Lights/ Flickers	ERROR CPU A[ ] Status number of CPU A	130
	CPU B handshake check				ERROR CPU B[ ] Status number of CPU B	131
	CPU C handshake check				ERROR CPU C[ ] Status number of CPU C	132

Table 4.5 A3VTU Self-Diagnosis (Continue)

No.	Diagnosis	Diagnosis Timing	A3VCPU Operation Status	RUN LED Status	A3VCPU Error Display	Error Code (Contents of D9009)
4	F-loop link check	At any time	Run	Lights	LINK F ERROR	180
	R-loop link check	At any time	Run	Lights	LINK R ERROR	181
5	Dual-power supply error	At any time	Operates if there is a switchable power supply/ Stops if there is no switchable power supply	Lights/ Flickers	POWER ERROR	150
6	Link parameter check	When the power supply is turned on or the A3VTU is reset When STOP or PAUSE is switched to RUN	Run	Lights	LINK PARA. ERROR	47
7	Dual module power supply overheat check	At any time	Run	Lights	HEAT ERROR	170

Table 4.5 A3VTU Self-Diagnosis

REMARKS

Refer to Section 13.1 Error Message Table for further details regarding the checks described above. "Stop" in the A3VTU operation status column, indicates that the system operations stop.

4.10 Parameter

(1) Parameter setting involves specifying various PC functions and device ranges as well as assigning the user memory. The set data is stored in the parameter memory area (the first 3K bytes of the user memory area).

(2) Some parameter data is set by default values as shown in Table 4.6.
Parameter data can use the default values without further modification.

(3) The parameter data can be modified within the setting range shown in Table 4.6 according to the usage objective.
The parameters are set using the peripheral device.
Refer to the appropriate Peripheral Device Operations Manual for a description of parameter setting operations.

(4) Ensure that the same parameter data is set in all three A3VCPU modules when operating in the majority operation mode. Failure to do so can result in the handshake error "ERROR CPU[ ] [ ]".

REMARKS

1) When estimating the memory cassette size required, calculate the number of bytes used from the settings made as follows:

Item	Setting Unit	Number of Bytes
Main sequence program capacity	1K step	2K
Subsequence program capacity		
File register capacity	1K point	2K
Comment capacity	64 points	1K
Sampling trace enabled	128 times	1K

2) When comment capacity is set by a peripheral device, a value greater than 1K byte is displayed since settings are made in excess of 1K byte automatically.B

Item \ Setting		Default Value	Setting Range	Usable Peripheral Equipment			
				PU	GPP	HGP	PHP
Main sequence program area		6K steps	1 to 30K steps (in units of 1K step)	○	○	○	○
Subsequence program capacity		Absent	1 to 30K steps (in units of 1K step)	○	○	○	○
File register capacity		Absent	1 to 8K points (in units of 1K points)	○	○	○	○
Comment capacity		Absent	0 to 4032 points (in units of 64 points)	—	○	○	○
Status latch	Memory capacity	Absent	0/8 to 24K bytes	—	○	○	○
	Data memory		Absent/present				
	File register		Absent/present (2 to 16K bytes)				
Sampling trace	Memory capacity	Absent	0/8K bytes	—	○	○	○
	Device setting		Device number				
	Execution condition		Per scan				
			Per time				
	Sampling count		0 to 1024 times (in units of 128 times)				

Table 4.6 Parameter Setting Range (Continue)

Item \ Setting		Default Value	Setting Range	Usable Peripheral Equipment			
				PU	GPP	HGP	PHP
Microcomputer program capacity		Absent	0 to 58K bytes (in units of 2K bytes)	—	○	○	○
Setting of latch (power failure compensation) range	Link relay (B)	Only for L1000 to 2047. Absent for others.	B0 to 3FF (in units of 1 point)	○	○	○	○
	Timer (T)		T0 to 255 (in units of 1 point)				
	Counter (C)		C0 to 255 (in units of 1 point)				
	Data register (D)		D0 to 1023 (in units of 1 point)				
	Link register (W)		W0 to 3FF (in units of 1 point)				
Setting of link range	Number of link stations	Absent	1 to 64	—	○	○	○
	Input (X)		X0 to 7FF (in units of 16 points)				
	Output (Y)		Y0 to 7FF (in units of 16 points)				
	Link relay (B)		B0 to 3FF (in units of 16 points)				
	Link register (W)		W0 to 3FF (in units of 1 point)				
Setting of internal relay (M), latch relay (L), step relay (S) setting		M0 to 999 L1000 to 2047 Absent for S	M/L/S0 to 2047 M, L, S are serial numbers	○	○	○	○
Setting of watch dog timer		200ms	10ms to 2000ms (in units of 10ms)	○	○	○	○
Setting of timer		100ms: T0 to 199 10ms: T200 to 255	256 points of 100ms, 10ms, and integrating timers (in units of 8 points) Timers have serial numbers.	○	○	○	○
I/O number assignment	Input (X) module	Absent	0 to 64 points (in units of 16 points)	—	○	○	○
	Output (Y) module						
	Special function module						
	Empty slot						
Setting of remote run/pause contact		Absent	X0 to 7FF (1 point for each of run and pause contacts. Setting of only pause contact cannot be performed.)	—	○	○	○
Operation mode at the time of error	Fuse blow	Continuation	Stop/continuation	—	○	○	○
	I/O verify error	Stop					
	Operation error	Continuation					
	Special function unit check error	Stop					
Annunciator display mode		F number display	Display of only F number or alternate display of F number and comment (Only alphanumeric characters may be displayed for comment.)	—	○	○	○
STOP → RUN display mode		Operation status prior to stop is re-output.	Output before stop or after operation execution	—	○	○	○
Print title entry		Absent	128 characters	—	○	○	○
Keyword entry		Absent	Max. 6 digits in hexadecimal (0 to 9, A to F)	○	○	○	○

Table 4.6 Parameter Setting Range

POINT

Set the watchdog setting to a value of the largest normal scan time plus 400ms.

4.11 Functions

4.11.1 Function list

Function	Description	Refer to:
Majority operations	○ Two operation modes are provided. One is the single- module mode in which one A3VTU module and one A3VCPU module operate together. The other is the majority operation mode in which one A3VTU and three A3VCPUs operate together. ○ Majority operation enables operation to continue without stopping if a malfunction occurs in an A3VCPU or a dual-power supply module.	Section 5
Module replacement during operation	○ This function enables A3VCPU modules, dual power supply modules, and I/O modules to be replaced during system operations without terminating system operations.	Section 4.11.2
Constant scan	○ Executes the sequence program at the predetermined intervals independently of the scan time. ○ Setting allowed between 10 and 2000ms.	Section 4.11.3
Latch (Power-failure backup)	○ Retains device data if the PC is switched off or reset or instantaneous power failure occurs 20ms or longer. ○ L, B, T, C, D and W can be latched.	Section 4.11.4
Remote RUN/STOP	○ Allows remote run/stop from external device (e.g. peripheral, external input, computer) with RUN/STOP switch in RUN position.	Section 4.11.5
Pause	○ Stops operation with the output (Y) status retained. ○ Pause function may be switched on by any of the following ways: ● RUN/STOP switch on the front of the CPU ● Remote pause contact ● Peripheral	Section 4.11.6
Status latch	○ Stores all device data to the status latch area of the memory cassette when the status latch condition is switched on. ○ The stored data can be monitored by the peripheral.	Section 4.11.7
Sampling trace	○ Samples the specified device operating status at predetermined intervals and stores the sampling result in the sampling trace area of the memory cassette. ○ The stored data can be monitored by the peripheral.	Section 4.11.8
Offline switch	○ Allows the device (Y, M, L, S, F, B) used with the OUT instruction to be disconnected from the sequence program operation processing.	Section 4.11.9

Table 4.7 Function List

4.11.2 Module replacement during online operations

APPLICATION

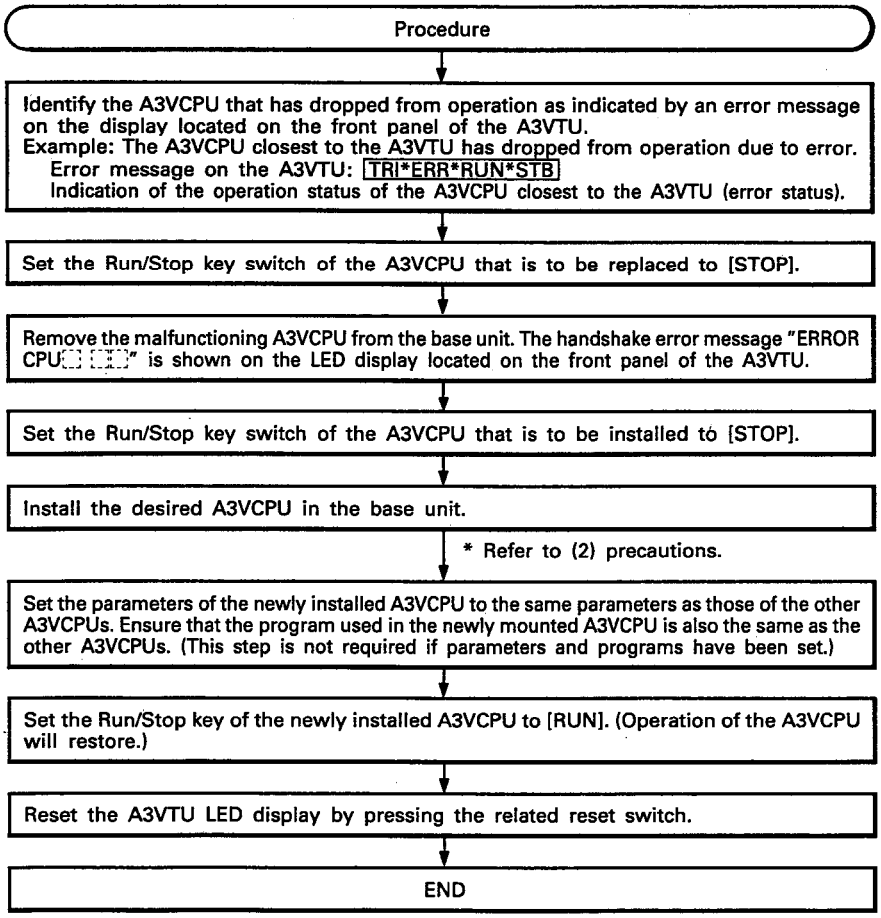
(1) Allows A3VCPU modules, dual-power supply modules, and I/O modules to be replaced during A3VTS system operation without stopping terminating system operations.

FUNCTION

(1) Allows A3VCPU modules to be replaced one at a time during system operation while in the majority operation mode. The system continues operating with other A3VCPUs.
However, it is necessary that one module other than the one being replaced be functioning normally.
(2) Allows power supply modules to be replaced one at a time when operating using dual-power supply modules. It is necessary that one module other than the one being replaced be functioning normally.
(3) Allows input and output modules to be replaced one at a time during system operation.
(4) The above three functions permits module replacement to be done without terminating the system operation.

OPERATION I

(1) Procedure for replacing A3VCPU modules (while in majority operation only)



(2) Precautions

(a) When system operation is to continue during CPU module replacement, at least one other A3VCPU must be operating correctly.

(b) As long as power is applied to the system, the replacement procedure described above must be followed xduring A3VCPU replacement even if the system is in the STOP status.

(c) Ensure that the program and parameters used by the newly installed A3VCPU are the same as those being used by the other two A3VCPUs. If the contents of either the program or parameters vary, the module will be dropped from operation or become a source of error generation.

(d) The messages listed below sometimes appear on the LED display located on the front panel of the A3VCPU module when a new A3VCPU is installed in the base unit. When they are displayed, reset with the A3VCPU RESET key switch. The display is cleared and the A3VCPU will restore operation.

Displayed error messages

A3VTU ERROR
DP RAM ERROR } One of the two will be displayed.

OPERATION II

(1) Procedure for dual-power supply module replacement

Follow the procedure given below to replace dual-power supply modules that have malfunctioned during system operation.

Procedure

↓

Turn off the power to the malfunctioning power supply module. The error message "POWER ERROR" is shown on the LED display located on the front panel of the A3VTU.

↓

Remove all cables connected to the malfunctioning power supply module.

↓

Remove the malfunctioning power supply module from the base unit.

↓

Install the desired power supply module in the base unit.

↓

Reconnect all required cables to the power supply module and turn on the power.

↓

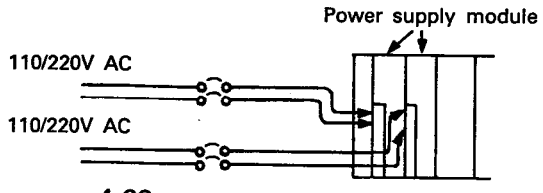
Reset the display by pressing the A3VTU LED reset switch.

↓

END

(2) Precautions

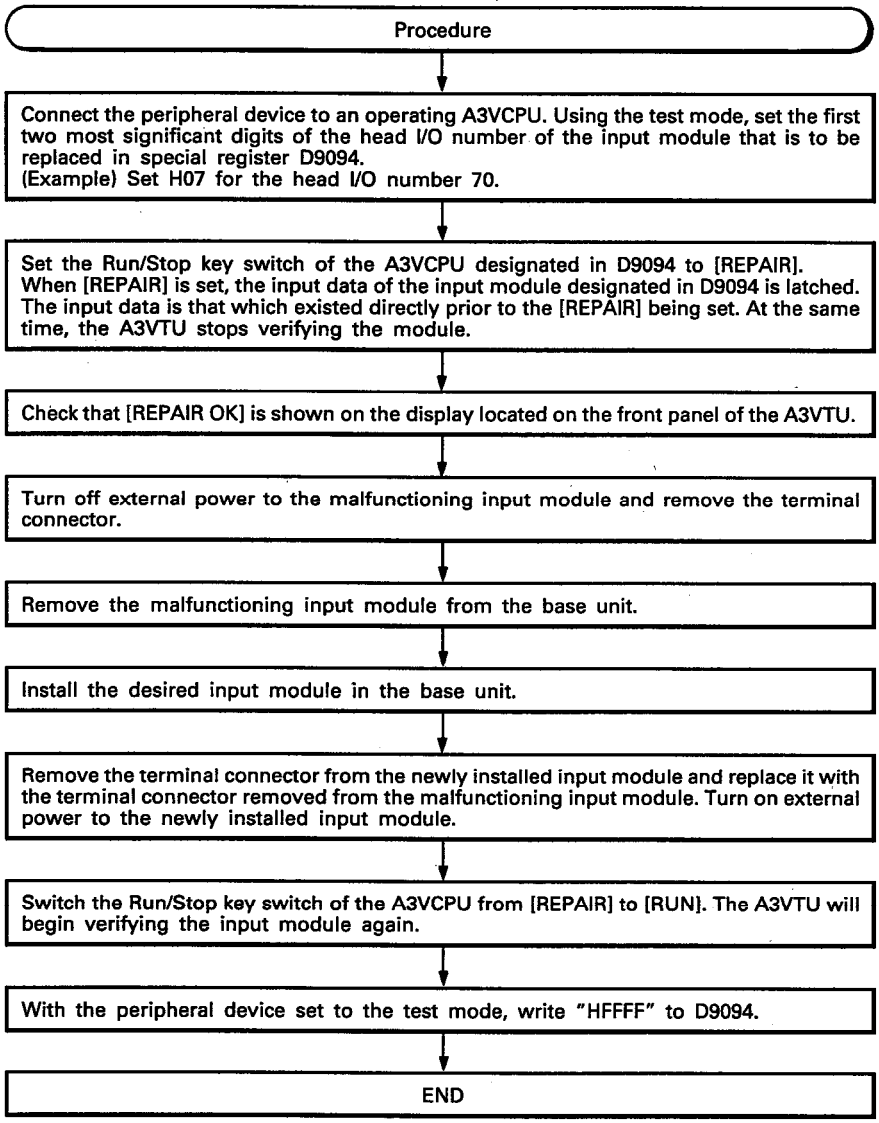
(a) When replacing power supply modules, it is important that the power supply for the power supply module being replaced is turned off. To ensure that this is done, the following wiring is recommended for the power supplies.



OPERATION III

(1) Procedure for I/O module replacement
Follow the procedure given below to replace I/O modules that have malfunctioned during system operation.

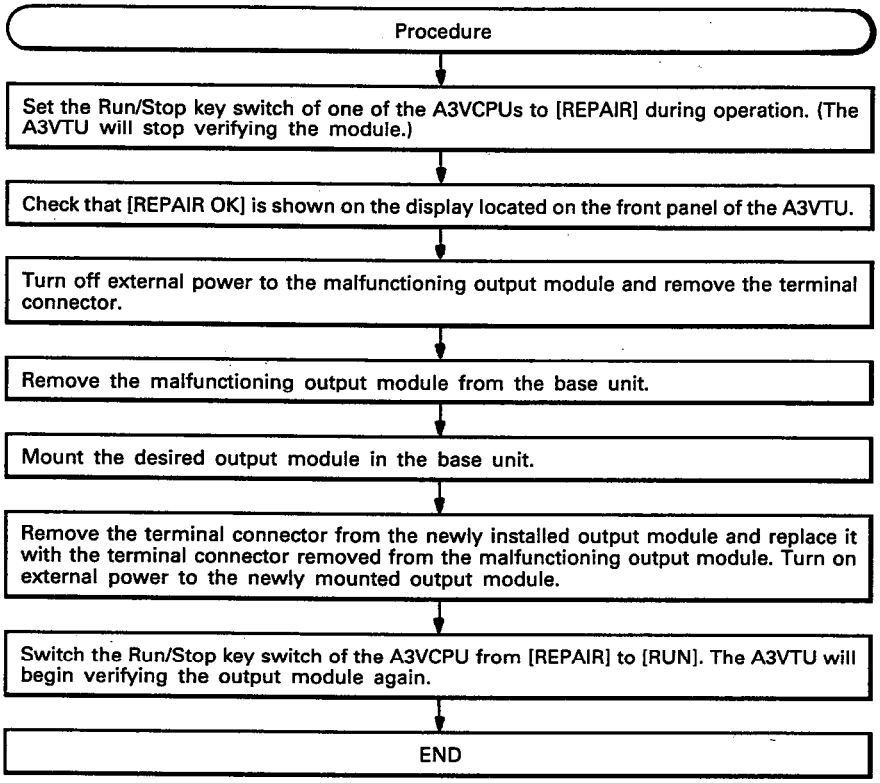
(a) Input module replacement



REMARKS

Two methods for replacing an input module are available. One uses the peripheral device as described above. The other uses the sequence program. In the latter, the first two most significant digits of the head I/O number are set in hexadecimal in D9094 using the sequence program. After this is done and the A3VCPU is set to [REPAIR], the replacement procedure is the same for both methods.

(b) Output module replacement



(2) Description of processing occurring during I/O module replacement

(a) The following processing occurs when the Run/Stop key switch of the A3VCPU is set to [REPAIR].

1) Module verification of all I/O modules is stopped beginning with the scan following the scan in which [REPAIR] was set.
2) For an input module, the input data of the input module corresponding to the address set in D9094 is latched until the END of the scan in which [REPAIR] was set. This data is contained in the image memory and no subsequent access is made to this input module.
3) When [REPAIR] is set for output modules, access of the output module in question continues.
4) After [REPAIR], CPU processing is executed using data contained in the image memory in relation to the module in question.

(b) The following processing occurs when the Run/Stop key switch of the A3VCPU is switched from [REPAIR] to [RUN].

1) Module verification of I/O modules is restarted with the scan following the scan in which [RUN] was set.
2) For input modules, access is restarted with the module in question with the scan following the scan in which [RUN] was set.

(c) Even during I/O module replacement, all modules other than the malfunctioning module operate normally.

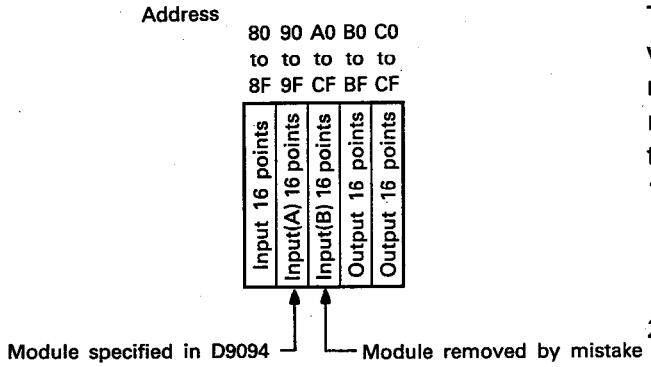
(3) Precautions

(a) The special function module cannot be replaced during operation. Set the RUN/STOP switch to the STOP position and turn the power off before replacing the module.

(b) Only input modules registered in special register D9094 can be replaced.
Replacing an input module that has not been registered will result in incorrect inputs.

Example:

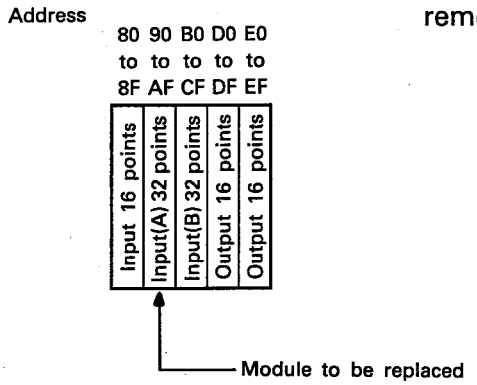
(1) Removal of a module unregistered in D9094



The diagram on the left shows an example where input module (B) was mistakenly removed in place of input module (A). Doing so results in the execution of the program using the following input data.

1) Data input is latched by X90 to 9F at the point [REPAIR] is set, and used. Input data received from external sources after the latching action is ignored.
2) XA0 to AF are all set to OFF since the module has been removed.

(2) An address between the first and last addresses of an input module is registered in D9094 and that module is removed.



The diagram on the left shows an example where the address [HA] was mistakenly registered in D9094 in place of [H9] and input module (A) was removed. Doing so results in the execution of the program using the following data.

1) X90 to 9F are all set to OFF since the module has been removed.
2) Data input is latched by X90 to 9F at the point [REPAIR] is set, and used. Input data received from external sources after the latching action is ignored.
Changes to XB0 to XBF due to input data from external sources is ignored.

(c) HFFFF is written in the special register D9094 automatically when power is applied. Verify the range of the data to be written to special register D9094 before it is written because the data outside the range can also be set as it is since the I/O number assignment range is not checked.

(d) The A3VTU does not perform module verification when the Run/Stop key switch is set to REPAIR in at least one of the A3VTU modules. Unit verification is restarted if the Run/Stop key switch is set to another position. The REPAIR mode is the same as the RUN mode except for the module verification.

(e) The A3VTU continues to perform output refresh for the output module even as it is being replaced. It is therefore very important to ensure that the external power supply of the output module is turned OFF when a replacement module is installed.

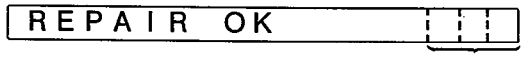
(f) When the key switch of more than one A3VCPU module is set to REPAIR, ensure that address D9094 in each A3VCPU module is set to the same value. If different values are set, the A3VCPU module closest to the A3VTU has priority when the key switches in multiple A3VCPU modules are set to REPAIR. The D9094 value in the A3VCPU module that has priority becomes valid. In single-module operations, the A3VCPU module set to RUN has priority.

(g) The latching of the input module data can be conducted only one time for each module. Repeat the single module tab replacement procedures when more than one input modules are to be replaced.

(h) Do not change system operation mode when [REPAIR OK] is displayed. A [UNIT VERIFY ERROR] message will be displayed if the system operation status is set from STOP PAUSE to RUN, a module is installed, and REPAIR is set to RUN.

(i) Always follow the specified I/O module replacement procedure so far as the power supply is turned ON even if the system Run/Stop key switch is set to STOP. Failure to do so will result in the message [UNIT VERIFY ERROR].

(j) The following message appears on the A3VTU display when the A3VCPU module Run/Stop key switch is set to [REPAIR].



The head I/O number of the I/O module specified in D9094 is displayed. A blank appears when not specified in D9094.

This display has a priority higher than any other including error messages. If left as [REPAIR] and an error is generated, the corresponding error message cannot be displayed. It is therefore important to reset the key switch from [REPAIR] to [RUN] as soon as the module is replaced. If an error has been generated, the corresponding error message is displayed when the key switch is set to [RUN].

(k) When the system stops because of an error, the module verification is performed even when the A3VCPU module Run/Stop key switch is set to [REPAIR].

4.11.3 CONSTANT SCAN

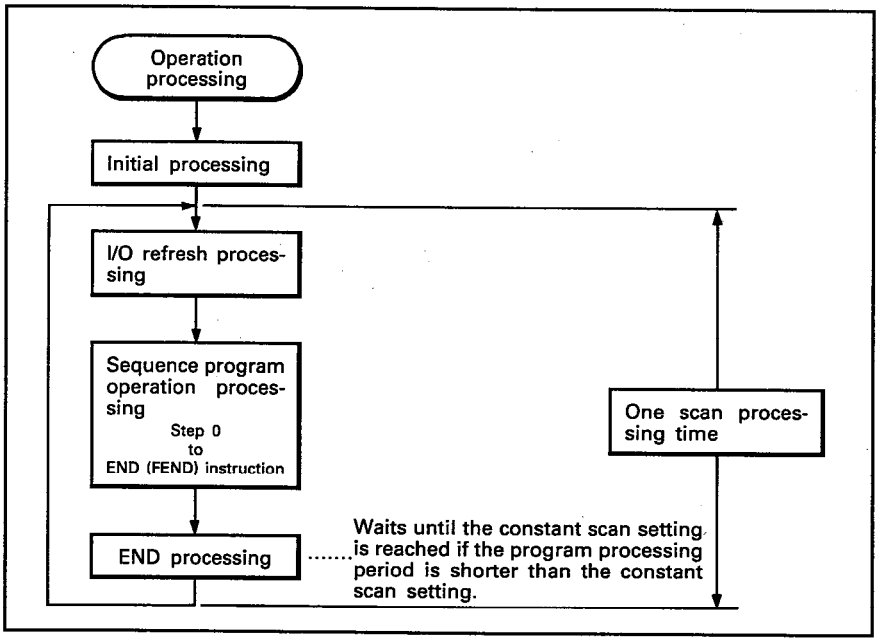
APPLICATION

The sequence program cannot output signals in fixed intervals since the scan time varies depending on whether an instruction is executed or not.
Constant scan can output signals at fixed intervals. This can improve positioning accuracy in such as simplified positioning operation.

FUNCTION

(1) Definition

Makes each scan time constant.



When operating in the majority operation mode, use the same constant scan value for each of the A3VCPU modules.

(2) Operation

(a) Constant scan is initiated at the scan when the set value is written to D9020.

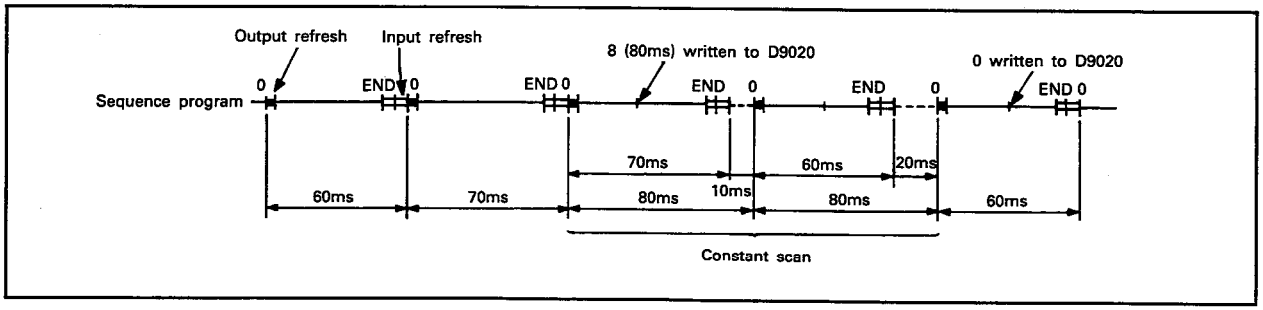


Fig. 4.10 Constant Scan Execution

(b) The constant scan setting must be greater than the maximum scan time in the sequence program.
The constant scan is not executed normally if its setting is shorter than the program scan time.

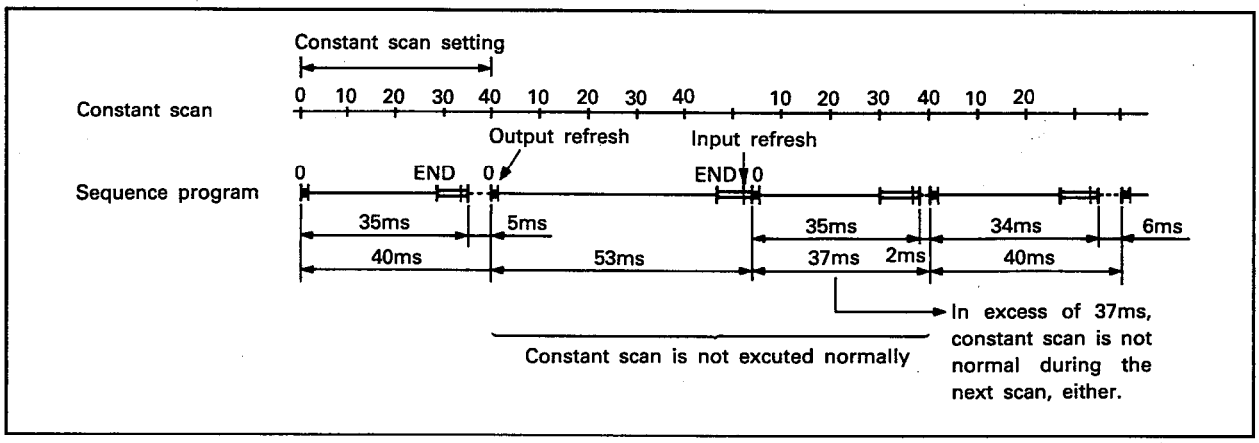


Fig. 4.11 Scan Time Longer Than Constant Scan Setting

OPERATION

(1) Execution of the constant scan

The following two types of operation procedures are performed for the execution and termination of the constant scan.

1) To write a value of "0" to D9020 by the sequence program.
2) To write a value of "0" to D9020 in the test mode of the peripheral device.

(a) To execute constant scan

1) Write the set value to D9020 in the sequence program; or
2) Write the set value to D9020 in test mode of the peripheral.

(b) To terminate constant scan

1) Write 0 to D9020 in the sequence program; or
2) Write 0 to D9020 in test mode of the peripheral.

(c) To change the set value during CPU RUN

1) Modify the set value write program using the peripheral, rewrite it during RUN, and switch on the constant scan setting command; or
2) Write a new value to D9020 in test mode of the peripheral.

(2) Constant scan setting range

(a) The constant scan setting is written in D9020 in 10ms increments between 1 and 199. If values other than 1 to 199 are set the follow occurs.
- −32768 to 0: No constant scan is set
- −1 to 199: Constant scan (10 to 1990ms)
  200 and above: A [WDT ERROR] message is displayed.

(b) The relationship between the D9020 settings and the WDT (watchdog timer) is defined as follows.

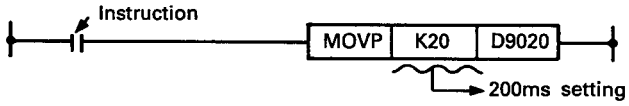
D9020 setting value ≦ (WDT setting)−1

A WDT (watchdog timer) error is generated when the value in D9020 is set to a value greater than this expression.

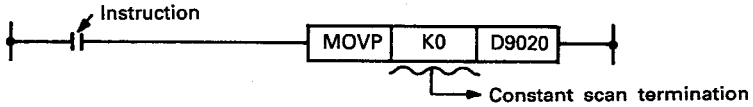
(3) Program example

The following example is a program that performs constant scan settings and termination.

(a) To set the constant scan of 200ms

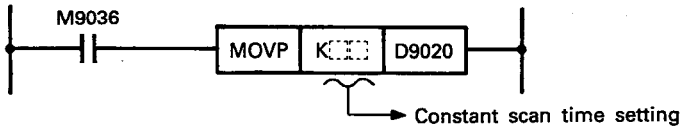


(b) To terminate the constant scan



CAUTION

(a) D9020 is cleared when the PC is switched on or reset. The following program is required to initiate constant scan after power on or reset.



(b) The constant scan function cannot be used with the CHG instruction.
The CHG instruction execution time will be included in the constant scan time if CHG is used with the function.

(c) The constant scan is prolonged and is not executed normally if an instantaneous power failure occurs less than 20ms.

(d) During majority operation, when the constant scan time for three A3VCPU modules differs, the system scans using the largest value.
A [WDT ERROR] is returned if the value set is greater than that of the watchdog timer.

(e) The monitor value for scan time during constant scan is the actual scan time and not the constant scan time.
The scan time stored in the special register D (D9017 to D9019) is the actual scan time and the constant scan time.

4.11.4 LATCH (power-failure backup)

APPLICATION

Retains data if an instantaneous power failure occurs more than 20ms during continuous control.

FUNCTION

(1) Definition

Retains device data in the CPU module when the PC is switched off or reset or if an instantaneous power failure has occurred for more than 20ms.

(2) Devices latched

1) Latch relay (L)
2) Link relay (B)
3) Timer (T)
4) Counter (C)
5) Data register (D)
6) Link register (W)

(3) Clearing the latched data

(a) Latched data can be cleared by setting all A3VCPU modules to [STOP] and performing either of the procedures described below ((1) or (2)).
The clearing of latch data occurs with each A3VCPU.

1) Set the RUN/STOP switch to STOP and move the RESET switch to LATCH CLEAR.

2) Clear all devices from the GPP/HGP/PHP.

(b) When latch clear is executed, the A3VCPU module LED panel displays the [LATCH CLEAR OK] message.
(c) When latch clear is executed, everything is cleared except device data of special relays (M), special registers (D), and off line switch settings (only during single-module operation). (Output (Y) is also cleared).

OPERATION

The latch range is set in the peripheral parameters per device.

CAUTION

(a) Device data within the latch range is backed by the battery (A6BAT) in the memory cassette.
The battery is therefore required even when operation is performed using a ROM which stores the sequence program.

(b) Latched/unlatched device data is stored in the CPU module. The data in the latch range is therefore corrupted if any of the following operations is performed with the power off.

1) Disconnect the battery connector from the memory cassette connector.
2) Remove the memory cassette from the CPU module.

(c) As stated above, the latch clear function is meant to be executed for each of the A3VCPUs. It is therefore necessary, that the latch clear function be executed for all A3VCPUs. If one of the A3VCPU modules is not cleared during majority operation, the uncleared module may be dropped when the A3VCPU is used in a systems operation.

4.11.5 REMOTE RUN/STOP

APPLICATION

(a) In any of the following cases, RUN/STOP may be executed at remote locations without controlling the RUN/STOP switch on the CPU front panel.
1) The CPU module is out of reach.
2) When the CPU module is contained in the control board.

FUNCTION

(1) Definition

Controls run/stop of the CPU module from an external device (e.g. peripheral, external input, computer) when the RUN/STOP switch is in RUN position.

(2) Operation

1) Remote stop
The CPU is set to STOP after the sequence program is executed up to the END (FEND) instruction.
2) Remote run
After remote stop, remote run sets the CPU back to RUN to execute the sequence program from step 0.

OPERATION

(a) Remote run/stop may be executed using:
1) Remote run contacts (external input to be set by the peripheral)
2) Peripheral;
During majority operating, cannot operate by peripheral

Remote RUN contact method

The A3VTS system Run/Stop is performed by setting the Remote RUN contact specified by the parameter setting to ON or OFF.
Setting CPU Run/Stop status by the Remote RUN contacts is performed as follows.

Remote RUN contacts: { OFF·····RUN status
ON ·····STOP status

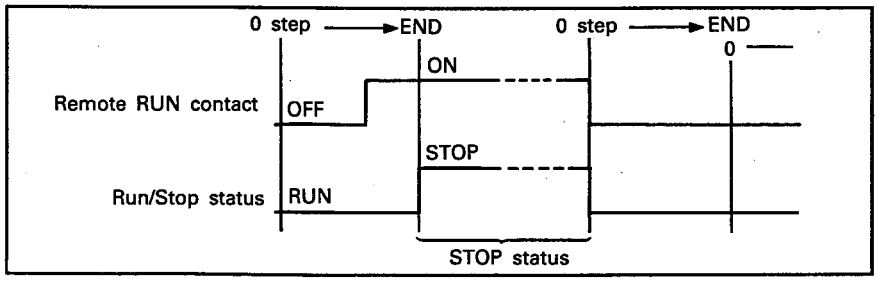


Fig. 4.12 Time Chart for Remote Run/Stop Operations Using Remote RUN Contacts

Peripheral device method

The A3VCPU module is set to RUN/STOP by the remote run/stop command from the peripheral.

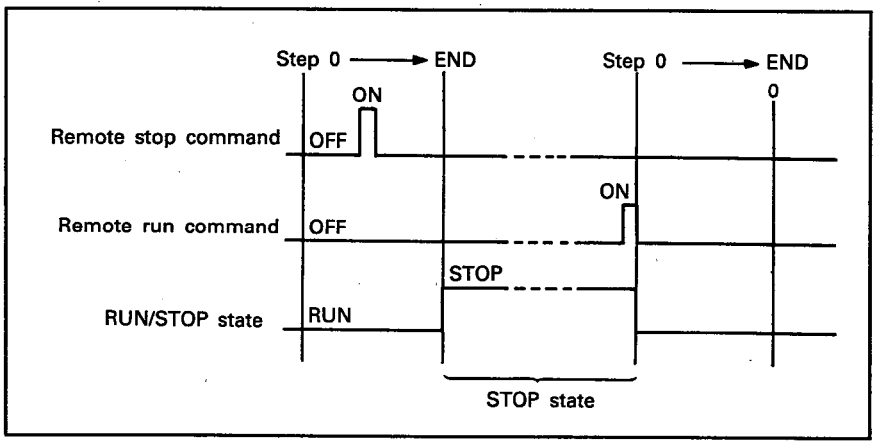


Fig. 4.13 RUN/STOP Timing Using Peripheral

CAUTION

(a) Operations cannot be performed by the peripheral device during majority operations.
Remote Run/Stop procedures are difficult to perform simultaneously from peripheral device in three A3VCPU modules. An operation timing discrepancy will result in an A3VCPU module malfunction and its being dropped from operation.

(b) After the system has been set to STOP status by remote STOP, the external device (remote RUN contacts, peripheral device) that initiated remote STOP must be set to remote RUN to set the RUN status again.

(c) System operation status changes according to the A3VTU and A3VCPU key switch setting as well as the instructions from external sources. This means that the status of keys can prevent the Remote Run/Stop from functioning. Refer to Chapter 5 for further details.

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CAUTION

The Remote Run/Stop function provided by peripheral device clears the data in each device during Remote RUN in addition to Run/Stop the CPU modules.
The content of device range that can be cleared differs depending on the ON/OFF status of special relays M9016 and M9017. This function is described below.

(a) System operation status is in either PAUSE or STOP (not limited to Remote STOP or PAUSE).

(b) The processing described in the table below is performed when the remote RUN is executed by peripheral device. Note that the following processing is not performed if the A3VCPU is in WAIT, error, or RUN.

M9017 \ M9016	ON	OFF
ON	Clears all areas other than special relays M, special registers D, and offline switch memory	Clears non-latched areas other than special relays M, or special registers D, and offline switch memory.
OFF	Same as above	Nothing is cleared

4.11.6 PAUSE

APPLICATION

Used when control is to be continued under the identical one set of conditions for output status during process control.

FUNCTION

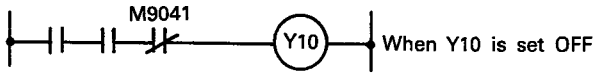
(1) Definition

The pause function stops the operation processing of programmable controller CPU while simultaneously holding output (Y) in its last state prior to entering the pause mode.
Therefore, since the output (Y), whitch was on immediately before the pause mode, remains on, the external load is also in the on status.

(2) Operation

(a) M9041 is switched on after END of the scan during which the PAUSE condition has been switched on.
Operation is stopped when the next scan (scan after M9041 is switched on) is executed up to the END (FEND) instruction.
(b) The CPU retains all output states after operation of one scan after M9041 is on.
Any output that should be switched off in PAUSE state must be interlocked using M9041.

Example:



OPERATION

(a) The A3VTS system may be set to PAUSE by:
1) RUN/STOP switch
2) Remote pause contacts (set by the peripheral); or
3) Peripheral (These operations cannot be performed during majority operation.)

RUN key switch

(a) The following procedures are used when executing PAUSE with the RUN key switch.
1) The program or peripheral device sets M9040 address of each A3VCPU module ON.
2) Set the A3VTU Run/Stop key switch to PAUSE.

(b) Operations stop when operations reach the END (FEND) of the scan after the scan in which operation (2) was performed.

(c) Set the A3VCPU module Run/Stop key switch to RUN to restart operations.

(d) If the M9040 is set OFF by the peripheral device and operations are restarted, then the method described in (c) must be performed since the A3VCPU module sometimes is dropped from operations due to a timing discrepancy that sets the M9040 OFF for each A3VCPU module.

(e) Be sure to perform the operations in (a) in the order of (1) and then (2). This is because the A3VCPU module may drop from operation due to a timing discrepancy that sets M9040 to ON in each of the three A3VCPU modules if they are performed in the reverse order.

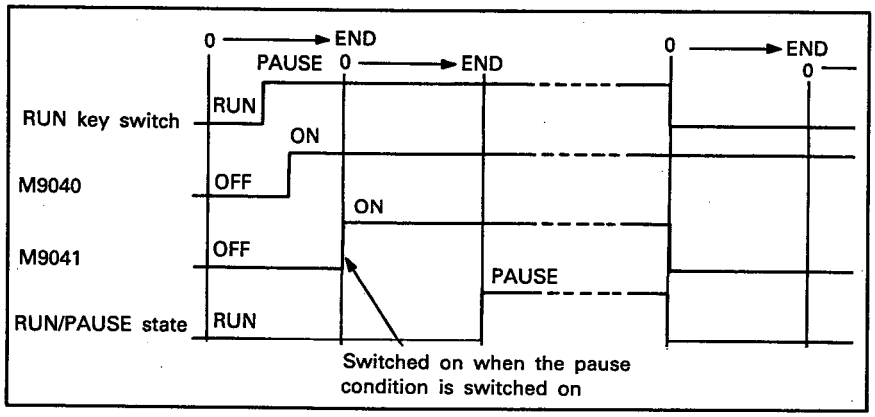


Fig. 4.14 PAUSE Timing by RUN key Switch

4

Remote PAUSE contact method

(a) Perform the following procedures when using the remote PAUSE contacts
  1) Set M9040 in each A3VCPU module ON by a program or a peripheral device.
  2) Set the remote PAUSE contact ON.

(b) Operations stop when operations reach the END (FEND) of the scan after the scan in which operation (2) was performed.

(c) Set the remote PAUSE contact OFF to restart operations.

(d) If M9040 is set OFF by the peripheral device and operations are restarted, then the method described in (c) must be performed since the A3VCPU module sometimes is dropped from operations due to a timing discrepancy that sets the M9040 OFF for each A3VCPU module.

(e) Be sure to perform the operations in (a) in the order of (1) and then (2). This is because the A3VCPU module may drop from operation due to a timing discrepancy that sets M9040 to ON in each of the three A3VCPU modules if they are performed in the reverse order.

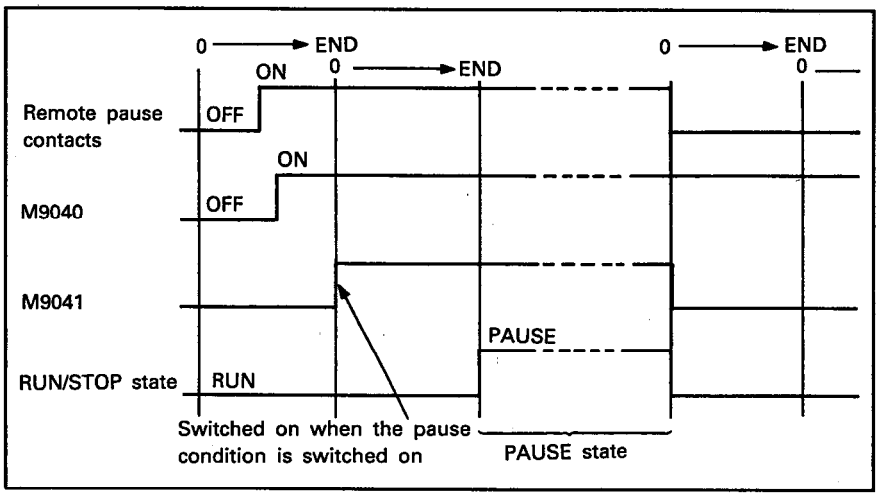


Fig. 4.15 PAUSE Timing by Remote Pause Contacts

Peripheral

1) Operation is stopped when the sequence program is executed up to the END (FEND) instruction during the scan after the remote pause command is given by the peripheral.
2) The operation is resumed when the remote run command is provided by the peripheral.

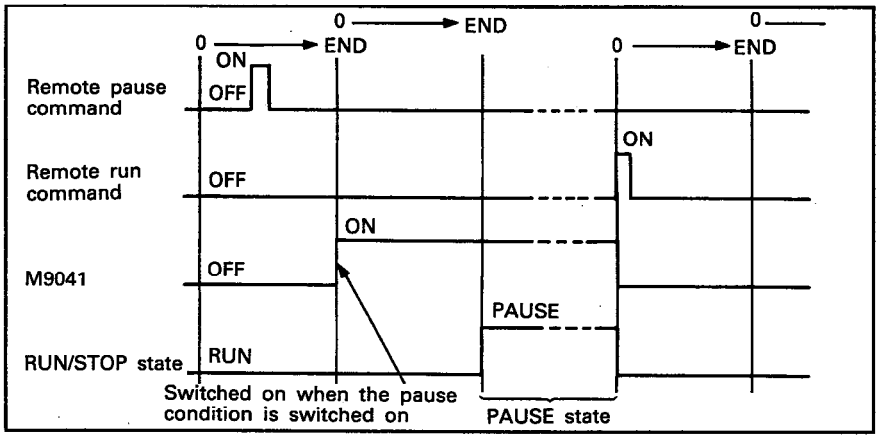


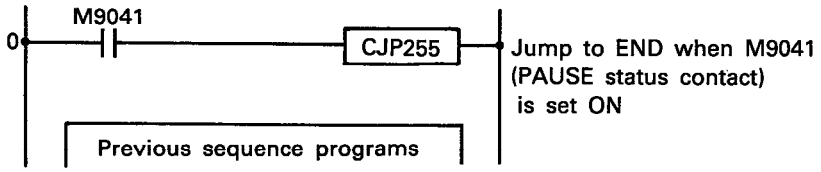
Fig. 4.16 PAUSE Timing by Peripheral

CAUTION

(a) The remote PAUSE instruction cannot be used by the peripheral device test operation when majority operations are performed. Remote PAUSE procedures are difficult to perform simultaneously from the peripheral device in three A3VCPU modules.
An operation timing discrepancy will result in an A3VCPU module malfunction and its being dropped from operation.

(b) Address M9040 must be set ON in each of the three A3VCPU modules when the PAUSE status is set by an A3VTU Run/Stop key switch or a remote PAUSE contact.
If even one of the A3VCPU modules is not set ON, the system operation will continue and the A3VCPU module that has M9040 set ON will generate an error and drops from operations.

(c) The PAUSE status is set after one scan operation when shifting the system operation status from a STOP to a PAUSE.
If it is desired to shift to PAUSE status without executing one scan operation, append the program described below to the user program in each A3VCPU module.



(d) Before setting the PAUSE status with either the Run/Stop key switch of the A3VTU or the remote PAUSE contact, be sure to first set address M9040 to ON in the three A3VCPU modules.
If the operation is performed in reverse, the A3VCPU modules will generate an error and can be dropped from operation due to a timing discrepancy that sets M9040 to ON in the three A3VCPU modules.

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4.11.7 STATUS LATCH

APPLICATION

Can be used to check device data when a given condition is switched on during debugging.

FUNCTION

(1) Definition

Status latch stores the contents of all devices in the status latch area of the memory cassette at the time the SLT instruction is executed.
The data stored in the status latch area can be read and monitored by GPP/HGP/PHP.

(2) Stored data

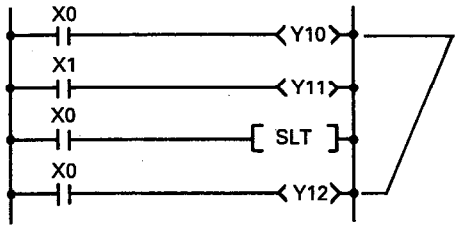
The following data may be written to the status latch memory area:

1) X, Y, M, L, S, F, B ····· ON/OFF data
2) T, C ····· Contact, coil ON/OFF data and present value
3) D, W, A, Z, V, R ····· Stored data

(3) Data storing timing

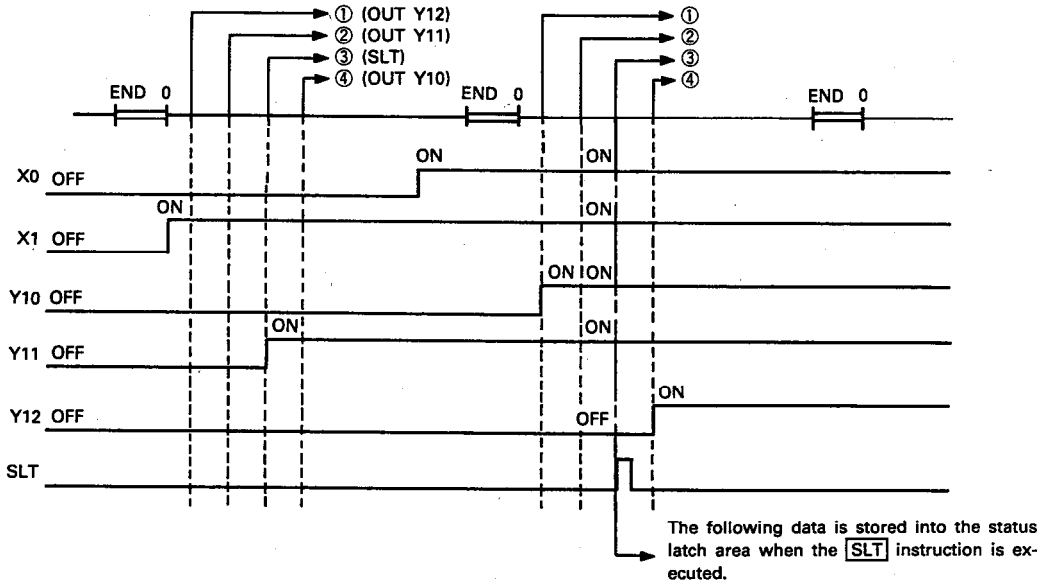
(a) Data is stored into the status latch area when the SLT instruction is executed. Hence, any device data that has changed after the execution of the SLT instruction is not stored into the status latch area.

(b) An explanation concerning the storage of data when the SLT instruction is executed will be given using the circuit shown in the figure below.



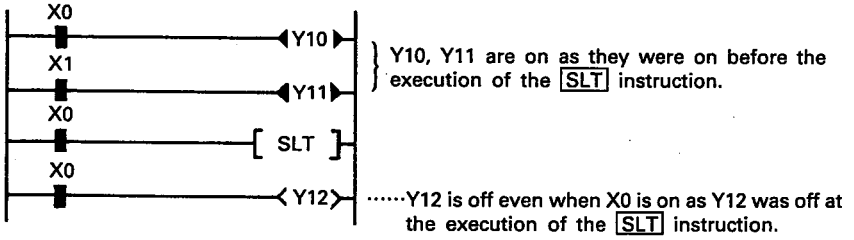
OUT instructions switched on/off by the same input (X0) exist before and after the SLT instruction.

Timing chart



X0	X1	Y10	Y11	Y12
ON	ON	ON	ON	OFF

Monitoring the status latch data



OPERATION

(a) Setting the status latch area

Specify the status latch area by setting the parameter using the GPP/HGP/PHP and write it to the CPU module.

(b) Executing the status latch

Data is written to the status latch area when the SLT instruction is executed.

(c) Resuming the status latch

To execute the SLT instruction again, reset the SLT instruction by executing the SLTR instruction.

CAUTION

(1) Execution of the SLT instruction increases scan time as indicated below. The watch dog timer should be set in consideration of the increase in scan time.

	Device Memory Only	Device Memory and File Register
Processing time (ms)	8.5	24.6

(2) The execution of the SLT instruction during majority operations must be done simultaneously in the three A3VCPU modules.
A timing discrepancy in the operation of one of the three A3VCPU modules will result in an error being generated in the A3VCPU module executing the SLT instruction and its being dropped from operation.

4.11.8 SAMPLING TRACE

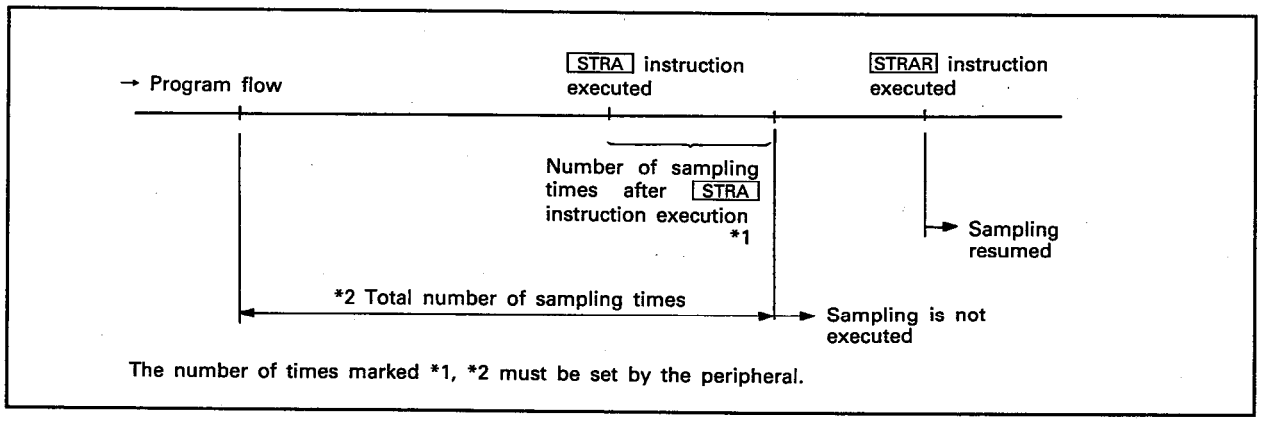
APPLICATION

Shortens the time required for debugging devices by verifying their contents in fixed intervals during debugging in accordance with a program. Allows debugging time to be reduced.

FUNCTION

(1) Definition

The sampling trace samples the contents of the specified device in a fixed interval (the sampling cycle) and stores them in the sampling trace area in the memory cassette.
The data stored in the sampling trace area is latched after a specified number of samplings occur when the STRA instruction is executed.
The data in the sampling trace area can be read and monitored by GPP/HPH/PHP.



(2) Devices used

The number of devices which may be used up for the sampling trace is limited as follows:

1) Bit devices (X, Y, M, L, S, F, B, T/C coil, T/C contact)
····· Max. 8 points

2) Word devices (T/C present value, D, W, R, A, Z, V)
····· Max. 3 points

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OPERATION

(a) Setting the sampling trace area

Specify the sampling trace area using the GPP/HGP/PHP and write to the CPU module.

(b) Setting the sampling trace data

Set the following data by the GPP/HGP/PHP and write to the CPU module.

1) Number of sampling trace times
2) Devices to be traced
3) Sampling period

(c) Starting the sampling trace

Sampling trace may be initiated by:

1) Peripheral;
2) Switching on M9047.

(d) Terminating and stopping the sampling trace

To terminate:

By executing the STRA instruction, sampling is executed the specified number of times, data is latched, and the sampling trace is terminated.

To stop:

Sampling trace may be stopped by using the peripheral or by switching off M9047.

(e) Checking the sampling trace data

Read and monitor the sampling trace area data using the periphral.

(f) Resuming the sampling trace

Execute the STRAR instruction.

CAUTION

(a) If the sampling of each period is set during majority operations, the sampling results may differ between A3VCPU modules since each A3VCPU module counts the sampling time and manages time individually.

4.11.9 OFFLINE SWITCH

The offline switch can only be used in the independent operation mode. It cannot be used in the majority operation mode.

APPLICATION

Can be used to make the following checks in test mode of the peripheral with respect to the OUT instructions which are not being switched on/off during execution of the sequence program.

1) Output module operation check
2) Output module and external device wiring check

FUNCTION

(1) Definition

(a) The offline feature disconnects devices (Y, M, L, S, F, B) used with the OUT instructions from the sequence program.
(b) Online/offline statuses are set when the imaginary offline switches as shown in Fig. 4.17 are closed/opened.

1) Opening the offline switch

Offline status is set. The OUT instruction device is disconnected from the sequence program.

2) Closing the offline switch

Online status is set. The OUT instruction device is controlled by the sequence program.

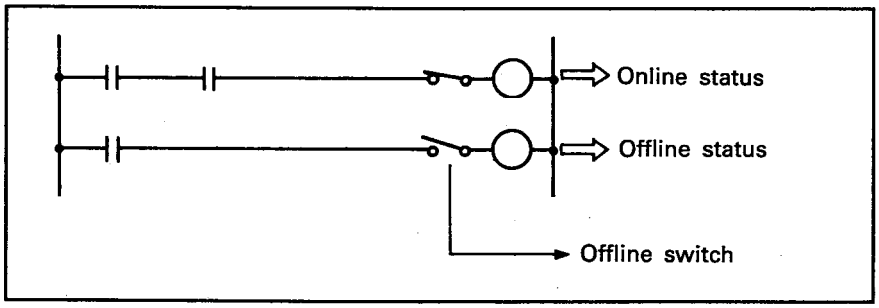


Fig. 4.17 Online/Offline Statuses

(2) Device statuses in offline mode

(a) OUT instruction devices remain in the state that they were immediately prior to entering offline mode.
(b) If set/reset is forced by the peripheral in offline mode, devices remain in the state that they were forced.

OPERATION

(a) Setting the offline switch

Set the offline switch using the peripheral.

(b) Canceling the offline switch

1) Use the peripheral.
2) Reset the CPU module.

CAUTION

(a) After the test operation is completed, it is necessary to cancel the offline switch setting and set the online mode.

(b) The offline switch cannot be used in majority operations. Using the offline switch results in instruction timing discrepancy causing the A3VCPU module to malfunction and be dropped from operations.

4.12 Handling

This section gives handling instructions, PC nomenclature and hardware setting instructions.
Refer to the appropriate chapter for information concerning procedures covering from when modules are installed to their operation.

4.12.1 Handling instructions

A3VTU and A3VCPU module handling cautions are described below.

(1) Do not subject the CPU module and memory cassette to impact or shock.

(2) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards. This can be a source of damage.

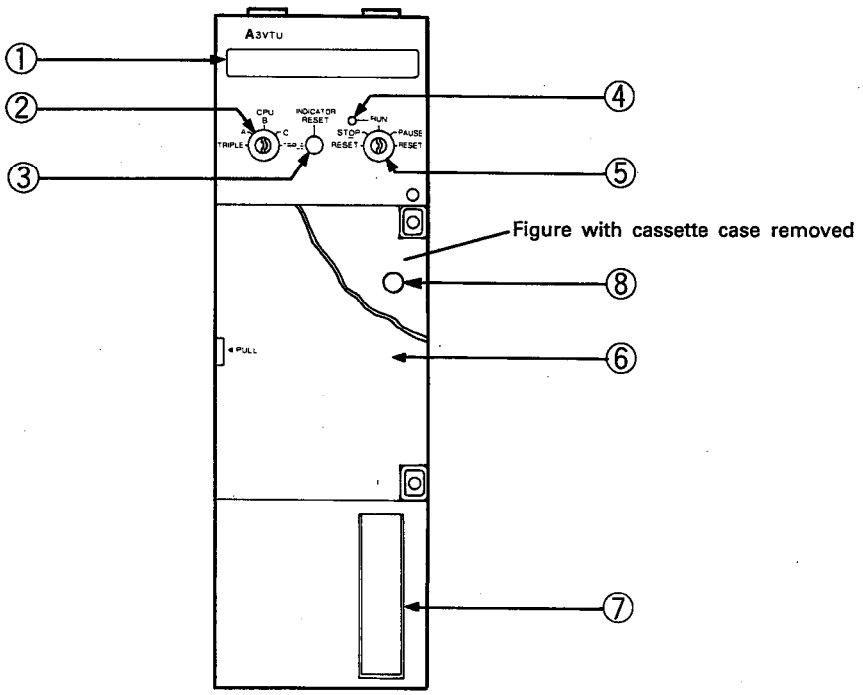
(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Tighten the module mounting and terminal screws as specified below.

Screw	Tightening Torque kg·cm (lb·inches)
Module mounting screws (optional) (M4)	8 (6.93) to 12 (10.39)

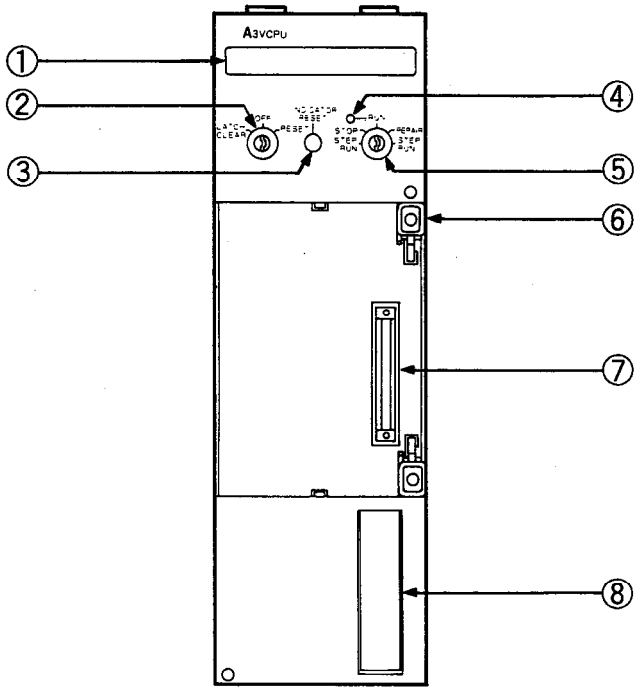
(5) After mounting the module in the base unit, ensure that the hook is locked in the base unit securely.
When removing the module, press the hook until it is completely free from the base and then pull the module forward. (Refer to Section 10.5 for further details.)

4.12.2 Nomenclature (A3VTU)



No.	Description	Application
①	LED display	An error message (maximum 16 characters) generated during self-diagnosis is displayed.
②	Operation mode setting key switch	A, B, C: Indicates the independent operation mode. Only the A3VCPU module corresponding to the indicated letter operates. The A3VCPU module nearest to the A3VTU is referred to as A and the others as B and C respectively. TRIPLE: This indicates the majority operation mode. Operations are performed by three A3VCPU in parallel.
③	LED display reset switch	Clears the present LED annunciator message. The next message in the annunciator queue is then displayed where appropriate.
④	RUN LED	This indicates system operation. Light: The system is operating when the key switch is in the RUN or PAUSE position. Extinguish: When the system is stopped due to the key switch being in the STOP or PAUSE position or due to a WDT ERROR error being generated during self-diagnosis. Flicker: Self-diagnosed error has occurred. (Operation will continue if the error detected has been specified in the parameter setting.)
⑤	RUN/STOP switch	RUN/STOP: To start/terminate running the PC program. PAUSE: To terminate running the PC program and maintain output status. RESET: To run hardware resets of the A3VTU and A3VCPU modules, when abnormal operation occurs, and when operations are initialized.
⑥	Cassette case	Only the memory cassette case is installed since user memory in the A3VCPU module is not used.
⑦	RS-422 connector	Not used. (Normally covered)
⑧	Master station link module operation/ standby switch	This manual switch is used to switch between operation and standby status of two link modules when used in the master station of a data link system. Pressing the button will set one of the two link modules to the operate mode and the other the standby. Push button operation is disabled when not used in the data link system.

4.12.3 Nomenclature (A3VCPU)



No.	Description	Application
①	LED display	Displays an error message produced during self- diagnosis and annunciator F number or comments arising from the SET F and OUT F instructions. 16-character display possible. (The possible display characters are alphanumeric and twenty-eight special characters.)
②	Reset key switch	RESET: Hardware reset. Used to reset the CPU after an operation error and to initialize operation. The latch memory is not cleared when the CPU is reset. LATCH CLEAR: Sets all latch area data (as defined in parameters) to OFF or 0. (Valid when the CPU is in STOP status)
③	LED display reset switch	Clears the present LED annunciator message. The next message in the annunciator queue is then displayed where appropriate.
④	RUN LED	Indicates the run status of the CPU. On: The CPU is in RUN or STEP-RUN status, no operation errors have occurred, the program is being run and the PC is active. Off: The CPU is in STOP, PAUSE or STEP-RUN status and the program is not being run. Light when a CPU other than the operating CPU during independent operations. Light when the WAIT status is set while operations are performed in the majority operations mode. Flicker: Self-diagnosed error has occurred. (Operation will continue if the error detected has been specified in the parameter setting.)
⑤	RUN/STOP switch	RUN/STOP: To start/terminate running the PC program. REPAIR: The sequence program calculations are performed. There is no module verification. (Used during replace of I/O modules) STEP RUN: Do not use this function.
⑥	Memory cassette release button	To remove the memory cassette, press the buttons in two locations, disengage the memory cassette from the connectors by raising it approximately 5mm (0.20in.) and then remove the cassette module.
⑦	Memory cassette loading connector	Used to connect the memory cassette to the CPU.
⑧	RS-422 connector	Peripheral programmer port. Fit cover (supplied) when not in use.

5. OPERATION MODE

The A3VTS system operation provides two types of operation status described below. Both are referred to as operation mode in this manual.
The operation mode setting is selected with the operation mode setting key switch located on the front panel of the A3VTU.

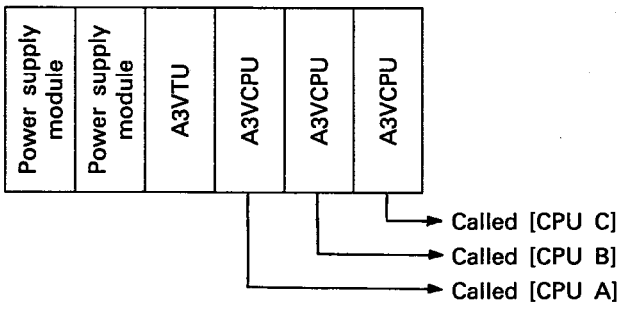
- Operation mode
  - Independent operation mode
  - Majority operation mode
    - Majority operation: Normal operation using three A3VCPU modules
    - Single-module operations: Operations are performed by a single A3VCPU module when a malfunction occurs.

(1) An A3VTU and a single A3VCPU module is used in the independent operation mode. This mode is selected by setting the operation mode setting key switch located on the front panel of the A3VTU to either [CPU A], [CPU B] or [CPU C]. In this mode, an A3VCPU module is operated independently. The independent operation mode is convenient for debugging operations.

(2) An A3VTU and three A3VCPU modules are used in the majority operation mode. This mode is selected by setting the operation mode setting key switch located on the front panel of the A3VTU to [TRIPLE]. Majority operations are performed if all three A3VCPU modules function normally. Single-module operation is performed by a normal single A3VCPU module and the A3VTU in this mode if any single A3VCPU module cannot operate.

(3) The operation mode setting is determined by the position of the operation mode setting key switch when the power is applied to the A3VTU or when the RUN/STOP key switch is set to RESET. The operation mode does not change even if the setting of the operation mode setting key switch is changed while the power is ON.
The power must be turned off one time and then turned on again or the RUN/STOP key switch must be set to RESET when the operation mode is changed.

(4) The descriptions CPU A, CPU B and CPU C in this manual are the same as the [A], [B] and [C] displayed on the operation mode setting key switch. The three A3VCPU modules are assigned the names of CPU A, CPU B, and CPU C, CPU A being the one closest to the A3VTU and CPU C the farthest.



5.1 Independent Operation Mode

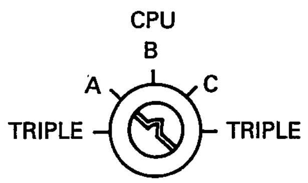
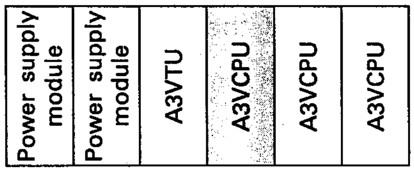
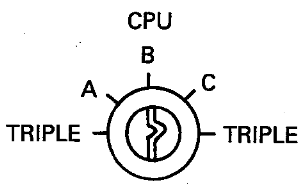
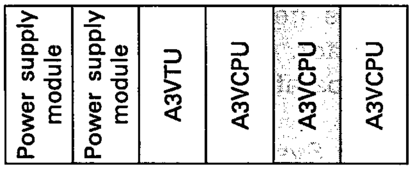
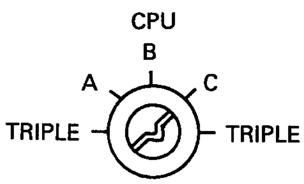
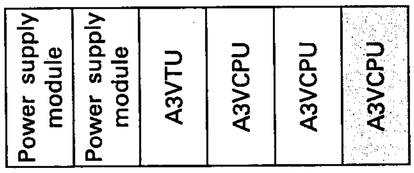
The independent operation mode is performed by the A3VTU and a single A3VCPU unit. This mode is selected by setting the operation mode setting key switch located on the front panel of the A3VTU which to [CPU A], [CPU B] or [CPU C]. Independent operations are performed in this mode by the A3VTU and the A3VCPU module that corresponds with the key switch setting. This mode will be referred to as the independent operation mode from now on.
The independent operation mode is a convenient mode to use when debugging system operations; the offline switch function, forced output or the remote RUN/PAUSE operations by the peripheral device.

(1) System operations stop if operations cannot be performed due to a malfunctioning A3VCPU module during independent operations.
Automatic switching to other A3VCPU modules cannot be performed even if they are installed.

(2) When the system stops due to a malfunction during independent operations, system operations can be started again if other A3VCPU modules are installed. Set the operation mode setting key switch to the selection position of another A3VCPU module that is operating and then set the A3VTU RUN/STOP key switch to the RESET position.

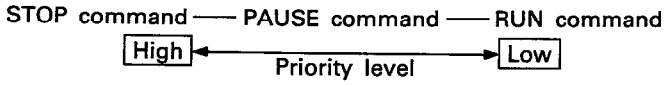
(3) A3VTU control is disabled when independent operations are performed except for the A3VCPU module that is set by the A3VTU operation mode setting key switch.
As a result, the A3VCPU module that is separated from the control cannot perform I/O control and monitor the input status even if the RUN/STOP key switch is set to RUN.
System operations are not influenced even if the separated A3VCPU module malfunctions because it is ignored by the A3VTU.

(4) The relation between the operation mode setting key switch and the operating CPU module when independent operations are performed is described as follows.

Operation Mode Setting Switch	Switch Settings and Operating CPU Relationship	
		The ▢ part of the A3VCPU module is the operating CPU and this CPU performs operations.
		The ▢ part of the A3VCPU module is the operating CPU and this CPU performs operations.
		The ▢ part of the A3VCPU module is the operating CPU and this CPU performs operations.

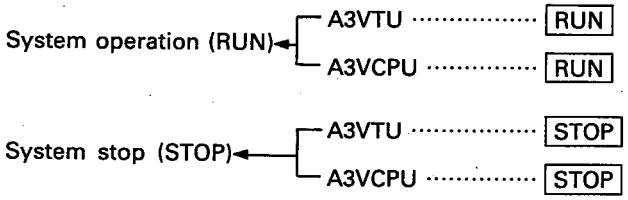
5.1.1 System operation status in the independent operation mode

The system operation status in the independent operation mode is determined by the A3VTU and A3VCPU module status and external instructions.
The priority level for each of A3VTU and A3VCPU module status is described below. System operation status is determined in the order of the highest priority level.



The general system status as well as the separate factors that determine each system operation status are explained below. The items described below are organized separately by each factor. Please refer to Appendix 6 for the system status when separate factors are combined.

(1) System RUN/STOP operation
Position the RUN/STOP key switch of the A3VTU or A3VCPU module in the locations shown below to start or stop the system operations.



Set the A3VTU RUN/STOP key switch to the appropriate position to operate or stop the system.

(2) Remote RUN/STOP instruction:
When the Remote RUN/STOP operation is performed to change the system status by an external instruction, first set the A3VTU and A3VCPU module key switch as shown below. Then perform the Remote RUN/STOP operation by the ON/OFF setting of the Remote RUN/STOP contacts or the Remote RUN/STOP instruction from the peripheral device.

Remote RUN/STOP contact

System operation (RUN) ←
- A3VTU ····· RUN/STOP key switch [RUN]
- A3VCPU ···· RUN/STOP key switch [RUN]
- Remote RUN/STOP contact [OFF]

System operation (RUN) ←
- A3VTU ····· RUN/STOP key switch [RUN]
- A3VCPU ···· RUN/STOP key switch [RUN]
- Remote RUN/STOP contact [ON]

Peripheral device

System operation (RUN) ←
- A3VTU ····· RUN/STOP key switch [RUN]
- A3VCPU ···· RUN/STOP key switch [RUN]
- Remote RUN instruction in the peripheral device test mode

System operation (RUN) ←
- A3VTU ····· RUN/STOP key switch [RUN]
- A3VCPU ···· RUN/STOP key switch [RUN]
- Remote STOP instruction in the peripheral device test mode

System operation status varies for combinations other than those described above. Refer to Appendix 6 for further details.

(3) PAUSE instruction

There are three ways to set the system to the PAUSE status. These settings can be performed by the A3VTU RUN/STOP key switch, the remote PAUSE contact or by a peripheral device. The setting and operation procedures are explained below:

A3VTU key switch

System PAUSE status ← A3VTU ····· RUN/STOP key switch [PAUSE]
A3VCPU ···· RUN/STOP key switch [RUN]
M9040 [ON]

Remote PAUSE contact

System PAUSE status ← A3VTU ····· RUN/STOP key switch [RUN]
A3VCPU ···· RUN/STOP key switch [RUN]
M9040 [ON]
Remote PAUSE contact [ON]

Peripheral device

System PAUSE status ← A3VTU ····· RUN/STOP key switch [RUN]
A3VCPU ···· RUN/STOP key switch [RUN]
Remote PAUSE instruction in the peripheral device test mode

The system operation status varies for combinations other than those described above. Refer to Appendix 6 for further details.

(4) [STOP] command

Perform the following operations to stop the system with the [STOP] command in the sequence program.

System stop ← A3VTU ····· RUN/STOP key switch [PAUSE]
A3VCPU ···· RUN/STOP key switch [RUN]
[STOP] instruction execution contact [ON]

(5) The system operation status is determined by combinations of each of the factors described above.
The status for the RUN LED of the A3VTU and the A3VCPU module at each system operation status is shown below.

System Operation Status	Contents
RUN	• The A3VTU and A3VCPU module RUN LED light. • The sequence program operation is executed.
PAUSE	• The A3VTU and A3VCPU module RUN LED extinguish. • Operations stop with output maintained.
STOP	• The A3VTU and A3VCPU module RUN LED extinguish. • The output is set OFF and operations stop.
Error	• The A3VTU and A3VCPU module RUN LED flash. • The output is set OFF and operations terminated.

The A3VCPU module is separated from operation.	• The RUN LED extinguishes disregarding of the key switch position. • The sequence program operation is terminated. • Communication with the peripheral device is possible.

5.2 Majority Operation Mode

The majority operation mode uses the A3VTU and three A3VCPU modules.
This mode is selected when the operation mode setting key switch located on the front panel of the A3VTU is set to [TRIPLE] and the three A3VCPU modules operate in parallel using majority logical operators.
In this section, the term majority operation is used to refer to the operations performed by three A3VCPU modules. Single-module operation refers to operations performed by a single A3VCPU module if a malfunction occurs.
Refer to Section 5.2.2 for an description of the system operation status when a malfunction occurs.

(1) Continuous system operations can still be performed in the majority mode without having to stop operations, even when there is only one other A3VCPU module that is operating normally and one or two A3VCPU modules are determined to be malfunctioning and removed from operation by the A3VCPU module or A3VTU self-diagnosis function.

(2) A majority logical operation is performed on the output data (Y) sent from each A3VCPU module when majority operations are performed. When a difference exists between one of the A3VCPUs and the others, the differing A3VCPU generates an error.
The system continues operation using the other two normal A3VCPUs.

(3) The A3VTU always supervises the three A3VCPU modules when majority operations are performed. Besides output (Y), majority operation provides execute timing for the A3VCPU module instructions indicated below.
When one of the three A3VCPU modules reaches one of the instructions described below, the A3VTU waits for the other A3VCPU modules to execute the instruction simultaneously. When the other A3VCPU modules do not reach the instruction after a fixed period of time elapses, a handshake error [ERROR CPU [ ] [ ]] or a time check error [TIME OVER CPU [ ]] message is returned, an error is generated in the A3VCPU module and is dropped from operation.

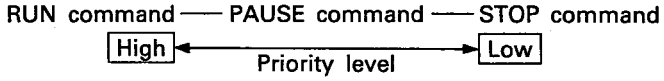
FROM	TOP	SEG	STOP
FROMP	DTO	PR	SUB
DFRO	DTOP	PRC	LRDR
DFROP	END	CHG	LWTP
TO	FEND		

(4) An A3VCPU that is malfunctioning or has been set in the WAIT status due to one of the reasons given in items (2) or (3) should be replaced. A module can be restored to operation by remedying the cause of the error, standardizing the program with that of other modules, or taking whatever action appropriate.
Replacing a malfunctioning A3VCPU or one that is in the WAIT status should promptly be replaced with another module or repaired. Advantage should be taken of the system since it is configured so as to improve operating ratio and reliability.

(5) System operation stops when all three A3VCPU modules malfunction in the majority operation mode.

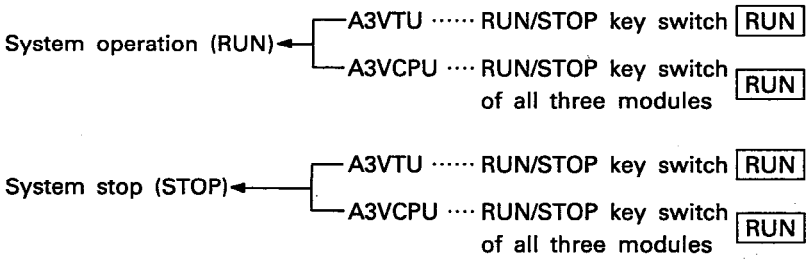
5.2.1 System operation status in the majority operation mode

The system operation status in the majority operation mode is determined by the status of the A3VTU and three A3VCPU modules (except for the A3VCPU module in the error or wait status) and external instructions.
The [STOP] instruction from the A3VTU RUN/STOP key switch has the highest priority to determine the A3VTS system operation status.
When the A3VTU is not set to [STOP], system operation status is determined by the operation status of the three A3VCPU modules, and if one of the three A3VCPUs has a higher level of priority than the others, the operation status of the system is the same as that of the A3VCPU with the highest priority. Priority level of individual instructions is shown below.



The general system status as well as the separate factors that determine each system operation status are explained below. The items described below are organized separately by each factor. Please refer to Appendix 6 for the system status when separate factors are combined.

(1) System RUN/STOP operation
Position the RUN/STOP key switch of the A3VTU or A3VCPU module in the locations shown below to start or stop the system operations.



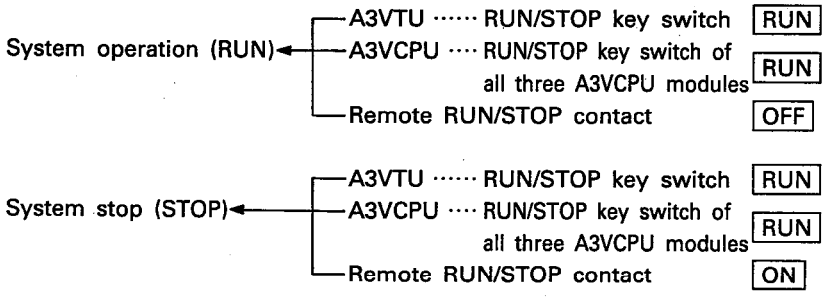
POINT

The system operates if the RUN/STOP key switch of even one A3VCPU module is set to [RUN] during system operation. However, operation is conducted with one module only and the other A3VCPU modules are dropped from operation.

Set the A3VTU RUN/STOP key switch to the appropriate position to operate or stop the system.

(2) Remote RUN/STOP instruction:
When the Remote RUN/STOP operation is performed change the system status by an external command, first set the A3VTU and A3VCPU module key switch as shown below. Then perform the Remote RUN/STOP operation by the ON/OFF setting of the Remote RUN/STOP contacts or the Remote RUN/STOP command.

Remote RUN/STOP contact



POINT

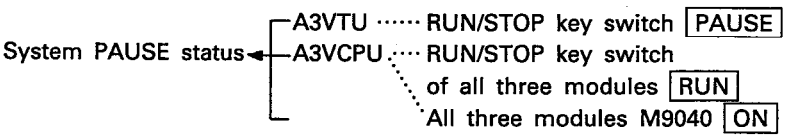
For Remote RUN/STOP operation, it is also possible to use the instructions from a peripheral device but this should not be used in the majority operation mode. Use of the method requires that instructions be sent simultaneously to all three A3VCPU modules. However, discrepancies in the timing at a particular A3VCPU will result in its generating an error and being dropped from operation.

5

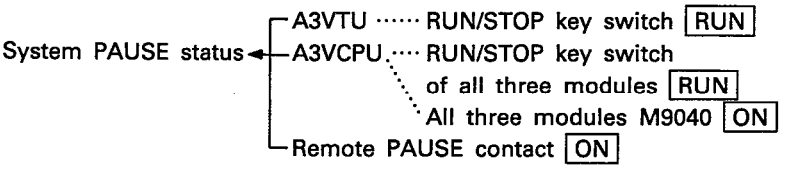
System operation status varies for combinations other than those described above. Refer to Appendix 6 for further details.

(3) PAUSE command
There are two ways to set the system to the PAUSE status. One uses the A3VTU RUN/STOP key switch and the other the remote PAUSE contact.
The setting and operation procedures are explained below.

A3VTU key switch



Remote PAUSE contact

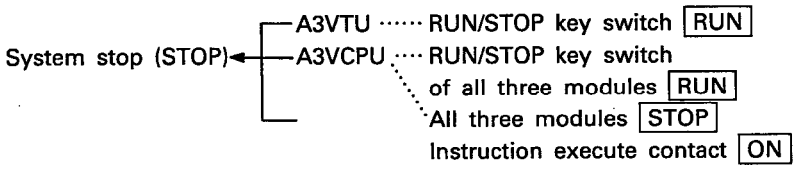


POINT

For Remote PAUSE operation, it is also possible to use the instructions from a peripheral device but this should not be used in the majority operation mode. Use of the method requires that instructions be sent simultaneously to all three A3VCPU modules. However, discrepancies in the timing at a particular A3VCPU will result in its generating an error and being dropped from operation.

System operation status varies for combinations other than those described above. Refer to Appendix 6 for further details.

(4) [STOP] instruction
Perform the following operations to stop the system with the [STOP] instruction ion the sequence program.



(5) The system operation status is determined by combinations of each of the factors described above.
The status for the RUN LED of A3VTU and the A3VCPU module at each system operation status is shown below.

System Operation Status	A3VCPU Module Operation Status	Remarks
RUN	RUN	The A3VTU and A3VCPU module [RUN] LEDs light. The sequence program operation is executed.
	Standby	The A3VCPU module on the right becomes the operating CPU and the other module becomes the standby module when majority operations are performed. A3VTU and A3VCPU [RUN] LEDs light. Sequence program operation is executed but output data stops at the A3VTU.
PAUSE	PAUSE	The A3VTU and A3VCPU module [RUN] LEDs extinguish. Operations stop with output maintained.
STOP	STOP	The A3VTU and A3VCPU module [RUN] LEDs extinguish. The output is set OFF and operations stop.
RUN, PAUSE or STOP	WAIT	The A3VCPU module enters the WAIT state when it is in either the STOP or PAUSE status during system operations. The A3VCPU module [RUN] LED extinguishes. The A3VCPU module is waiting for restore.
RUN, PAUSE, STOP or error	Error	The A3VCPU module [RUN] LED extinguishes. Return to operation by replacing malfunctioning CPU or eliminating the cause of error.

5.2.2 Operation status when there is a malfunction

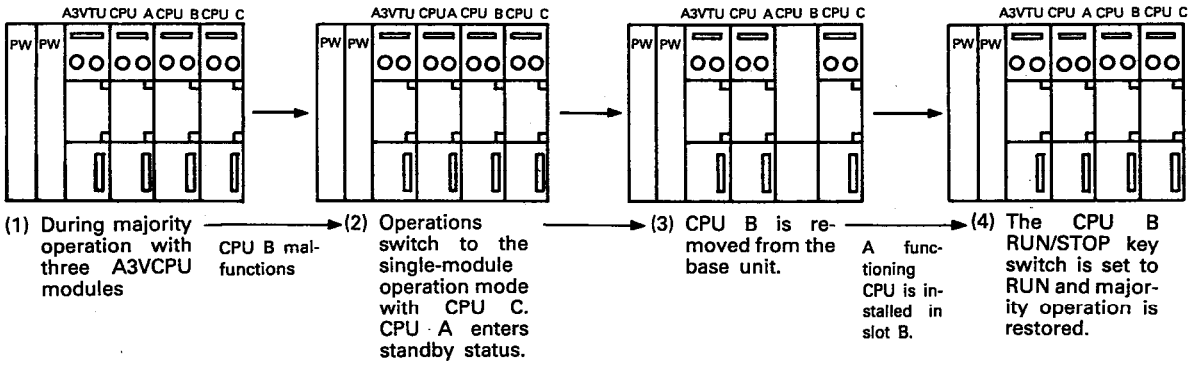
This section describes what occurs in each A3VCPU module operation status and system operation status when a self-diagnosis error or majority decision error is generated during majority operations.

(1) Processing when there is a malfunction

(a) The A3VTU manages each A3VCPU module operation status and determines the switching of CPUs when a malfunction occurs.

(b) If even one of the A3VCPU modules malfunctions during majority operation or the WAIT status is set, operations switch the single-module operation mode to continue system operations.

(c) When single-module operation is set, the CPU to the right of the CPU that was stopped due to malfunction has priority and performs operations. The output data (Y, B, and W) from this CPU is output through the A3VTU to the I/O modules.
Examples of the CPU switching and the various CPU operation status are described below.



Operation status of the system and the A3VCPU modules

System	RUN
CPU A	RUN
CPU B	RUN
CPU C	RUN

System	RUN
CPU A	Standby
CPU B	Error
CPU C	RUN

System	RUN
CPU A	Standby
CPU B	Error
CPU C	RUN

System	RUN
CPU A	RUN
CPU B	RUN
CPU C	RUN

(d) When operation shifts to the single-module operation because a malfunction occurs and there are two functioning A3VCPU modules, the operation status of each CPU becomes as follows.

- The A3VCPU module to the right of the malfunctioning CPU outputs data (Y, B, W) to external I/O modules under A3VTU management and is referred to as the operation CPU.
- For the other functioning module, data is input in the same manner as the operating CPU, but output data is not output to external I/O modules. This CPU is referred to as the standby CPU.

When there is only one functioning A3VCPU module, there is no standby CPU. The flow of I/O data during single-module operation when a malfunction has occurred is shown in Fig. 5.1 on the next page.

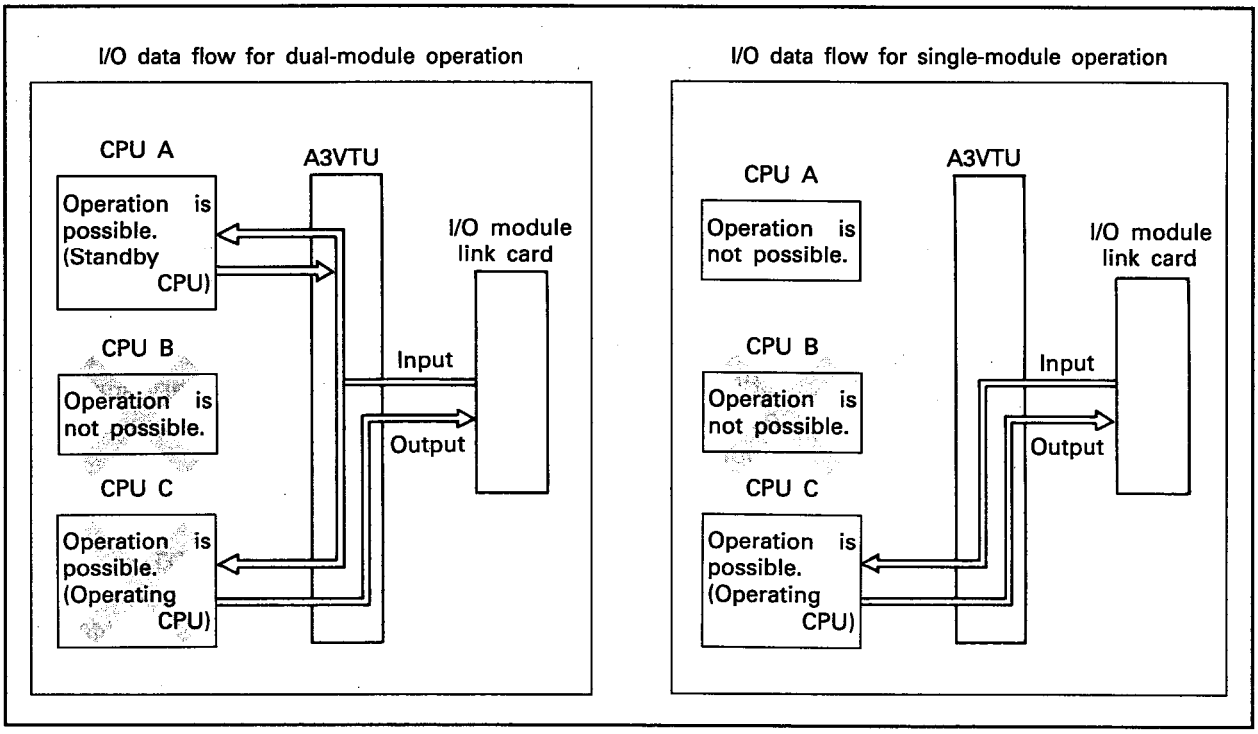


Fig. 5.1 I/O Data Flow when a Malfunction Occurs

(2) A3VCPU module operation restore processing

(a) Even when single-module operation has been set due to error generation, the A3VTU can check the items listed below in relation to each of the A3VCPUs and determine whether or not majority operation can be set again or not.

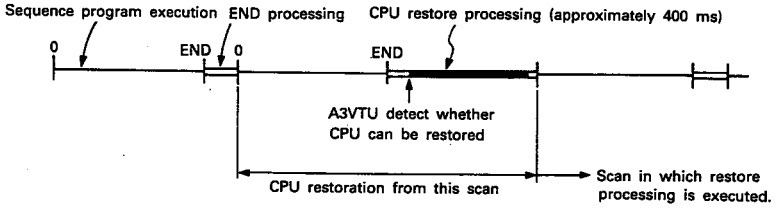
- Perform communication and check for replies.
- Check if an error is being generated that may prevent operations.
- Check if the operation status is the same as the system status.

If the three items described above are satisfactory, the corresponding A3VCPU operation is restored.

(b) If an A3VCPU module is in the error or wait status, eliminate the source of the error and restore the module to operation by either resetting the CPU or replacing the malfunctioning A3VCPU module with a functioning A3VCPU module.

(c) During the END processing, the A3VTU checks whether an A3VCPU which has been malfunctioning can restore the operation. When it is determined that operation is possible the processing shown below is executed immediately and operations are restored from the next scan.

- The entire contents of the data memory are transferred from the operating CPU to the restored CPU.
- The A3VTU outputs the RUN instruction to the restored CPU.



CPU restore processing is executed once every scan. It is executed during END processing while the system is operating.

Approximately 400ms is required for CPU restore processing.

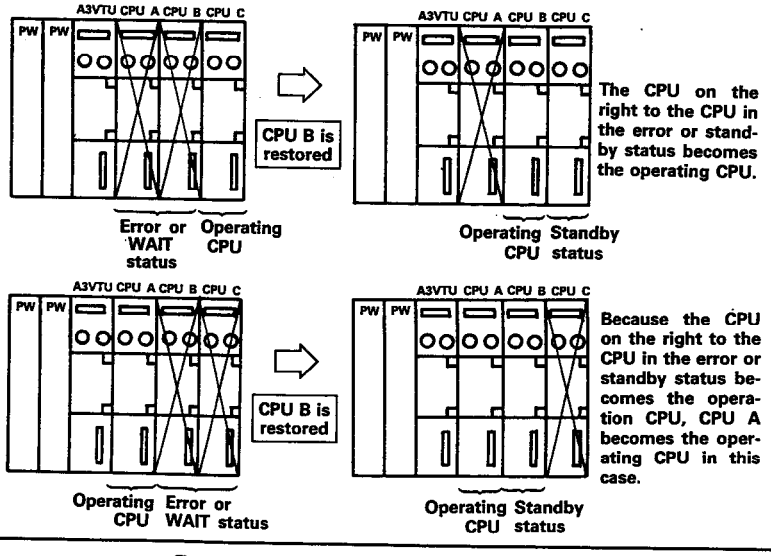
Set the time setting of the watchdog timer (WDT) to a value equal to the maximum time for the regular scan plus the time required for the CPU restore processing (400ms) when majority operation is performed.

A "WDT ERROR" error is generated during the CPU restoration when the set value is insufficient.

POINT

When one of two A3VCPUs that have generated an error or are set to in the WAIT status can be restored to operation, that A3VCPU is set to the standby status. In such a case, the process detailed in (c) is executed. However, there are times when the CPU in the operation status will be set to standby and the restored CPU will be set to the operation status when the physical location of the A3VCPU requires such be done.

Example

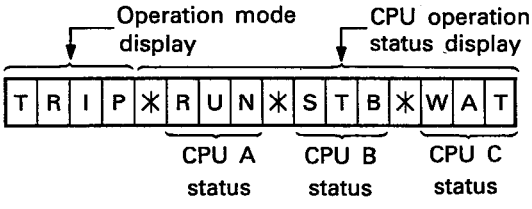


5.3 Operation Mode Display

The LED display located on the front panel of the A3VTU module can indicate the operation mode and the operation status of the three A3VCPU modules in addition to the error messages. The meaning of the display messages is described below.

(1) Error messages are given priority over all other displays during operation mode. Therefore, an error message is displayed if an error is generated even when an operation mode message has been displayed.
The normal operation mode message can be redisplayed by pressing the indicator reset switch located on the front panel of the A3VTU module after an error has been corrected.
However, if another malfunction occurs, the corresponding error message is displayed automatically after the operation mode has been displayed for approximately 5 seconds.

(2) The display format of the operation mode on the LED display located on the front panel of the A3VTU module is shown below.



The display on the left is an example of operation mode message display during majority decision operation; CPU A in the operation, CPU B in the standby status, and CPU C in the WAIT status.

(3) The messages displayed in the LED display panel and their meanings are described below.

Display	Message	Meaning
Operation mode display	TRIP	Majority operation mode
	CPU A	Independent operation by CPU A in the independent operation mode
	CPU B	Independent operation by CPU B in the independent operation mode
	CPU C	Independent operation by CPU C in the independent operation mode
CPU operation status display	RUN	Corresponding CPU is in the RUN status. This is the operating CPU.
	STB	Corresponding CPU is in the RUN status. This is the standby CPU).
	PSE	Corresponding CPU is in the PAUSE status.
	STP	Corresponding CPU is in the STOP status
	WAT	Corresponding CPU is in the WAIT status
	ERR	Corresponding CPU has generated an error. (Operation is not possible.)
	*—	Corresponding CPU has been dropped from operation. (Independent operation mode only)

* When a CPU is dropped from operation, such a status is indicated by [ ]—[ ].

5.4 Operation Precautions

This section describes the cautions concerning operations in the individual operation mode and the majority operation mode.

(1) The system operation can be reset by either turning off the power once and then back it on again or using a reset switch. When resetting with a reset switch use the A3VTU RUN/STOP key switch.

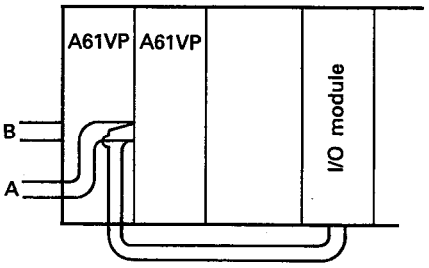
Reset Method	Reset Range
Power supply ON → OFF	All modules are reset
Reset using the A3VTU RUN/STOP key switch	All modules are reset except for AD51E and A81 CPU.
Reset using the A3VCPU module reset switch	Only this A3VCPU module is reset.

(2) The three A3VCPU modules can use peripheral devices. Peripheral devices cannot be connected to the A3VTU. STOP the system when connecting a peripheral device to the A3VCPU module to modify the program, or write the data. RUN the system only after writing the same data to the three A3VCPU modules.
If system operation is started after writing the data to only one or two of the three A3VCPU modules, the remaining A3VCPU module is dropped from operation. Therefore, do not use this procedure for a A3VCPU module that is running while the system is in the RUN status. The system will stop sometimes if attempted.

(3) Always use the A3VCPU module RUN/STOP key switch to RUN or STOP the system in the majority operation mode.
In the majority operation mode, the system is in the RUN status even if only one of the three A3VCPU modules is in the RUN mode. Even if the A3VCPU module RUN/STOP key switch is set to STOP with the A3VTU RUN/STOP key switch set in the RUN, the system will RUN as long as the other A3VCPU module operation status is RUN.

Except when replacing the A3VCPU module, the A3VCPU RUN/STOP key switch should be kept in RUN during majority operations. Use the RUN/STOP key switch of the A3VTU to control system RUN and STOP.

(4) When using the power supply module and the I/O module connected in parallel with a 110/220V power supply as shown in the figure on the right, the system will continue to run even if the power supply of the A system in the figure goes OFF.



However, since the power supply to the I/O module is set OFF, all data operations are all set OFF and normal operation cannot be performed.

(5) When restoring the A3VCPU module that is in the WAIT status, and if a message is displayed on the A3VCPU module LED panel, press the INDICATOR RESET button repeatedly until a message no longer displayed. Sometimes, if restore processing is performed while a message is being displayed, a handshake error "ERROR CPU [ ][ ]" occurs and restoration is precluded.

6. POWER SUPPLY MODULE

6.1 Power Supply Module Specifications

This section describes the specifications and selections for the power supply module.

6.1.1 Power supply module specifications

The power supply module specifications are indicated in the following table.

Item		Specifications					
		A61VP	A61P	A62P	A63P	A65P	A66P
Base loading position		Power supply slot	Power supply slot	Power supply slot	Power supply slot	Power supply slot	I/O module loading slot
Input voltage		100—120V AC +10%, −15% (85 to 132V AC)			24V DC +30%, −35% (15.6 to 31.2V DC)	100—120V AC +10%, −15% (85 to 132V AC)	
		200—240V AC +10%, −15% (170 to 264V AC)				200—240V AC +10%, −15% (170 to 264V AC)	
Input frequency		50/60Hz ± 5%			—	50/60Hz ± 5%	
Max. input apparent power		110VA			65W	110VA	95VA
Inrush current		20A, within 8ms			100A, within 1ms	20A, within 8ms	
Rated output current	5V DC	8A	8A	5A	8A	2A	—
	24V DC ±10%	—	—	0.8A	—	1.5A	1.2A
*1 Overcurrent protection	5V DC	8.8A or higher	8.8A or higher	5.5A or higher	8.5A or higher	2.2A or higher	—
	24V DC	—	—	1.2A or higher	—	2.3A or higher	1.7A or higher
*2 Overvoltage protection	5V DC	5.5 to 6.5V	5.5 to 6.5V	5.5 to 6.5V	5.5 to 6.5V	5.5 to 6.5V	
	24V DC	—	—	—	—	—	—
Power supply ON terminal, rated switching voltage and current							250V AC 2A 30V DC 2A
Efficiency		65% or higher					
Power indicator		Power LED display					
Terminal screw size		M4 × 0.7 × 6					M3 × 0.5 × 6
Applicable wire size		0.75 to 2mm² (18 to 14 AWG)					
Applicable solderless terminal		V1.25-4, V1.25-YS4A, V2-S4, V2-YS4A					V1.25-3, V1.25-YS3A, V2-S3, V2-YS3A
Applicable tightening torque		12kg·cm (10.39 lb·inch)					7kg·cm (6.06 lb·inch)
External dimensions mm(inch)		250(9.84) × 55(2.17) × 121(4.76)					250(9.84) × 37.5(1.48) × 121(4.76)
Weight kg(lb)		0.95(2.09)	0.98(2.16)	0.94(2.07)	0.8(1.76)	0.94(2.07)	0.75(1.65)

Table 6.1 Power Supply Module Specifications

POINT

***1: Overcurrent protection**

**The overcurrent protection device shuts off the 5V, 24V DC circuit and stops the system if the current flowing in the circuit exceeds the specified value.
When this device is activated, the power supply module LED is switched off or dimly lit. In this case, remove any cause of overcurrent and start up the system.
The system is initialized if the current value is the rated value.**

***2: Overvoltage protection**

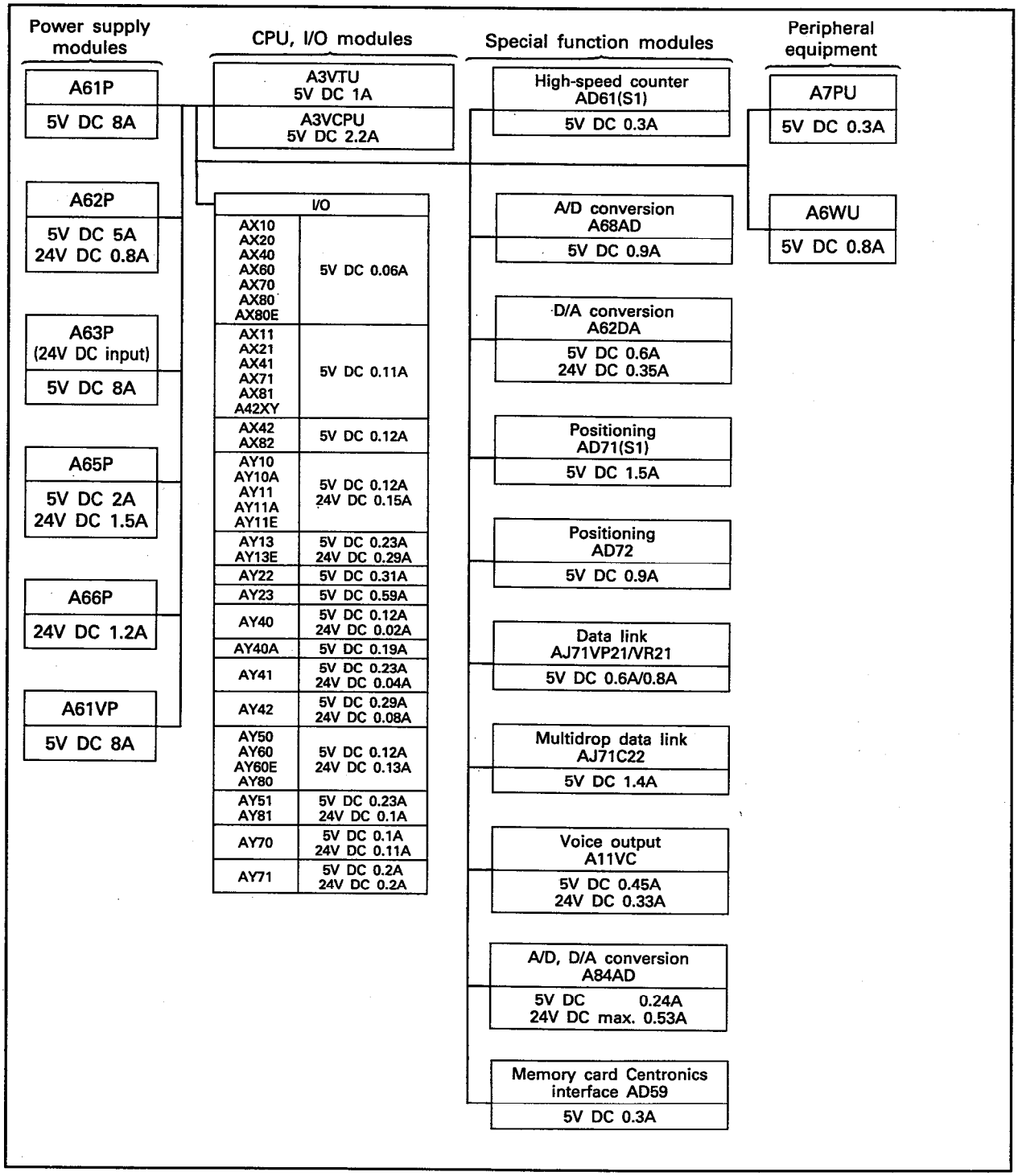
**The overvoltage protection device shuts off the 5V DC circuit and stops the system if 5.5 to 6.5V voltage is applied to the circuit.
When this device is activated, the power supply module LED is switched off. In this case, switch off, then on the input power to restart the system.
The power supply module must be changed if the system is not booted and the LED remains off.**

6.1.2 Selection of power supply module

Select the power supply module according to the total current consumption of I/O modules, special function modules, and peripheral equipment supplied by that power supply module.

(1) Current consumption of each module

The current capacity of each power supply module and the current consumption of each module are indicated below. Select an appropriate power supply module, referring to the values indicated below.



(2) A61VP usage precautions
Always install the two A61VP power supply modules to the dual power supply base unit (A30VB main unit and A68VB extension base unit) as a 2-unit installation.
Normal operations are not possible if the A61VP is installed in the A65B or A68B extension base module. Do not use this installation configuration because it might damage the power supply module.
If the previous power supply modules (A6[ ]P) are installed and used in the A30VB or A68VB, normal operations cannot be performed as described above. Do not use this installation configuration because it might damage the power supply module.

(3) Notes on use of the A66P

(a) Install the A66P module in the rightmost slot of the base unit, or its right slot must be occupied with a dummy module or blank cover, or left empty.

(b) The A66P output current (24V DC) depends on the left-hand adjacent module.

Left Hand Adjacent Module	Power Supply Module	Input Module Dummy Module	Output Module Special Function Module	Vacant
Configuration	Power supply module / A66P / Vacant	Input module Dummy module / A66P / Vacant	Output module Special function module / A66P / Vacant	Vacant / A66P / Vacant
Max. output current for 24V DC	0.5A	1.2A	1.0A	1.5A

6.1.3 Fuse specifications

This section describes the specifications of fuses used for the power supply modules and output modules.

Item \ Type	GTH4	SM6.3A	MF51NM8	HP-32	HP-70K	MP-20	MP-32	MP-50
Application	For power supply A61P, A62P, A61VP, A65P, A66P	For power supply A63P	For output AY11E, AY13E	For output AY23	For output AY22	For output AY50, AY80	For output AY60	For output AY60E
Shape	Cartridge type	Cartridge type	Cartridge type	Plug type	Plug type	Plug type	Plug type	Plug type
Rated current	4A	6.3A	8A	3.2A	7A	2A	3.2A	5A
External dimensions mm(inch)	φ6(0.24) × 32(1.26)	φ6(0.24) × 32(1.26)	φ5.2(0.20)× 20(0.79)	30.3(1.19) × 8(0.31) × 20(0.79)	30.3(1.19) × 8(0.31) × 20(0.79)	17.2(0.68) × 5.5(0.22) × 19(0.75)	17.2(0.68) × 5.5(0.22) × 19(0.75)	17.2(0.68) × 5.5(0.22) × 19(0.75)

Table 6.2 Fuse Specifications

6.2 Handling

This section gives handling instructions, PC nomenclature and hardware setting instructions.

6.2.1 Handling instructions

The handling precautions for the power supply module from removing it from the shipping container to installation are described in this section.

(1) Do not subject the power supply module and memory cassette to impact or shock.

(2) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards. This may cause damage.

(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Tighten the module mounting and terminal screws as specified below.

Screw	Tightening Torque kg·cm (lb·inches)
Module terminal block installation screws (M3)	5 (4.33) to 8 (6.93)
Module terminal block installation screws (M4)	10 (8.66) to 14 (12.13)
Module mounting screws (optional) (M4)	8 (6.93) to 12 (10.39)

(5) After mounting the module in the base unit, ensure that the hook is locked in the base unit securely. When removing the module, press the hook until it is completely free from the base and then pull the module forward. (Refer to Section 10.5 for further details.)

6.2.2 Nomenclature

(1) Nomenclature of A61VP module

Module fixing hook
Hook for fixing the module to the base unit.

"POWER" LED
AC power supply and internal DC power supply indicator indicating LEDs
The POWER LED extinguishes when the fuse blows or the power supply malfunctions.

"OVERHEAT" LED
This LED lights when the power supply overheats. (Refer to Chapter 13).

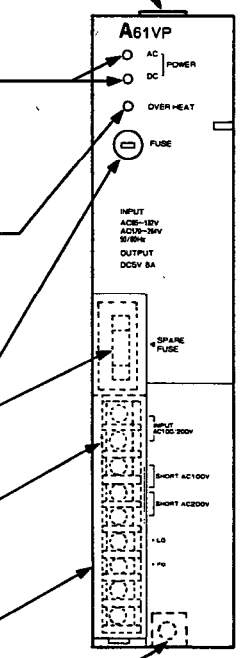
Power fuse, fuse holder
4A cartridge fuse for AC input power is fixed by the fuse holder.

Spare fuse for power supply
Spare fuse for power supply installed to the rear side of terminal cover.

Terminal block
For details, see below. (Located under the terminal cover)

Terminal cover
Cover for protection of terminal block. Remove during wiring. Install after wiring.

Module fixing screw mounting hole
Allows fixing the module with a screw in addition to the module fixing hook. (For M4 screw)



Terminal details

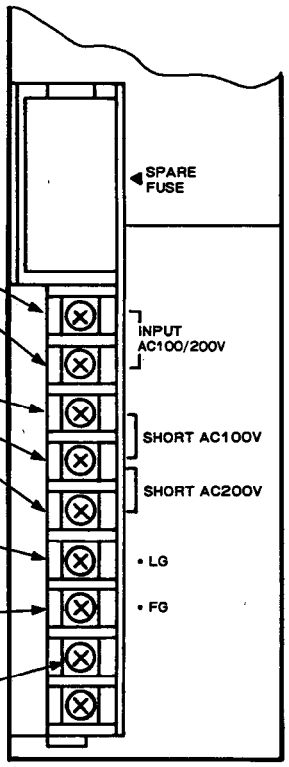
Power input terminals
Power input terminals to which AC power of 100V AC or 200V AC is connected.

Applied voltage select terminals
Terminals for selecting applied voltage. Use 100V AC or 200V AC as described below. When 100V AC is input, connect together the "SHORT AC 100V" terminals with the attached short chip. When 200V AC is input, connect together the "SHORT AC 200V" terminals with the attached short chip.

LG terminal
Grounding of power filter. Has half the input potential.

FG terminal
Connection terminal connected to the shielding pattern on printed circuit board.

Terminal screw
M4 × 0.7 × 6



(2) Nomenclature of A61P module

Module fixing hook
Hook for fixing the module to the base unit.

"POWER" LED
LED for indicating 5V DC power

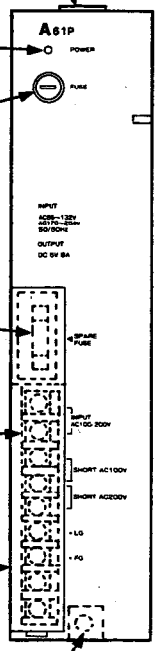
Power fuse, fuse holder
4A cartridge fuse for AC input power is fixed by the fuse holder.

Spare fuse for power supply
Spare fuse for power supply installed to the rear side of terminal cover.

Terminal block
For details, see below. (Located under the terminal cover)

Terminal cover
Cover for protection of terminal block. Remove during wiring. Install after wiring.

Module fixing screw mounting hole
Allows fixing the module with a screw in addition to the module fixing hook. (For M4 screw)



6

Terminal details

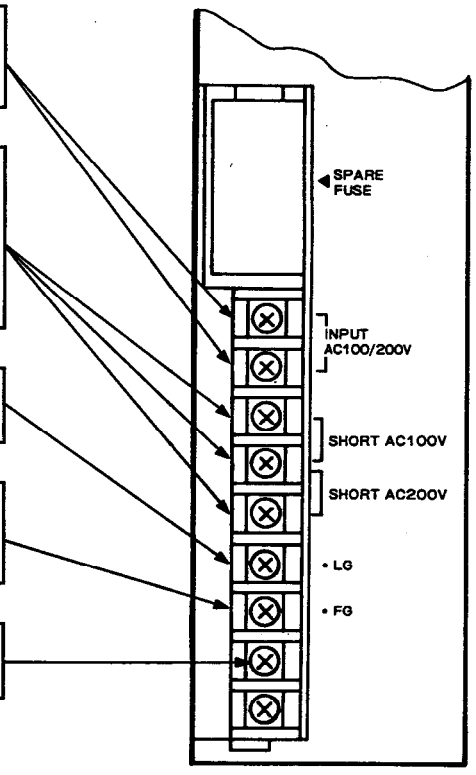
Power input terminals
Power input terminals to which AC power of 100V AC or 200V AC is connected.

Applied voltage select terminals
Terminals for selecting applied voltage. Use 100V AC or 200V AC as described below. When 100V AC is input, connect together the "SHORT AC 100V" terminals with the attached short chip. When 200V AC is input, connect together the "SHORT AC 200V" terminals with the attached short chip.

LG terminal
Grounding of power filter. Has half the input potential.

FG terminal
Connection terminal connected to the shielding pattern on printed circuit board.

Terminal screw
M4 × 0.7 × 6



(3) Nomenclature of A62P, A65P module

Module fixing hook
Hook for fixing the module to the base unit.

"POWER" LED
LED for indicating 5V DC power

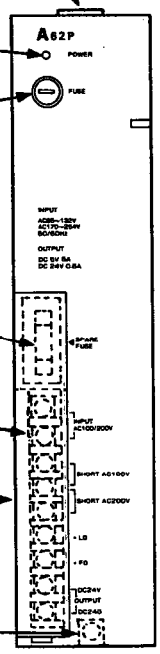
Power fuse, fuse holder
4A cartridge fuse for AC input power is fixed by the fuse holder.

Spare fuse for power supply
Spare fuse for power supply installed to the rear side of terminal cover.

Terminal block
For details, see below. (Located under the terminal cover)

Terminal cover
Cover for protection of terminal block. Remove during wiring. Install after wiring.

Module fixing screw mounting hole
Allows fixing the module with a screw in addition to the module fixing hook. (For M4 screw)



Terminal details

Power input terminals
Power input terminals to which AC power of 100V AC or 200V AC is connected.

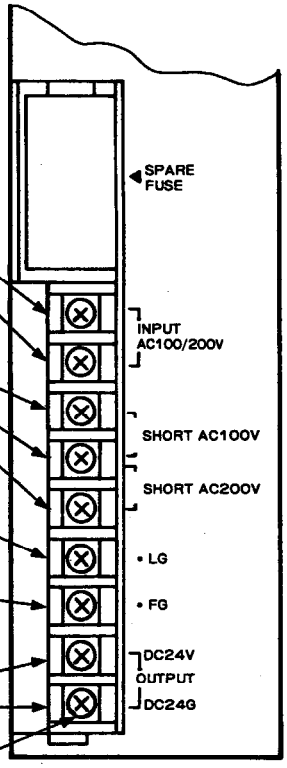
Applied voltage select terminals
Terminals for selecting applied voltage. Use 100V AC or 200V AC as described below. When 100V AC is input, connect together the "SHORT AC 100V" terminals with the attached short chip. When 200V AC is input, connect together the "SHORT AC 200V" terminals with the attached short chip.

LG terminal
Grounding of power filter. Has half the input potential.

FG terminal
Connection terminal connected to the shielding pattern on printed circuit board.

24V DC, 24G DC terminals
For supply to output module which requires 24V inside the module. (Supplied to the module via external wiring)

Terminal screw
M4 × 0.7 × 6



6

(4) Nomenclature of A63P module

Module fixing hook
Hook for fixing the module to the base unit.

"POWER" LED
LED for indicating 5V DC power

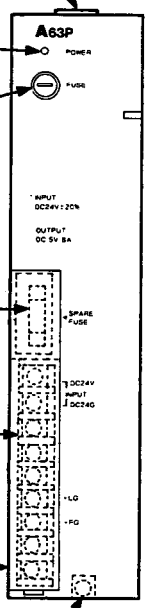
Power fuse, fuse holder
6.3A cartridge fuse for AC input power is fixed by the fuse holder.

Spare fuse for power supply
Spare fuse for power supply installed to the rear side of terminal cover.

Terminal block
For details, see below. (Located under the terminal cover)

Terminal cover
Cover for protection of terminal block. Remove during wiring. Install after wiring.

Module fixing screw mounting hole
Allows fixing the module with a screw in addition to the module fixing hook. (For M4 screw)



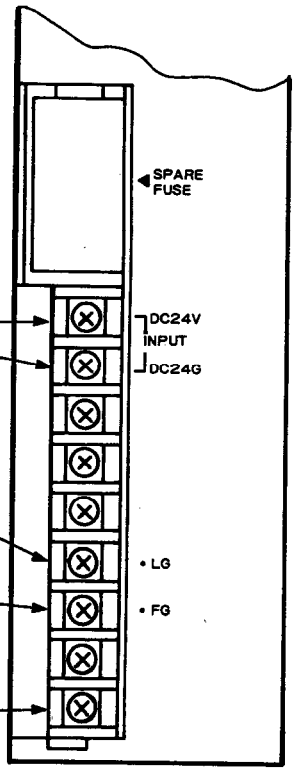
Terminal details

Power input terminals
Power input terminals for 24V DC.
The power fuse will be blown if the positive and negative terminals are reversed.

LG terminal
Grounding of power filter. Has half the input potential.

FG terminal
Connection terminal connected to the shielding pattern on printed circuit board.

Terminal screw
M4 × 0.7 × 6



(5) Nomenclature of A66P module

Module fixing hook
Hook for fixing the module to the base unit.

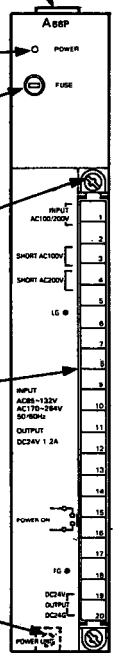
"POWER" LED
LED for indicating 5V DC power

Power fuse, fuse holder
4A cartridge fuse for AC input power is fixed by the fuse holder.

Terminal block fixing screw
Screw for installing and fixing the terminal block to the module.

Terminal block
For details, see below. (Located under the terminal cover)

Module fixing screw mounting hole
Allows fixing the module with a screw in addition to the module fixing hook. (For M4 screw)



Terminal details

Power input terminals
Power input terminals to which AC power of 100V AC or 200V AC is connected.

Applied voltage select terminals
Terminals for selecting applied voltage. Use 100V AC or 200V AC as described below. When 100V AC is input, connect together the "SHORT AC 100V" terminals with the attached short chip. When 200V AC is input, connect together the "SHORT AC 200V" terminals with the attached short chip.

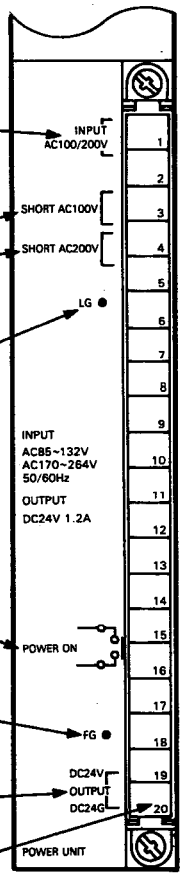
LG terminal
Grounding of power filter. Has half the input potential.

Power ON terminal
Contact terminal which conducts at normal 24V DC output when power input turns on.

FG terminal
Connection terminal connected to the shielding pattern on printed circuit board.

24V DC, 24G DC terminals
For supply to output module which requires 24V inside the module. (Supplied to the unit via external wiring)

Terminal screw
M3 × 0.5 × 6



(6) Setting

In the A61VP, A61P, A62P, A65P and A66P power supply modules the terminals should be short-circuited by the short clip (accessory) according to the supplied voltage value. This section describes how to set the short clip.

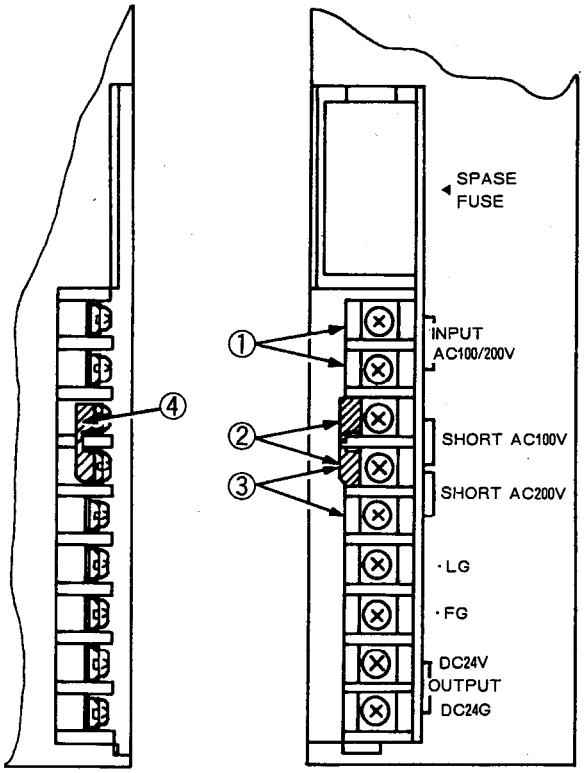
Remove the terminal cover from the power supply module.

↓

Remove the pair of terminal screws, ② or ③, according to the supply voltage range 1 used.
②: For the 100V AC range.
③: For the 200V AC range.

↓

Install the short clip ④ and fix it with the terminal screw. Install the short chip in the direction shown in the figure at right. (The figure at right shown an example when the supply line voltage is 100V AC.)



POINT

If the setting differs from the supply line voltage, the following occurs. Therefore, do not mis-set.

	Supply Line Voltage	
	100V AC	200V AC
Setting to 100V AC (Install the short chip to ②)	—	The power supply module is damaged. (The CPU is not damaged.)
Setting to 200V AC (Install the short chip to ③)	No error occurs in the module. However, the CPU does not operate.	—
No setting (The short chip is not installed)	No error occurs in the module. However, the CPU does not operate.	

7. BASE UNIT

7.1 Base Unit Specifications

This section describes the specifications of the base units (main base unit, extension base unit) that can be used in the A3VTS system.

7.1.1 Specifications of base units

(1) Specifications of main base units

Item \ Type	A30VB
Installable modules	Dual power supply module A61VP 2 modules Majority module A3VTU 1 module Multiplex CPU module A3VCPU 3 modules
Extension connection	Can be connected up to seven levels
Installation hole size	6mm(0.24inch) dia. per-shaped hole (for M5 screw)
External dimensions mm(inch)	480(18.9) × 250(9.84) × 29(1.14)
Weight kg(lb)	2.3(5.06)

Table 7.1 Basic Base Unit Specifications

(2) Specifications of extension base units

Item \ Type	A68VB	A65B	A68B
Loaded I/O modules	8 can be loaded	5 can be loaded	8 can be loaded
Power supply module installation criteria	Dual power supply module A61P 2 modules required (A61VP power supply module can be installed only)	Power supply module required (A61VP power supply module cannot be installed)	Power supply module required (A61VP power supply module cannot be installed)
Installation hole size	6mm(0.24inch) dia. per-shaped hole (for M5 screw)		
External dimensions mm(inch)	522(20.6) × 250(9.84) × 29(1.14)	352(13.9) × 250(9.84) × 29(1.14)	466(18.3) × 250(9.84) × 29(1.14)
Weight kg(lb)	2.4(5.28)	1.4(3.08)	1.9(4.18)

Table 7.2 Extension Base Unit Specifications

7.2 Handling

This section gives base unit handling instructions, notes on using the extension bases, nomenclature and hardware setting instructions.

7.2.1 Handling instructions

(1) Since the base cover, connector and printer PCB are manufactured of plastic, do not subject the base units to impact or shock.

(2) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards. This may cause damage.

(3) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(4) Refer to the specifications first and then use the base unit and the power supply module because there are conditions for combining them. Failure to do so may result in damage to units.

7.2.2 Base unit and power supply module combined use

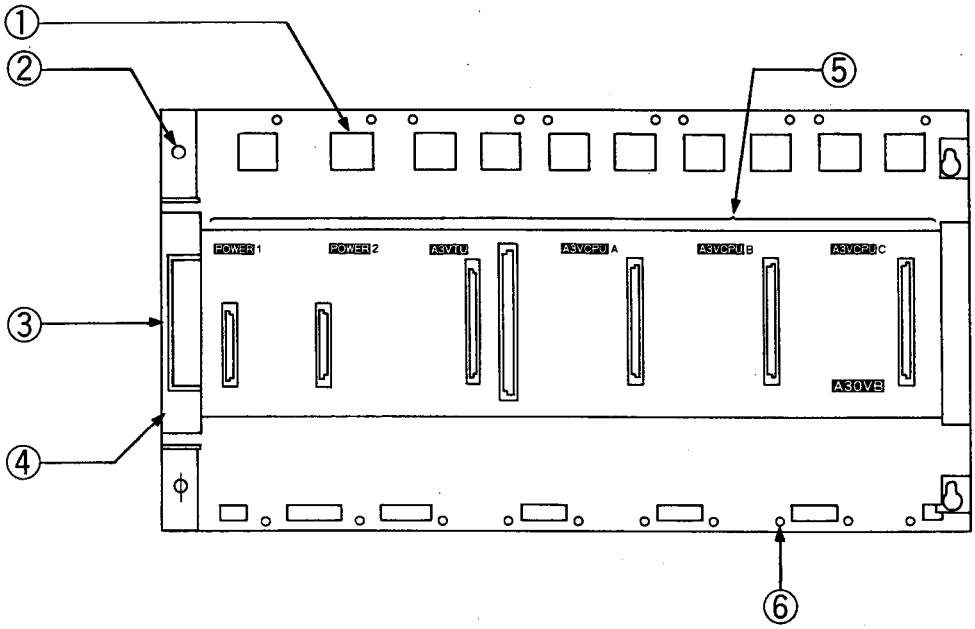
(1) A30VB and A68VB
Use the two A61VP dual power supply modules for each A30VB or A68VB base unit.
If one A61VP module is installed and used, the system may stop when the power supply module malfunctions since dual power supply modules are not duplex.
Power supply modules other than the A61VP cannot be used. The system will not operate normally if these modules are used. This will also damage the power supply module.

(2) A65B and A68B
Use A61P, A62P, A63P or A65P power supply modules for the A65B or A68B base unit.
The A61VP cannot be used in the A65B and A68B. The system will not operate normally if these units are used. This will also damage the power supply module.

7.2.3 Nomenclature

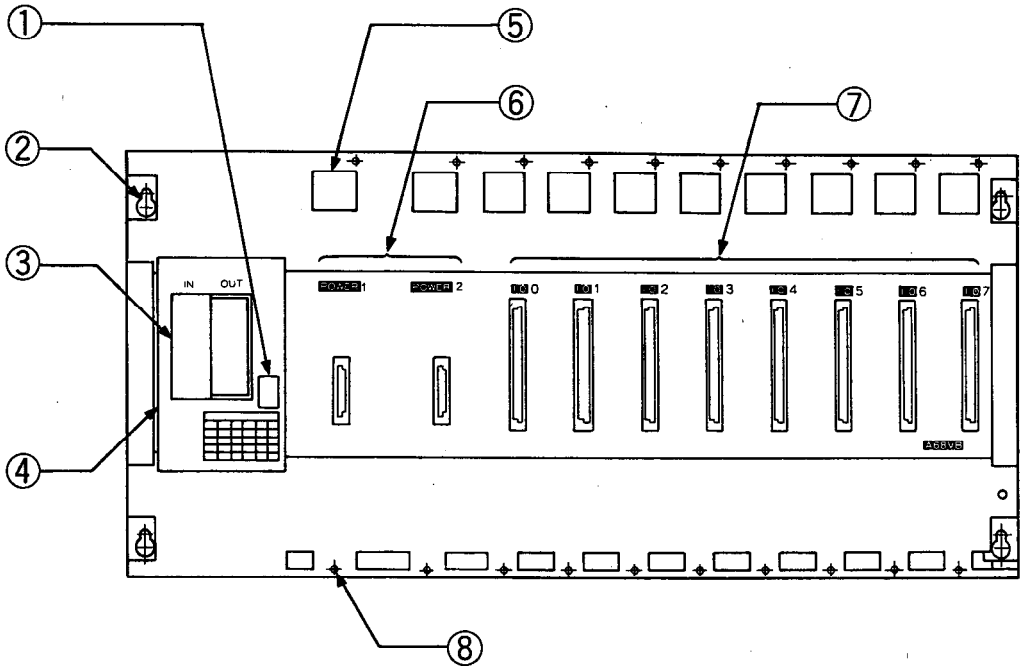
This section describes the names and functions of the main base unit and the extension base unit.

(1) Main base unit (A30VB)



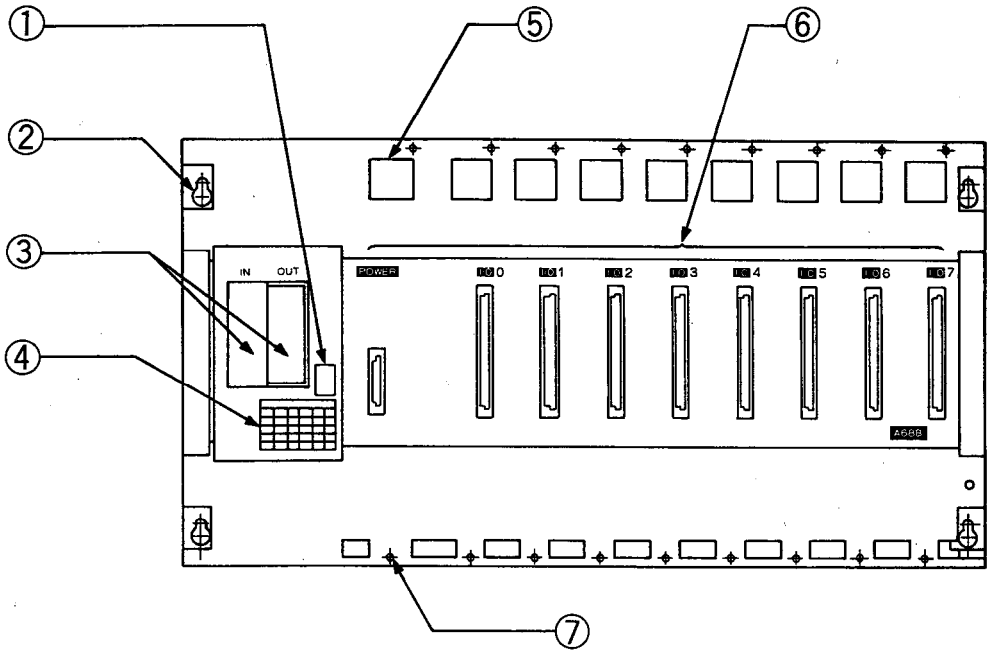
No.	Name and Appearance	Application
①	Module fixing hole	Cut out to accept projection and hook at rear of modules.
②	Guide hole for base installation	Pear-shaped hole for mounting this base unit to the panel of control box, etc. (For M5 screw)
③	Connector for extension cable	Connector for sending and receiving signals to and from the extension base unit. Connect the extension cable (AC□□B).
④	Base cover	Cover for protection of connector for extension cable. When extension is made, it is necessary to remove the top of connector with a tool such as nippers.
⑤	Module connectors	These are the power supply module, majority module and multiplex CPU module connectors. (Install the corresponding module to all connectors. If there is a space where a module is not connected, dust will enter and may cause operation malfunctions.)
⑥	Module fixing screw	The module can be fixed with a screw in addition to the module fixing hook. Screw size: M4 × 0.7 screw.

(2) Extension base unit (A68VB)



No.	Name and Appearance	Application
①	Stage number setting switch	Switch for setting the stage number of extension base. (Located under the base cover) For the stage number setting procedure, refer to Section 7.2.4.
②	Guide hole for base installation	Pear-shaped hole for mounting this base unit to the panel of control box, etc. (For M5 screw)
③	Connector for extension cable	Connector for sending and receiving signals to and from the extension base unit. Connect the extension cable (AC□□B).
④	Base cover	Cover for protection of connector for extension cable. When connection is made with another extension base, it is necessary to remove the area enclosed by a groove at the OUT character portion above the base cover with a tool such as nippers.
⑤	Module fixing hole	Cut out to accept projection and hook at rear of modules.
⑥	Power supply module connector	These connector are used to install power supply modules. Two power supply modules are connected.
⑦	Module connectors	These are the I/O module, power supply (A66) and special function module connectors. Insert a blind cap, AG60 blank cover or AG62 dummy module to vacant connectors to prevent the entry of dust.
⑧	Module fixing screw	The module can be fixed with a screw in addition to the module fixing hook. Screw size: M4 × 0.7 screw.

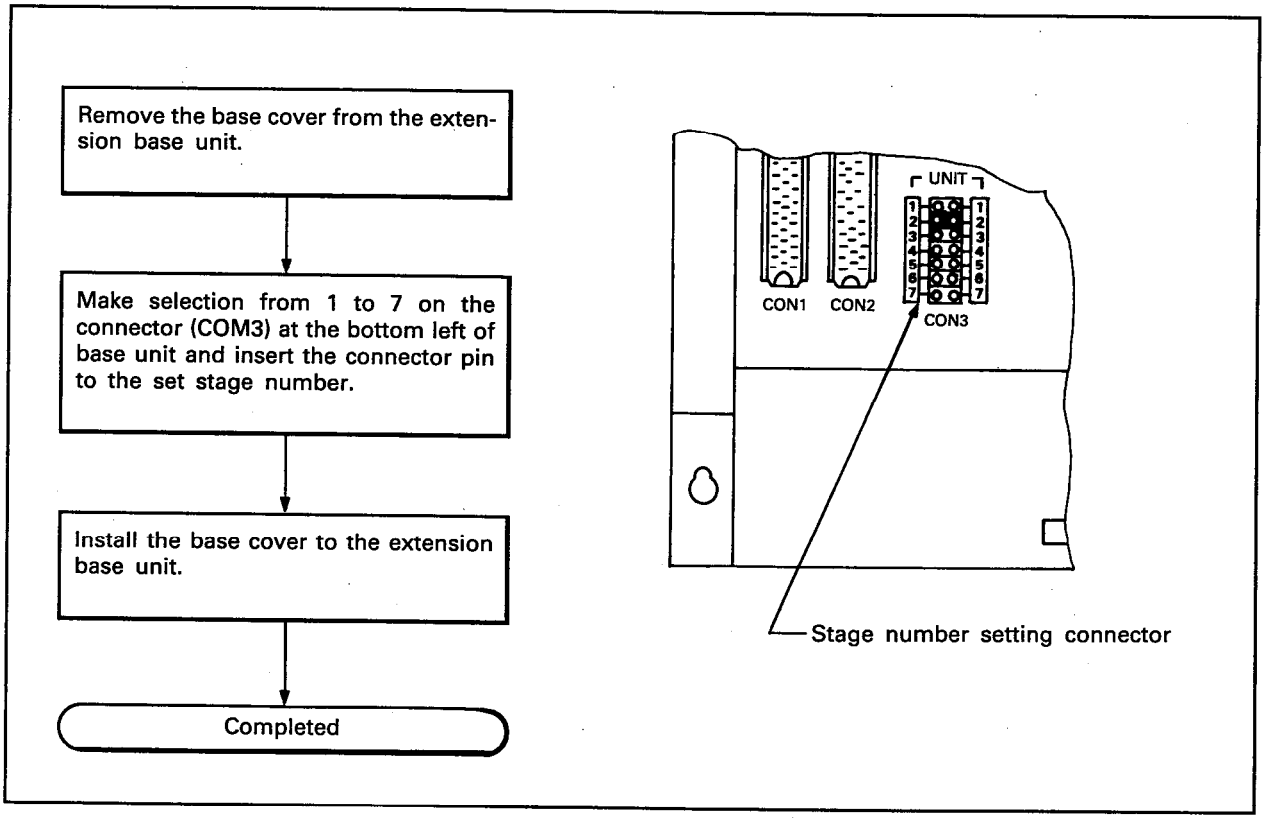
(3) Extension base units (A65B,A68B)



No.	Name and Appearance	Application
①	Stage number setting switch	Switch for setting the stage number of extension base. (Located under the base cover) For the stage number setting procedure, refer to Section 7.2.4.
②	Guide hole for base installation	Pear-shaped hole for mounting this base unit to the panel of control box, etc. (For M5 screw)
③	Connector for extension cable	Connector for sending and receiving signals to and from the extension base unit. Connect the extension cable (AC□□B).
④	Base cover	Cover for protection of connector for extension cable. When connection is made with another extension base, it is necessary to remove the area enclosed by a groove at the OUT character portion above the base cover with a tool such as nippers.
⑤	Module fixing hole	Cut out to accept projection and hook at rear of modules.
⑥	Module connectors	These are the I/O module, power supply (A66) and special function module connectors. Insert a blind cap, AG60 blank cover or AG62 dummy module to vacant connectors to prevent the entry of dust.
⑦	Module fixing screw	The module can be fixed with a screw in addition to the module fixing hook. Screw size: M4 × 0.7 screw.

7.2.4 Setting of extension stage numbers

This section explains the stage number setting procedure of each extension base unit. (when the extension base unit is used.)



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	Extension Stage Number Setting						
	1st stage	2nd stage	3rd stage	4th stage	5th stage	6th stage	7th stage
Extension stage number setting	UNIT CON3	UNIT CON3	UNIT CON3	UNIT CON3	UNIT CON3	UNIT CON3	UNIT CON3

Extension Base Unit Stage Number Setting

POINT

Set the stage number setting connector (CON3) to a number, from 1 to 7, which matches the number of extension stages. If the same number has been set to two or more extension base units, or no stage number has been set, mis-input or mis-output will result.

8. EXTENSION CABLE

8.1 Specifications

This section describes the specifications of extension cables which can be used for the system.

Item / Type	AC06B	AC12B	AC30B
Cable length m(ft)	0.6(1.97)	1.2(3.94)	3(9.84)
Resistance value of 5V DC supply line (Ω at 55°C)	0.019	0.028	0.052
Application	For connection between main base and extension base and between extension bases		
Weight kg(lb)	0.34(0.75)	0.52(1.14)	1.06(2.33)

Table 8.1 Extension Cable Specifications

9. MEMORY CASSETTE, MEMORY

9.1 Specifications

This chapter describes the specifications of memories and memory cassettes which can be used.

9.1.1 Memory cassette specifications

This section describes the specifications of memory cassettes used.

Item \ Type	A3NMCA-0	A3NMCA-2	A3NMCA-4	A3NMCA-8	A3NMCA-16	A3NMCA-24
*Memory capacity (bytes) (RAM memory capacity)	None installed	16K	32K	64K	128K (96K)	192K (144K)
Number of ROM loading sockets	2 pcs. (for 28 pins)					
Loadable ROM type	4KROM, 8KROM, 16KROM					
Loadable RAM type	4KRAM	Unloadable				
External dimensions mm(inch)	110(4.33) × 79.5(3.13) × 33(1.30)					
Weight kg(lb)	0.13(0.29)	0.13(0.29)	0.13(0.29)	0.13(0.29)	0.13(0.29)	0.13(0.29)

*: The RAM memory is soldered to the PCB.

Table 9.1 Memory Cassette Specifications

9.1.2 Memory specifications

Item \ Type	4KRAM	4KROM	8KROM	16KROM
Memory specifications	IC-RAM (Read and write possible)	EP-ROM (only read is possible)		
Memory capacity (bytes)	8K	8K	16K	32K
Structure	28-pin IC package	28-pin IC package	28-pin IC package	28-pin IC package
Remarks	When loading memory into the memory cassette two memory ICs of the same specification are always required.			

When the parameter setting is performed by a peripheral device, refer to the Section 9.2.5 for further details regarding the data and capacity which can be stored in memory cassette.

Table 9.2 Memory Specifications

9.1.3 Battery specifications

This section describes the specifications of battery used for RAM memory backup and power failure compensation.

Item \ Type	A6BAT
Nominal voltage	3.6V DC
Guaranteed life	5 years
Total power failure backup time	Depends on memory cassette types as indicated below: A3NMCA-0: Min. 10800 hours, A3NMCA-24: MIN. 1950 hours
Application	For IC-RAM memory backup and power failure compensation function
External dimensions mm(inch)	ϕ16(0.63) × 30(1.18)

Table 9.3 Battery Specifications

9.2 Handling

This chapter explains the handling instructions from unpacking to installation and also the nomenclature and setting of various conditions.

9.2.1 Handling instructions

The handling precautions for the memory cassette and battery from removing them from the shipping container to installation are described in this section.

(1) Memory cassette, memories

(a) Since the memory cassette and pin connector are manufactured from plastic, do not subject the memory cassette and memories to impact or shock.

(b) Do not remove printed circuit boards from the housing. There are no user-serviceable parts on the boards. This may cause damage.

(c) Ensure that no conductive debris can enter the module. If it does, make sure that it is removed. Guard particularly against wire offcuts.

(d) When loading the memory cassette into th main unit, press the memory cassette securely into the housing.

(e) When loading the memory into the socket, press the memory securely against the socket and the lock it with the lever.
After loading, check that the memory is flush with the socket.

(f) Never place the memory on metal, which may allow current flow, or on an object which is charged with static electricity, such as wood, plastic, vinyl, fiber, cable, and paper.

(g) Do not touch the legs of the memory. Also, do not bend the legs. The memory may be damaged.

(h) When mounting the memory, be sure to fit the memory the right way round as indicated on the socket. If reversely installed, the memory will be damaged.

(i) Do not touch the CPU memory cassette connector. Touching the connector may result in improper contact.

IMPORTANT

Before installing or removing the memory cassette to or from the CPU, GPP, be sure to turn off the power. If installation or removal is performed with the power on, the contents of the memory cassette will be damaged.

(2) Battery

(a) Do not short-circuit the battery.

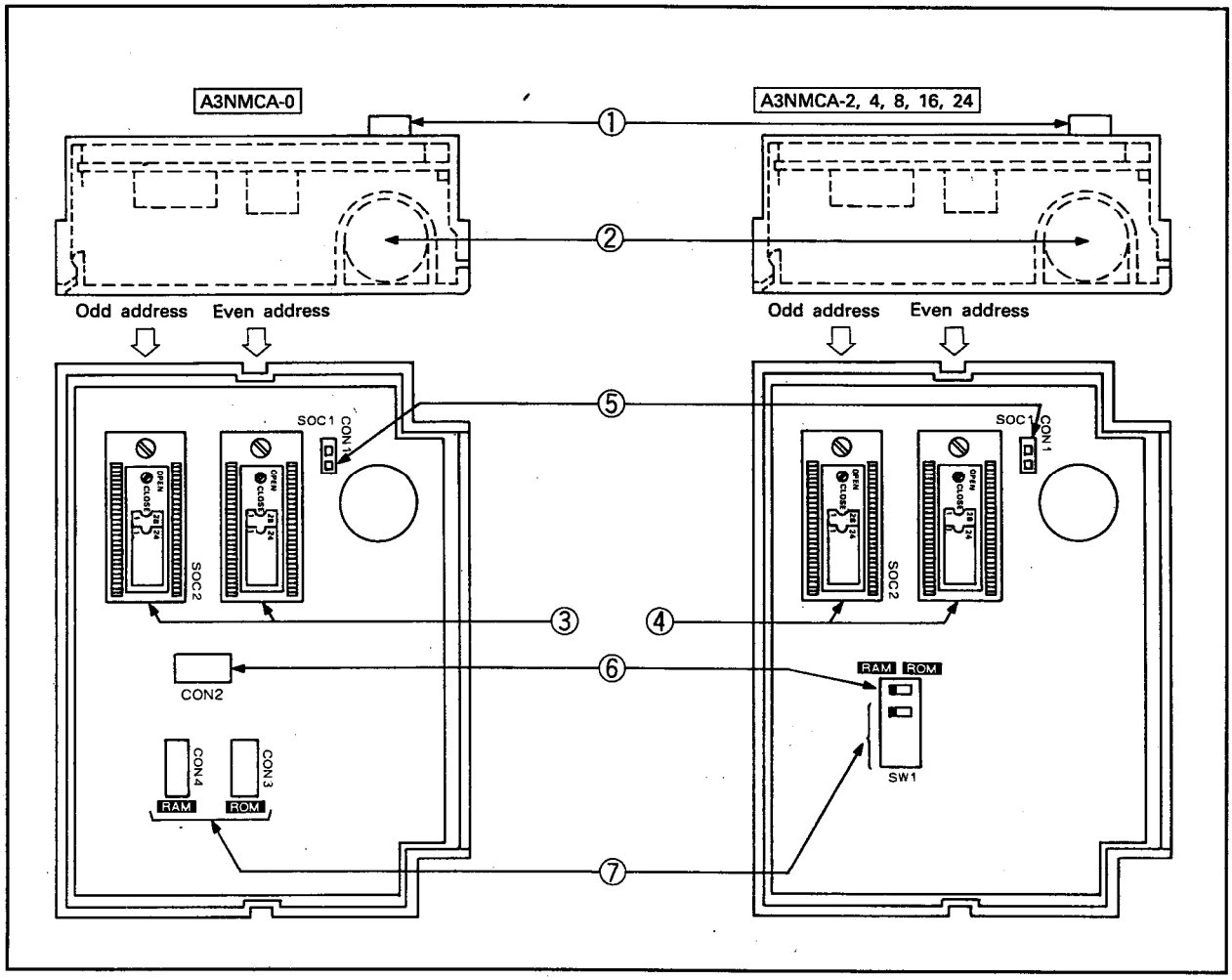
(b) Do not disassemble the battery.

(c) Do not throw the battery into flames.

(d) Do not heat the battery.

(e) Do not solder the poles of the battery.

9.2.2 Nomenclature



No.	Description	Explanation	Remarks
①	CPU connector	Connects the memory cassette to the CPU.	
②	Battery (A6BAT)	RAM backup and power failure compensation.	
③	Program memory sockets	I.C. sockets with locking facility for IC-RAM/EP-ROM. Identical memory I.C. types must be loaded into the two sockets. When ROMs are used, the odd-address ROM must be loaded into SOC1. and the even-address ROM into SOC2.	*
④		I.C. sockets with locking facility for EP-ROM only Identical memory I.C. types must be loaded into the two sockets. The odd-address ROM must be loaded into SOC1. and the even-address ROM into SOC2.	*
⑤	Pins for connection of battery plug	Connect the battery leads to the connector (CON1). Before shipment, the wires are disconnected to prevent battery consumption.	*
⑥	Memory setting switch	Memory select switch.	*
⑦	Memory protect switches	Set the protect range of the IC-RAM contents. (With protect ON, writing to the RAM is disabled.)	*

*: Requires setting before using the memory cassette.

9.2.3 Memory IC installation

(1) Holding the memory chips

If the memory chip pins or leads are touched by hand, they can be damaged by static electricity or the pins may be bent and cause improper connection. Hold the module as shown in the figure and install it correctly.

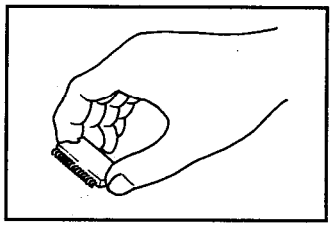


Fig. 9.1 Holding the IC

(2) Chip installation direction

If the memory chip direction is incorrect, the memory chip will be damaged when the power is turned on. Make sure that the memory chip direction is correct before installing it.
The installation direction is indicated on the memory socket. Install the memory chip using the following as the reference.
EP-ROM ···· Notch
IC-RAM ····· Notch or broken line

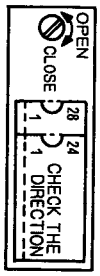
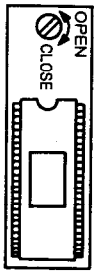
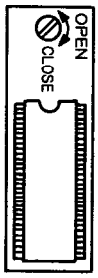
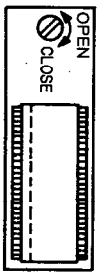
Socket	EP-ROM	IC-RAM	
		Notch	Broken line
			

Fig. 9.2 IC Loading Direction

(3) Setting the IC type

Set the jumper or switch to RAM or ROM in accordance with the IC used.

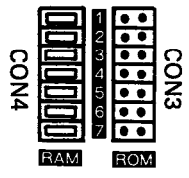
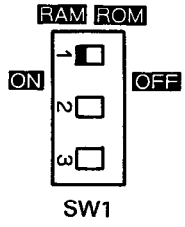
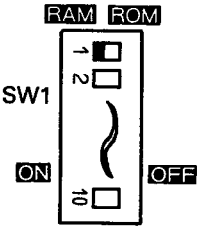
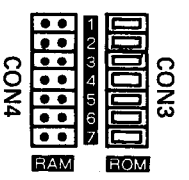
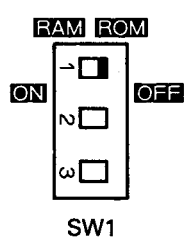
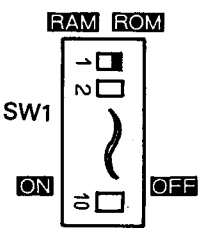
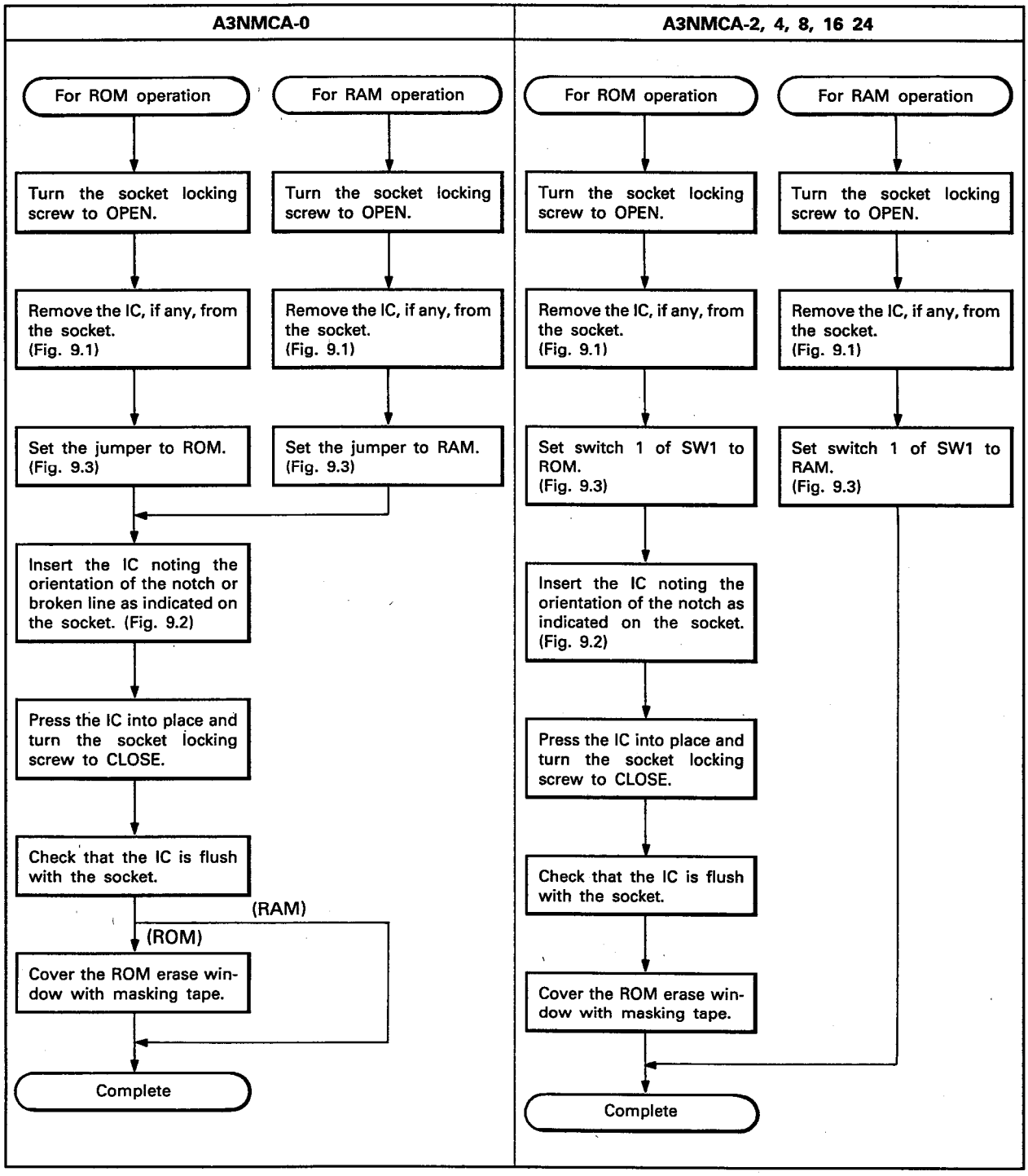
		A3NMCA-0	A3NMCA-2, 4	A3NMCA-8, 16, 24	
IC type setting	RAM				1) Load the IC after setting its type. 2) When the A3NMCA-0 is used, set the jumper to CON3 (ROM) or CON4 (RAM). CON3·····ROM setting CON4·····RAM setting 3) When the A3NMCA-2 to 24 is used, set switch 1 of SW1 to the appropriate position.
	ROM				

Fig. 9.3 Setting the IC Type

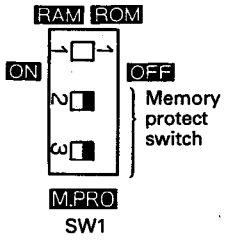
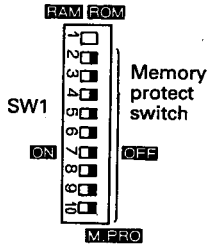
(4) IC loading procedure

Install the memory chip using the following procedure.



9.2.4 Memory protect switch setting

The RAM memory may be protected by switching the memory protect switch ON . (See below) This protects the memory from accidental program changes.
When changes to the PC program are to be made, switch the memory protect switch OFF .
The switch layout varies depending on the memory cassette type as shown below.

A3NMCA-0	A3NMCA-2, 4	A3NMCA-8, 16, 24
		

The memory ranges protected by each switch are shown below:

Memory Protect Range	Setting	Applicable Memory Cassette
(Byte number) 0 ∫ 16K	Jumper set to ON of CON2 2 of SW1 ON	A3NMCA-0 and -2, A3NMCA-4, A3NMCA-8, A3NMCA-16, A3NMCA-24
16K ∫ 32K	3 of SW1 ON	A3NMCA-4, A3NMCA-8, A3NMCA-16, A3NMCA-24
32K ∫ 48K	4 of SW1 ON	A3NMCA-8, A3NMCA-16, A3NMCA-24
48K ∫ 64K	5 of SW1 ON	A3NMCA-8, A3NMCA-16, A3NMCA-24
64K ∫ 80K	6 of SW1 ON	A3NMCA-16, A3NMCA-24
80K ∫ 96K	7 of SW1 ON	A3NMCA-16, A3NMCA-24
96K ∫ 112K	8 of SW1 ON	A3NMCA-16, A3NMCA-24
112K ∫ 128K	9 of SW1 ON	A3NMCA-16, A3NMCA-24
128K ∫ 144K		A3NMCA-24
144K ∫ 192K	10 of SW1 ON	A3NMCA-24

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POINT

(1) Activating memory protection
Refer to the addresses (step numbers) of each memory area (sequence program, computer program, sub-sequence program, comments, sampling trace, status latch and file registers) to perform the protection settings.

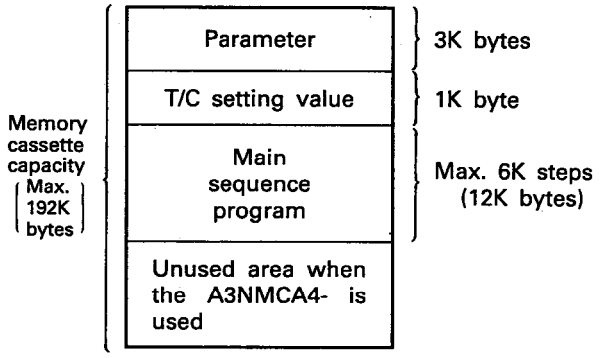
(2) Do not memory protect areas required for sampling trace or status latch data when using these functions. If the protection is activated the executed contents cannot be stored in the memory.

9.2.5 User memory installation

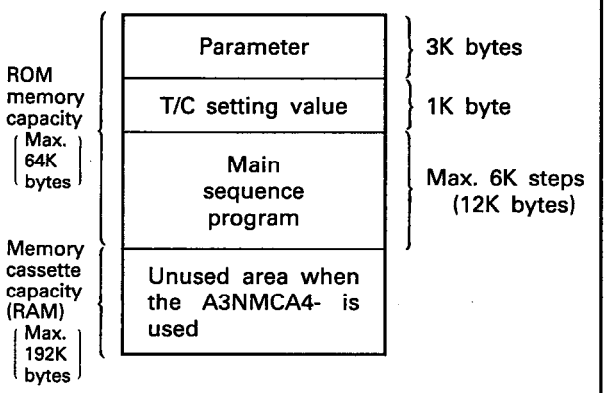
The usage capacity and availability of user memory in the memory cassette can be set by the peripheral device parameter settings. This section describes the user memory assignments and memory capacity in the two cases - parameters are set or not set with a peripheral device.

(1) When peripheral device parameters are not set
User memory assignments and memory capacity when the memory is used without parameter settings is described below.

RAM operation



ROM operation



REMARKS

(1) The 4K bytes parameter and T/C setting value area is automatically set in the user memory area.
(2) The main sequence program refers to the main routine program and the subroutine program.
(3) There is an unused portion of memory when the sequence program capacity is smaller than the user memory (memory cassette) capacity as shown in the figure above.

(2) When peripheral device parameters are set

This section describes the user memory assignment and memory capacity when parameters (capacity settings for the sequence program, comments, etc.) are set with a peripheral device. Select the memory cassette whose storage capacity is sufficient for memory area required according to the setting of parameters.

RAM operation

Memory cassette RAM area

Parameters	4K bytes used regardless of the parameter setting
T/C setting value	
Main sequence program	Settings made in 1K steps (2K bytes) within a range of 1 to 30K steps (2 to 60K bytes).
Microcomputer program	
T/C setting value	When the sub-sequence program is used, 1K byte is used regardless of parameter settings.
Sub-sequence program	Settings made in 1K steps (2K bytes) within a range of 1 to 30K steps (2 to 60K bytes).
Sub-microcomputer program	
Device P.I. address, other contents	When the sub-sequence program is used, 5K bytes is used regardless of parameter settings.
Sampling trace	Selectable: Not used (0K bytes), Used (8K bytes)
Status latch: Data area	Selectable: Not used (0K bytes), Used (8K bytes)
Status latch: File register	Selectable: Not used (0K bytes), Used (amount set by the file register) Setting made in 2K bytes units (1024 points) within a range of 0 to 16K bytes (0 to 8192 points). Setting made in 1K byte units (64 points) within a range of 0 to 16K bytes (0 to 8192 points).
File register	
Comment	

ROM operation

Memory cassette ROM area

Parameters	4K bytes used regardless of the parameter setting
T/C setting value	
Main sequence program	Settings made in 1K steps (2K bytes) within a range of 1 to 30K steps (2 to 60K bytes).
Microcomputer program	

Memory cassette RAM area

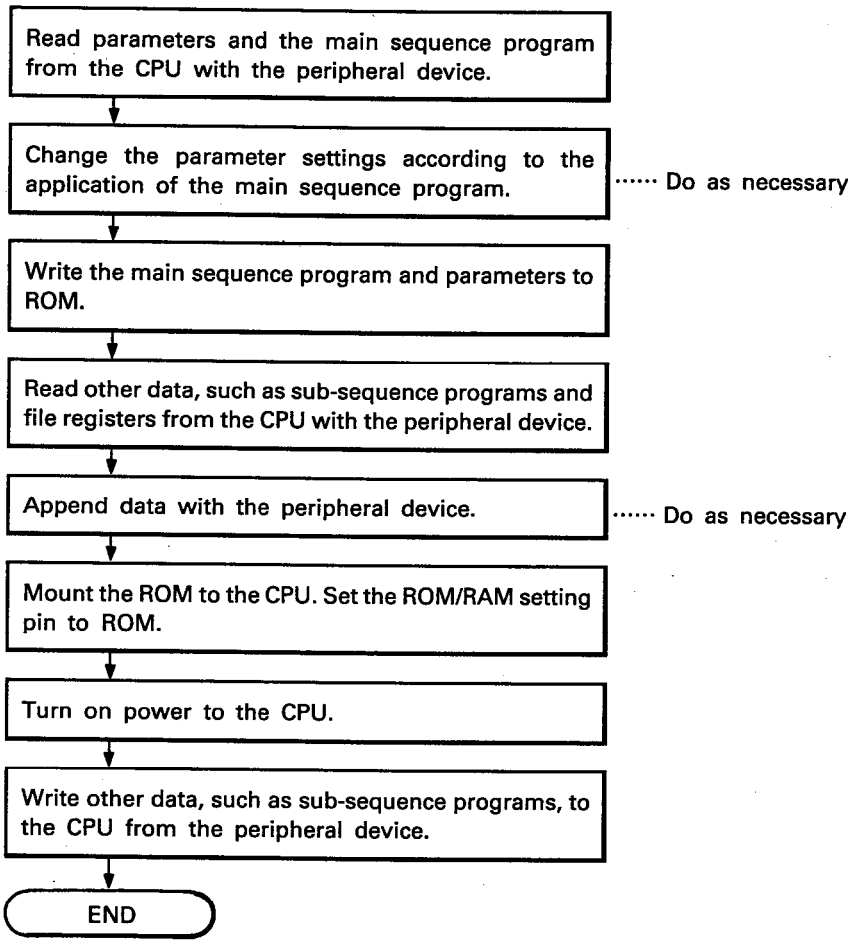
T/C setting value	When the sub-sequence program is used, 1K byte is used regardless of parameter settings.
Sub-sequence program	Settings made in 1K steps (2K bytes) within a range of 1 to 30K steps (2 to 60K bytes).
Sub-microcomputer program	
Device P.I. address, other contents	When the sub-sequence program is used, 5K bytes is used regardless of parameter settings.
Sampling trace	Selectable: Not used (0K bytes), Used (8K bytes)
Status latch: Data area	Selectable: Not used (0K bytes), Used (8K bytes)
Status latch: File register	Selectable: Not used (0K bytes), Used (amount set by the file register) Setting made in 2K bytes units (1024 points) within a range of 0 to 16K bytes (0 to 8192 points). Setting made in 1K byte units (64 points) within a range of 0 to 16K bytes (0 to 8192 points).
File register	
Comment	

(3) Precautions concerning ROM operations

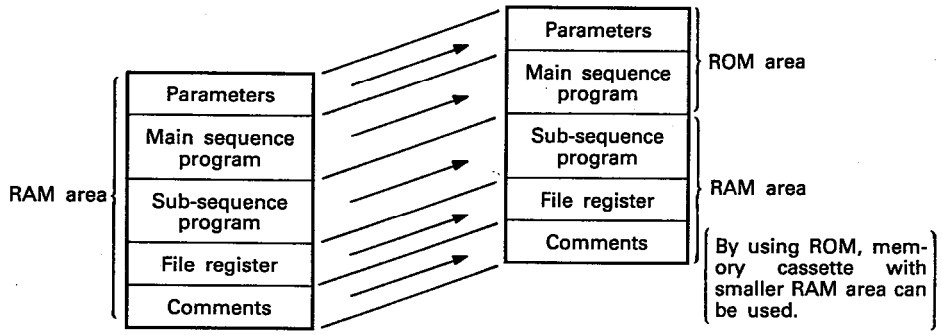
When operating using a main sequence program that has been written to ROM, sub-sequence programs cannot be used without special procedures being taken.

Follow the procedures given below to write updated information to the memory cassettes.

Memory area can be used more effectively by also writing other data such as file registers and comments to the cassettes using the procedure given below.

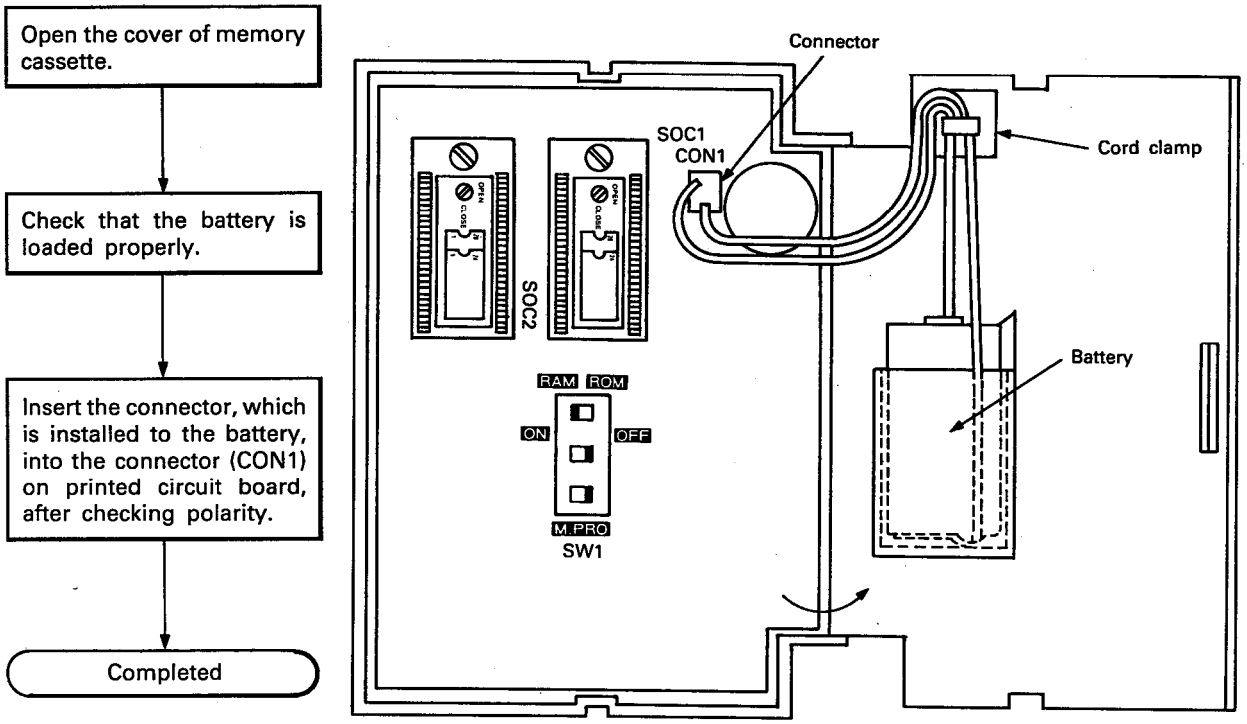


[Example of data transfer using a ROM]



9.2.6 Battery installation

The connector of battery is disconnected before shipment. When RAM memory backup or power failure compensation is required, connect by the following procedure.



REMARKS

The connector of the battery has been disconnected in order to prevent the consumption of battery during distribution and storage, connect the connector before use.

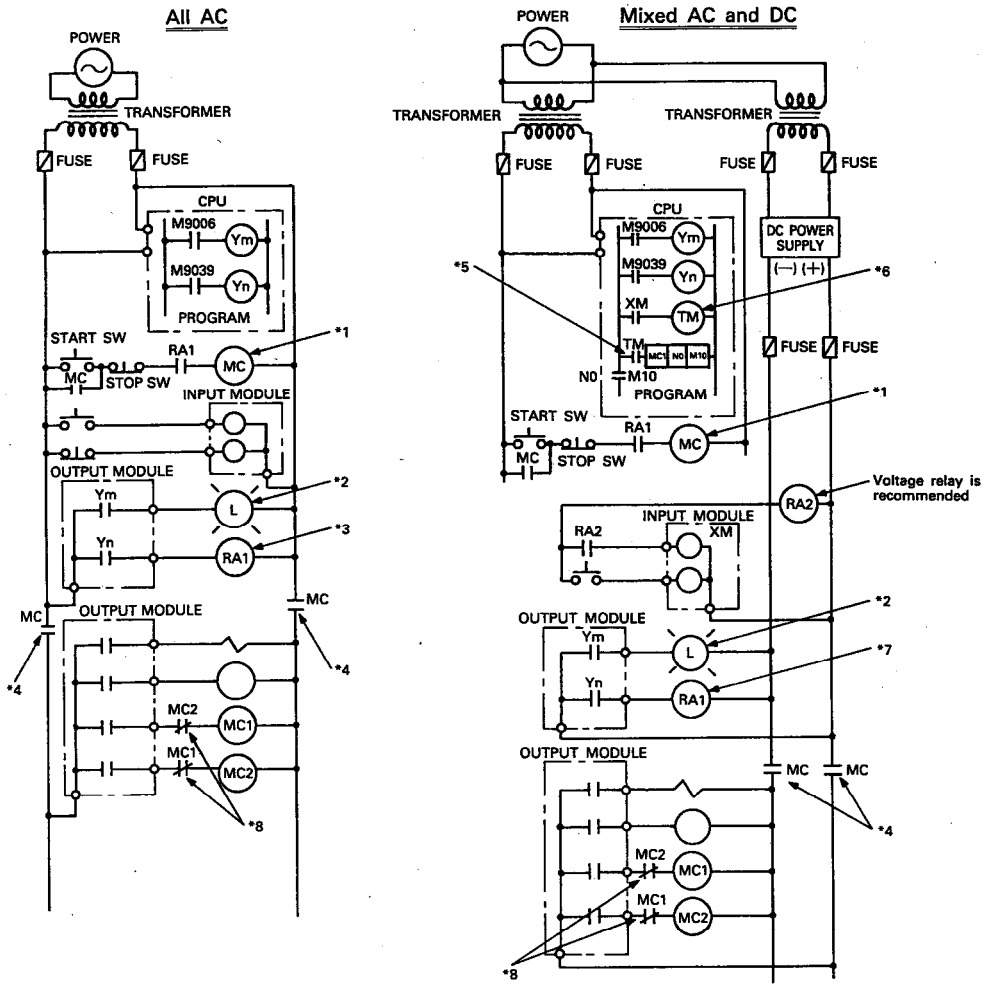
10. LOADING AND INSTALLATION

This chapter describes the loading and installation procedures and instructions for mascumuim reliability of the system.

10.1 Consideration for Safety

When the power of system is turned on or off, process output may not temporarily perform normal operation due to the difference between the delay time and rise time of the power supply of programmable controller main unit and the external power supply (especially DC) for the process. Also, at the time of an error of the external power supply, output process may possibly make an erroneous operation.
In order to prevent the aforementioned erroneous operations from resulting in an erroneous operation of the entire system and also for safety reasons, constitute circuits (such as emergency stop circuit, protection circuit, and interlock circuit), that prevent machine damage or and accident due to erroneous operation outside the programmable controller.
A system design circuit example based on the above concept is shown on the following page.

System design circuit example



*1: Run/stop circuit interlocked with RA1 (run monitor relay)
*2: Battery low alarm
*3: RA1 switched on by M9039 (run monitor relay)
*4: Power to output equipment switched off when stop signal given.
For emergencies
Stopped when limits exceeded.
*5: Input switched when power supply established.
*6: Set time for DC power supply to be established.
*7: On when run by M9039
*8: Interlock circuits
For opposing operations such as forward and reverse rotation, and for operations which will cause damages to the machine or accidents, provide the interlock circuit externally.

The power-on procedure is as follows:

For AC

1) Switch on power.
2) Set CPU to RUN.
3) Switch on the start switch.
4) When the magnetic contactor (MC) comes in, output equipment is powered and may be driven from the program.

For AC/DC

1) Switch on power.
2) Set CPU to RUN.
3) When DC power is established, RA2 turns on.
4) Timer (TM) times out after the DC power reaches 100%.
(The set value of TM should be the period of time from when RA2 switches on to the establishment of 100% DC voltage. Set the set value to approximately 0.5 seconds.)
5) Switch on the start switch.
6) When the magnetic contactor (MC) comes in, the output equipment is powered and may be driven by the program.
When using a voltage relay in RA2, timer (TM) is not needed in a program.

10.2 Installation Environment

Never install the ANCPU system in the following environments:

(1) Locations where ambient temperature is outside the range 0 to 55°C.

(2) Locations where ambient humidity is outside the range of 10 and 90%RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive gasses and combustible gasses.

(5) Locations where there is a high level of conductive powder such as dust and iron filings, oil mist, salt, and organic solvent.

(6) Locations exposed to the direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

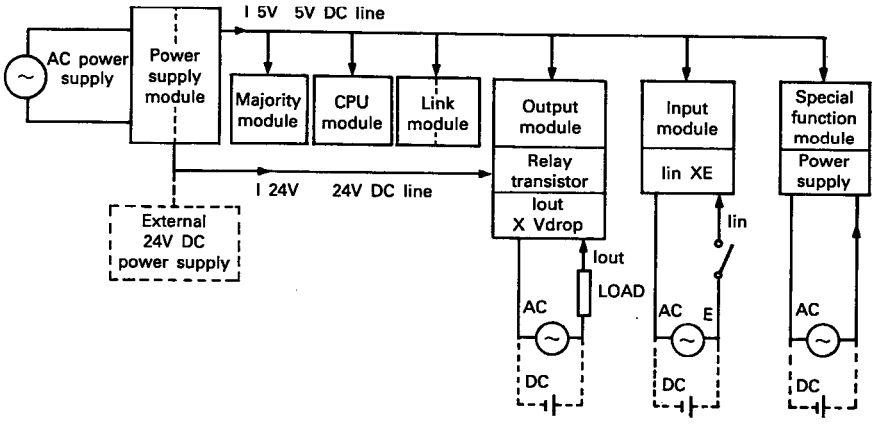
(8) Locations where vibration and shock are directly transmitted to the main unit.

10.3 PC Generated Heat Calculation

The operating ambient temperature of the PC must be kept below 55°C. It is necessary that the average power consumption of modules and other equipment inside panel be known for heat radiation design of the panel. The following describes how to determine the average power consumed by the A3VTS system. Use the power consumption value is used to calculate the temperature rise inside the panel.

Average power consumption

Power is consumed by the following PC areas:



(1) Power supply module power consumption

Approximately 70% of the power supply module current is converted into power with the remaining 30% dissipated as heart, i.e., 3/7 of the output power is used.
Case of using A6□P power supply module, 1.1(W) modify 1.0(W).

$$Wpw = \frac{3}{7}((I\ 5V \times 5) + (I\ 24V \times 24)) \times 1.1\ (W)$$

where, I 5V = 5V DC logic circuit current consumption of each module.
I 24V = current consumption of the output modules (with an average number of points switched on) ··· (Not for 24V input power supply modules)

(2) Total 5V DC power consumption

5V is supplied to each module via the base plate, this powers the logic circuitry.

$$W\ 5V = I\ 5V \times 5\ (W)$$

(3) Total 24V DC output module power consumption (with an average number of points switched on)
24V is supplied to drive output devices.
W24V = I 24V × 24 (W)

(4) Power consumption of output circuits (with an average number of points switched on)
Wout = Iout × Vdrop × average number of outputs on at one time (W)
where, Iout = output current (actual operating current) (A)
Vdrop = voltage dropped across each output load (V)

(5) Power consumption of input circuits (with an average number of points switched on)
Win = Iin × E × average number of inputs on at one time (W)
Where, Iin = input current (effective value for AC) (A)
E = input voltage (actual operating voltage) (V)

(6) Power consumption of the special function module power supply is expressed as:
Ws = I 5V × 5 + I 24V × 24 + I 100V × 100 (W)

The sum of the above values is the power consumption of the entire PC system.
W = Wpw + W5V + W24V + Wout + Win + Ws (W)

Further calculations are necessary to work out the power dissipated by the other equipment in the panel.

Generally temperature rise in the panel is expressed as:

$$T = \frac{W}{UA} (°C)$$

where, W = power consumption of the entire PC system (obtained as above)
A = panel inside surface area (m^2)
U = 6 if the panel temperature is controlled by a fan, etc.
4 if panel air is not circulated.
T = Temperature rise inside the panel (°C)

10

POINT

If temperature rise inside the panel exceeds the set limit, heat exchangers should be attached to the panel to lower the temperature inside the panel.
Precaution should be used when using a fan to cool the panel as dust and dirt from outside the panel will be sent passed into the interior. This could have negative effects on the programmable controllers.

10.4 Mounting of Base Unit

This section describes precautions concerning the handling of the main base unit and the extension base units.

10.4.1 Mounting instructions

Explanation is given to the instructions for mounting the PC to a panel, etc.

(1) To improve ventilation or facilitate the replacement of unit, provide 80mm(3.15inch) or more the clearance around the PC.

(2) Do not mount the base unit vertically or horizontally to allow ventilation.

(3) Ensure that the base unit mounting surface is uniform to prevent strain. It excessive force is applied to the printed circuit boards, this will result in incorrect operation. Therefore, mount the base unit on a flat surface.

(4) Avoid mounting the base unit close to vibration source, such as large-sized magnetic contactors and no-fuse breakers, install the base unit in another panel or separate the base unit from the vibration source.

(5) Provide a wiring duct as necessary.
However, if the dimensions from the top and bottom of the PC are less than those shown in Fig. 10.1, note the following points:

(a) When the duct is located above the PC, the height of the duct should be 50mm(1.97inch) or less to allow for sufficient ventilation.
Set the distance form the top of the PC so that the hook latch at the top of the module can be pushed. If the hook latch at the top of the module cannot be pushed, the module cannot be replaced.

(b) When the duct is located under the PC, install the duct so that optical fiber cables or coaxial cables may be connected and also consider the minimum bending radius of the cable.

(6) In order to avoid the negative effects of noise and heat, do not place equipment in front of the programmable controller at distances less than 100mm (3.94inch) if the equipment should be mounted on the back side of the door. Allow at least 50mm (1.97inch) clearance on both sides of the base unit.

10.4.2 Installation

This section explains the mounting for basic and extension base units.

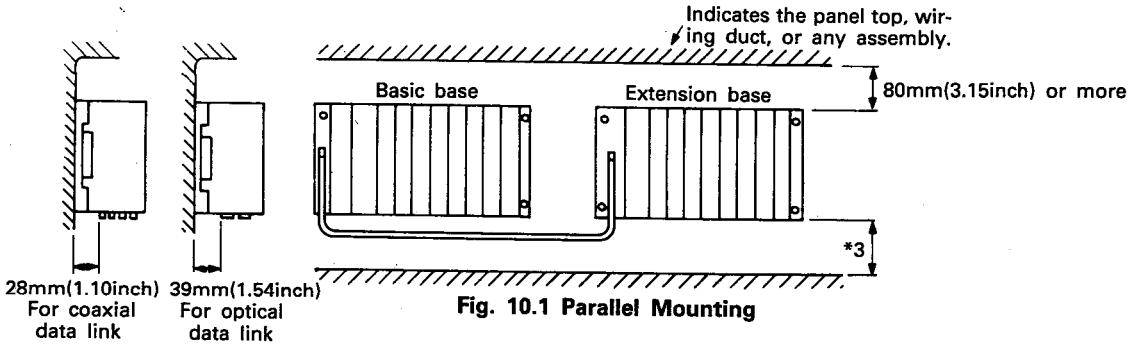


Fig. 10.1 Parallel Mounting

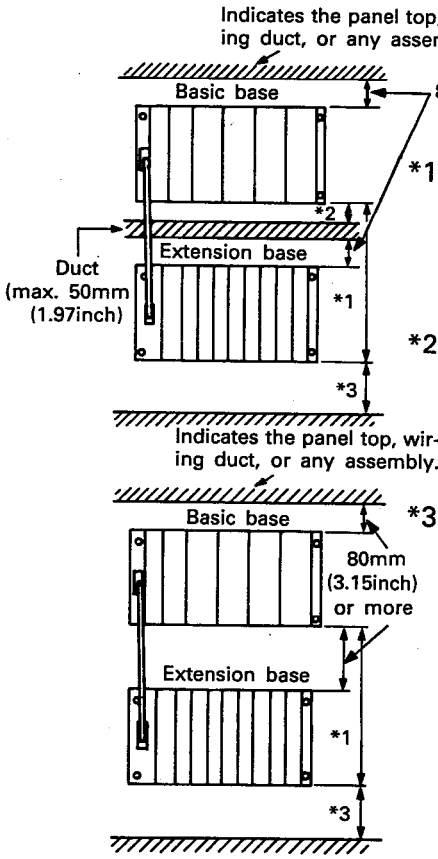


Fig. 10.2 Serial Mounting

*1: Depends on the length of the extension cable as indicated below.
450mm(17.72inch) or less for Type AC06B cable
1050mm(41.34inch) or less for Type AC12B cable
2850mm(112.21inch) or less for Type AC30B cable

*2: 50mm(1.97inch) or more when the link unit is not used.
90mm(3.54inch) or more when 4.5mm(0.18inch) optical fiber cable is used.
110mm(4.33inch) or more when 8.5mm(0.33inch) dia. optical fiber cable or coaxial cable is used.

*3: 50mm(1.97inch) or more when the link unit is not used.
90mm(3.54inch) or more when 4.5mm(0.18inch) optical fiber cable is used.
130mm(5.19inch) or more when 8.5mm(0.33inch) dia. optical fiber cable or coaxial cable is used.

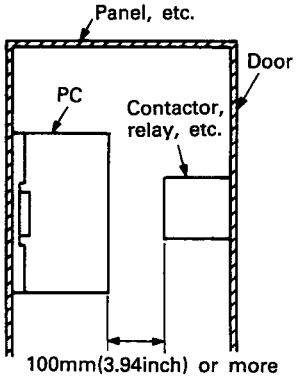


Fig. 10.3 Minimum Front Clearance with Panel Door Shut

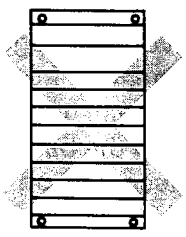


Fig. 10.4 Vertical Mounting (Not allowed)

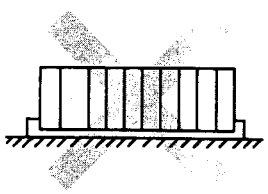


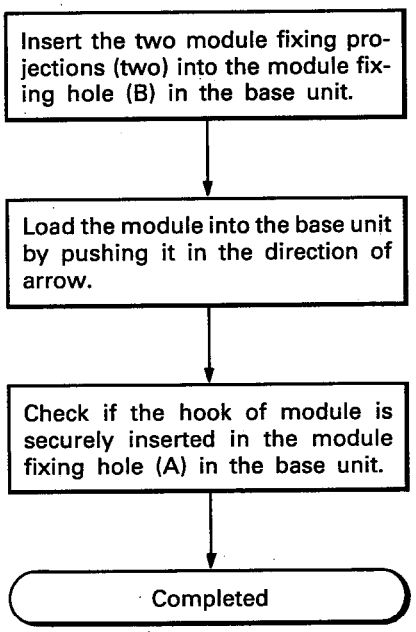
Fig. 10.5 Horizontal Mounting (Not allowed)

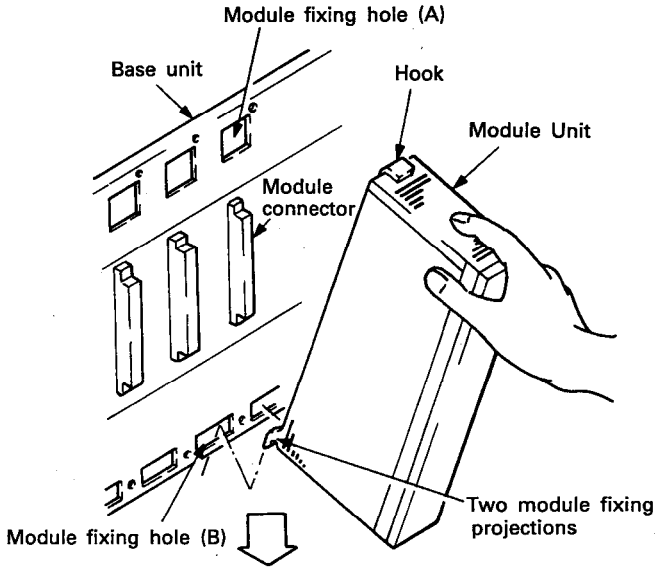
10.5 Installation and Removal of Module

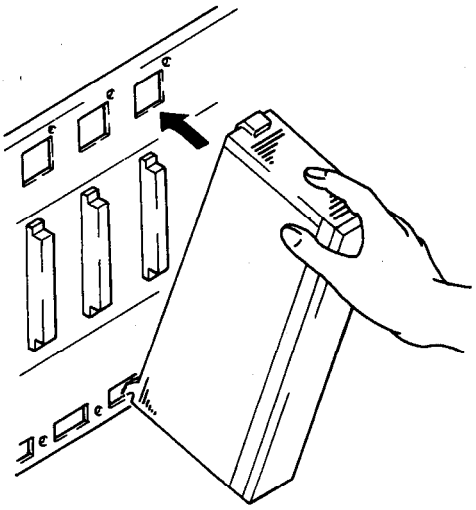
This section explains the installation and removal procedures of the power supply module, CPU module, I/O module, special function module, etc to and from the base module.

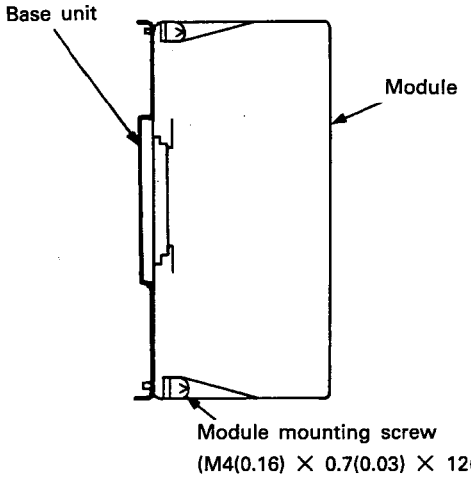
(1) Installation of module

The unit installation procedure is explained.









POINT

(1) To fix the module, be sure to insert the module fixing projection into the module fixing hole (B). If the module is forcibly fixed without insertion, the pins in the module connector may be bent or damaged.

(2) When the base unit is used at locations where there are especially large vibration and/or shock, screw the module to the base. Applicable screw size is M4(0.16) × 0.7(0.03) × 12mm (0.47inch). See the figure at right.

(2) Removal of module

The unit removal procedure is explained.

Hold the module with both hands and push the hook latch at the top of module.

↓

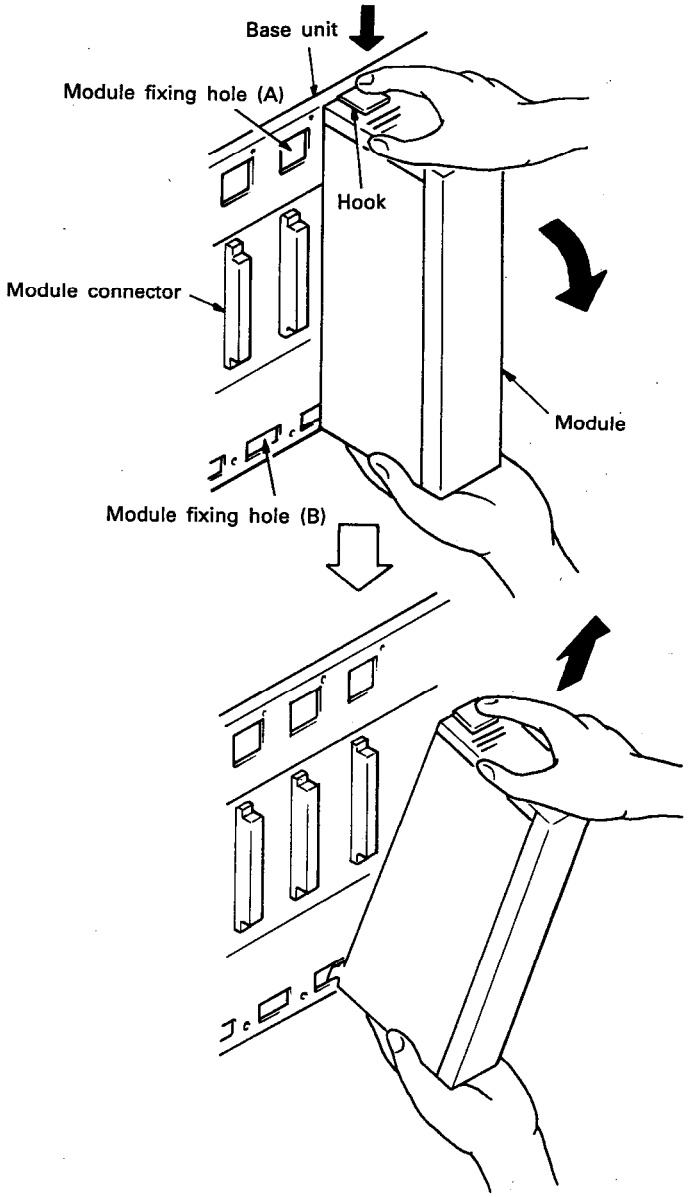
While pushing the hook latch, pull the module toward you.

↓

Lift upwards and remove the module fixing projections from the module fixing hole (B).

↓

Completed



POINT

To remove the module, be sure to disengage the hook from the module fixing hole (A) and then remove the module fixing projections from the module fixing hole (B). If the module is forcibly removed, the hook or module fixing projections will be damaged.

10.6 Wiring

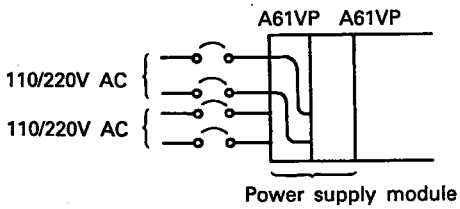
Wiring instructions for the A3VTS system.

10.6.1 Wiring instructions

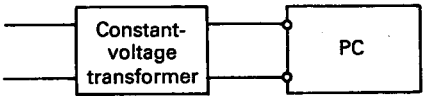
Instructions for wiring the power cable or I/O cables.

(1) Wiring of power source

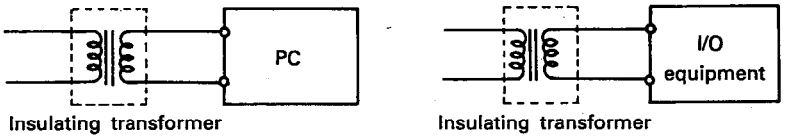
(a) To enhance reliability, two power supply modules are used in the A3VTS system providing backup functions in case a malfunction should occur in one of the power supply modules or a failure should occur in one of the power feed lines. It is therefore important that the power source for the two power supply modules be separate.



(b) When voltage fluctuations are larger than the specified value, connect a constant-voltage transformer.



(c) Use a power supply which generates minimal noise across wire and across PC and ground. When excessive noise is generated, connect an insulating transformer.

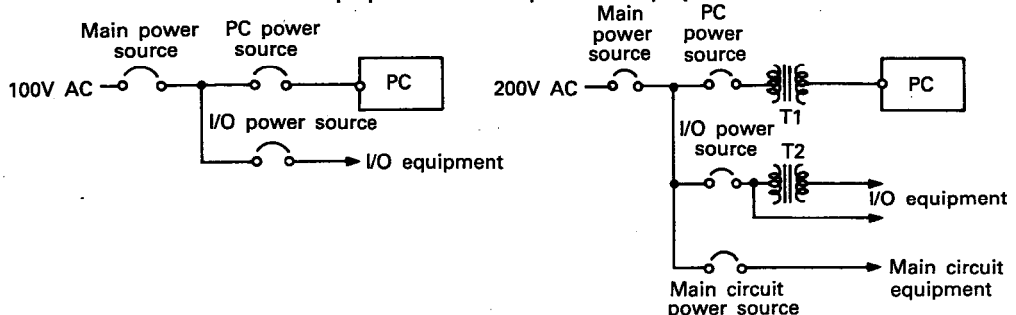


(d) When a power transformer or insulating transformer is employed to reduce the voltage from 200V AC to 100V AC, use one with a capacity greater than that indicated in the following table.

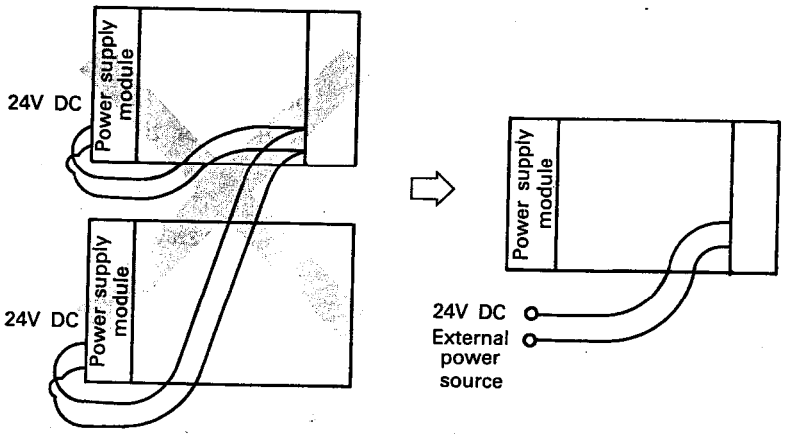
Power Supply Module	Transformer Capacity
A61P	110VA × n
A62P	110VA × n
A65P	110VA × n
A66P	95VA × n
A61VP	110VA × n

"n" stands for the number of power supply modules.

(e) When wiring, separate the PC power source from those for I/O equipment and power equipment as shown below.



(f) Precautions concerning the use of the 24V DC output of the A62P, A65P, and A66P power supply modules.
Avoid connecting the 24V DC output of multiple modules in parallel to one I/O module as this could lead to power supply module failure.
When the 24V DC output capacity of one power supply module is insufficient, use an external 24V DC power supply source.

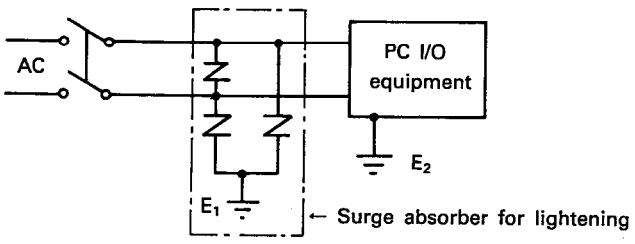


(g) Twist the 110V AC, 220V AC, and 24V DC cables as closely as possible. Connect modules with the shortest possible wire lengths.

(h) To minimize voltage drop, use the thickest (max. 2mm^2(14 AWG)) wires possible for the 110V AC, 220V AC, and 24V DC cables.

(i) Do not bundle the 110V AC and 24V DC cables with main-circuit wires or the I/O signal wires (high-voltage, large-current). Also, do not wire the above indicated cables close to the aforementioned wires. If possible, provide more than 100mm(3.94inch) distance between the cables and wires.

(j) As a measure against verylarge surges (e.g. due to lightening), connect a varistor as shown below.



IMPORTANT

(1) Ground the surge absorber (E_1) an the PC (E_2) separately from each other.

(2) Select a surge absorber making allowances for power voltage rises.

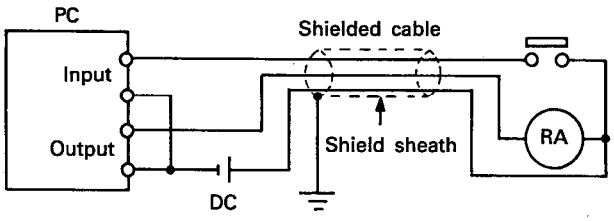
(2) Wiring of I/O equipment

(a) Applicable size of wire to the terminal block connector is 0.75(18) to 2mm^2(14 AWG). However, it is recommended to use wires of 0.75mm^2(18 AWG) for convenience.

(b) Separate the input and output lines.

(c) I/O signal wires must be at least 100mm(3.94inch) away from high-voltage and large-current main circuit wires.

(d) When the I/O signal wires cannot be separated from the main circuit wires and power wires, ground on the PC side with batch-shielded cables. Under some conditions it may be preferable to ground on the other side.



(e) If wiring has been done with of piping, ground the piping.

(f) Separate the 24V DC I/O cables from the 100V AC and 200V AC cables.

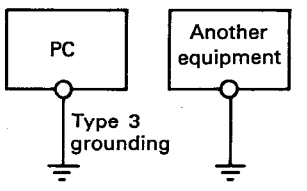
(g) If wiring over 200mm(7.87inch) or longer distance, trouble can be caused by leakage currents due to line capacity. Take corrective action as described in Section 13.4.

(3) Grounding

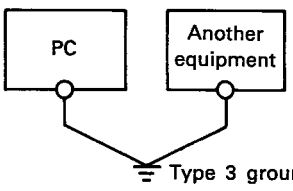
(a) The A series PC has good noise resistance. Therefore, the PC may be used without grounding except when there is excessive noise.
However, follow (b) to (e) described below.

(b) Ground the PC as independently as possible. Class 3 grounding should be used (grounding resistance 100Ω or less).

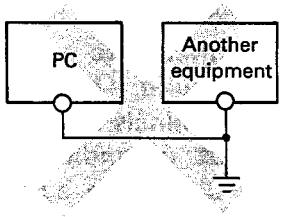
(c) When independent grounding is impossible, use the joint grounding method as shown in the figure below (2).



(1) Independent grounding ····· Best



(2) Joint grounding ····· Good



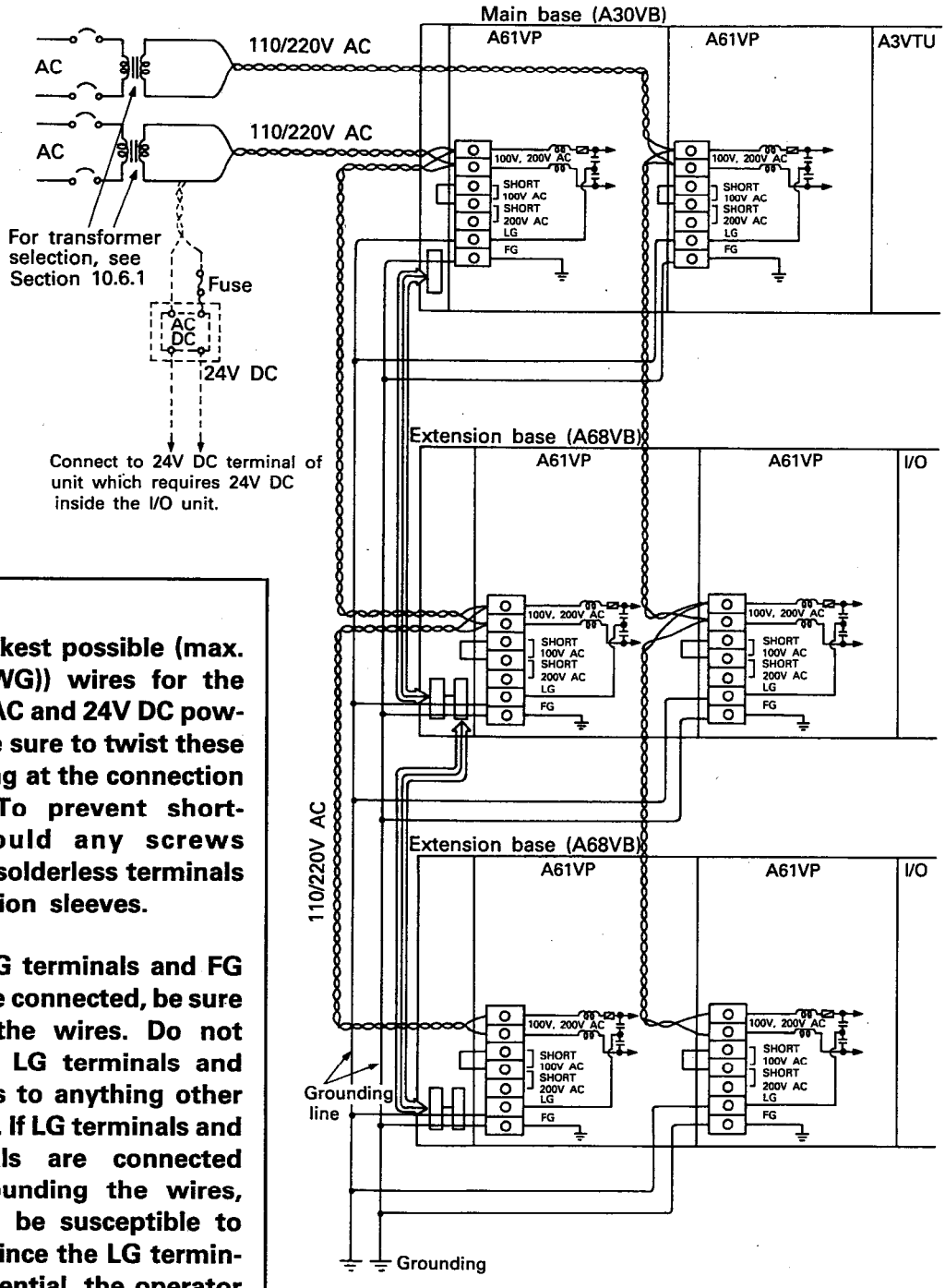
(3) Joint grounding ····· Not allowed

(d) Use 2mm^2(14 AWG) or thicker grounding wire. Grounding point should be as near as possible to the PC to minimize the distance of grounding cable.

(e) Should incorrect operation occur due to grounding, disconnect one or both of the LG and FG terminals of base units from the grounding.

10.6.2 Wiring to unit terminals

This section explains the wiring of power lines and grounding lines to the main and extension bases.



IMPORTANT

(1) Use the thickest possible (max. 2mm²(14 AWG)) wires for the 110V/220V AC and 24V DC power cables. Be sure to twist these wires starting at the connection terminals. To prevent short-circuit should any screws loosen, use solderless terminals with insulation sleeves.

(2) When the LG terminals and FG terminals are connected, be sure to ground the wires. Do not connect the LG terminals and FG terminals to anything other than ground. If LG terminals and FG terminals are connected without grounding the wires, the PC may be susceptible to noise, also since the LG terminals have potential, the operator may get an electric shock when touching metal parts.

10

11. TEST OPERATION AND ADJUSTMENTS

11.1 Check Points Before Start of Test Operation

This section explains the points to be checked prior to the test operation of programmable controller.

Item	Check Point	Description
1	Loading and setting of memory cassette	(1) Check that the memory cassette is securely inserted into the CPU module. Check that the memory cassette clicks when loaded. (2) Check that the used memory capacity matches the capacity of the memory cassette. (3) Check that the RAM/ROM setting is correct. (4) Check that the RAM or ROM is loaded securely. (When installed in the ROM socket) (5) Check that the memory protect is OFF.
2	Loading of battery (inside the memory cassette)	(1) Check whether the connector for battery lead wires, which has been disconnected before shipment, is securely inserted in the pin connector on the printed circuit board. (The red lead is positive and the blue lead negative.) (2) Check that the voltage of battery has not reduced. (Nominal value: 3.6V)
3	Connection of extension cable	(1) Check that the connectors of main base and extension base are properly connected with the connectors of extension cable. (2) Check that the connector position of extension base is correct.
4	Extension stage number setting of extension base	(1) Check that setting has been performed. (2) Check that the same number has been set. (3) Check whether one base has been set at more than one place.
5	Loading of modules	(1) Check that the types of unit loaded in each slot of main base and extension base is correct. (2) Check that the setting of the point setting switch of dummy unit (AG62) is proper. (3) Check whether the module configuration uses more I/O points more than the I/O points of CPU specifications.
6	Fuse	(1) Check if the fuse has blown or been damaged.
7	Connection of power and I/O cables	(1) Check the cables connected to each terminal of the terminal block. (2) Check the terminal screws of terminal block for the power supply module and terminal block for I/O module. (3) Check the cable size.

Table 11.1 Check Points

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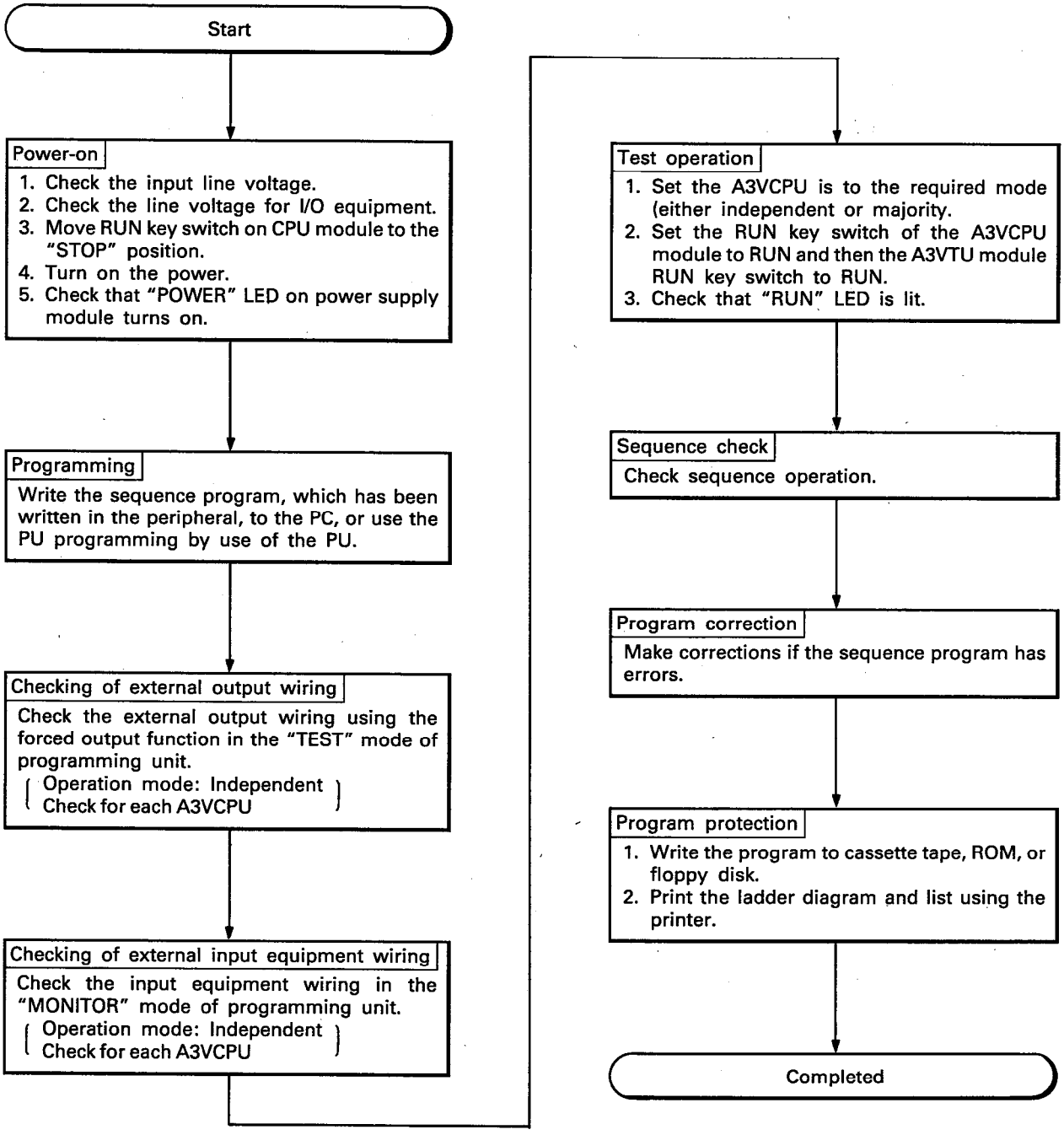
11.2 Test Operation and Adjusting Procedure



12. MAINTENANCE AND INSPECTION

This chapter describes items for daily and periodic maintenance and inspection in order to maintain the programmable controller in the normal and best conditions.

12.1 Daily Inspection

Table 12.1 shown the inspection items which are to be checked daily.

Number	Check Item		Check Point	Judgement	Corrective Action
1	Base unit mounting conditions		Check for loose mounting screws and cover.	The base unit should be securely mounted.	Retighten screws.
2	Mounting conditions of I/O module, etc.		Check if the module is disengaged or the hook is securely engaged.	The hook should be securely engaged and the module should be positively mounted.	Securely engage the hook.
3	Connecting conditions		Check for loose terminal screws.	Screws should not be loose.	Retighten terminal screws.
			Check distance between solderless terminals.	Proper clearance should be provided between solderless terminals.	Correct.
			Check connectors of extension cable.	Connections should not be loose.	Retighten connector mounting screws.
4	CPU module indicator lamps	"POWER" LED	Check that the LED is on.	On. (Off indicates an error.)	See section 13.3.2.
		"RUN" LED	Check that the LED is on during run.	On. (Off or flicker indicates an error.)	See Section 13.3.3 and 13.3.4.
		Input LED	Check that the LED turns on and off.	On when input is on. Off when input is off. (Display, which is not as mentioned above, indicates an error.)	See Section 13.3.6.
		Output LED	Check that the LED turns on and off.	On when output is on. Off when output is off. (Display, which is not as mentioned above, indicates an error.)	See Section 13.3.5.

Table 12.1 Daily Inspection

12.2 Periodic Inspection

This section explains the inspection items which are to be checked every six months to one year. If the equipment have been moved or modified or wiring has been changed, also make the inspection.

Number	Check Item		Checking Method	Judgement	Corrective Action
1	Ambient environment	Ambient temperature	Measure with thermometer and hygrometer. Measure corrosive gas.	0 to 55°C	When PC is used inside a panel, the temperature in the panel is ambient temperature.
		Ambient humidity		10 to 90%RH	
		Ambience		There should be no corrosive gases.	
2	Line voltage check		Measure voltage across 100/200V AC terminal.	85 to 132V 170 to 264V AC	Change supply power. Change transformer tap.
3	Mounting conditions	Looseness, play	Move the unit.	The module should be mounted securely and positively.	Retighten screws. For CPU, I/O, and power supply modules check all connections.
		Ingress of dust or foreign material	Visual check.	There should be no dust or foreign material, in the vicinity of the P.C.	Remove and clean.
4	Connecting conditions	Loose terminal screws	Retighten.	Connectors should not be loose.	Retighten.
		Distances between solderless terminals.	Visual check.	Proper clearance should be provided between solderless terminals.	Correct.
		Loose connector	Visual check.	Connectors should not be loose.	Retighten connector mounting screws.
5	Battery		Check battery status by monitoring special auxiliary relays M9006 and M9007. Replace battery if necessary.	Preventive maintenance	If battery capacity reduction is not indicated, change the battery when specified service life is exceeded.
6	Fuse		Check fuses.	Preventive maintenance	Change the fuse periodically due to rush current.

Table 12.2 Periodic Inspection

12.3 Replacement of Battery

M9006 or M9007 turns on when the voltage of battery for program backup and power failure compensation reduces.
Even if this special relay turns on, the contents of the program and power failure compensation are not lost immediately.
However, if the ON state is overlooked, the PC contents may be lost.
Special auxiliary relays M9006 and M9007 are switched on to indicate that the battery life has reduced to the time (minimum) indicated in Table 12.3 and it must be replaced if continued power failure RAM and/or data back-up is required.
The following sections gives the battery service life and the battery changing procedure.

12.3.1 Service life of battery

This service life of the battery depends on the capacity of the memory. Table 12.3 shows service life according to memory.

Battery Life / Memory Cassette Type	Battery Life (Total power failure time) [Hr]		
	Guaranteed value (Min)	Actually applied value (Typ)	After M9006 & M9007 are set ON. (Min)
A3NMCA-0	10800	27000	200
A3NMCA-2	7200	18000	200
A3NMCA-4	5400	13000	170
A3NMCA-8	3600	9000	170
A3NMCA-16	2150	5400	130
A3NMCA-24	1950	4900	100

*The actually applied value indicates a typical value and the guaranteed value indicates the minimum value.

Table 12.3 Battery Life

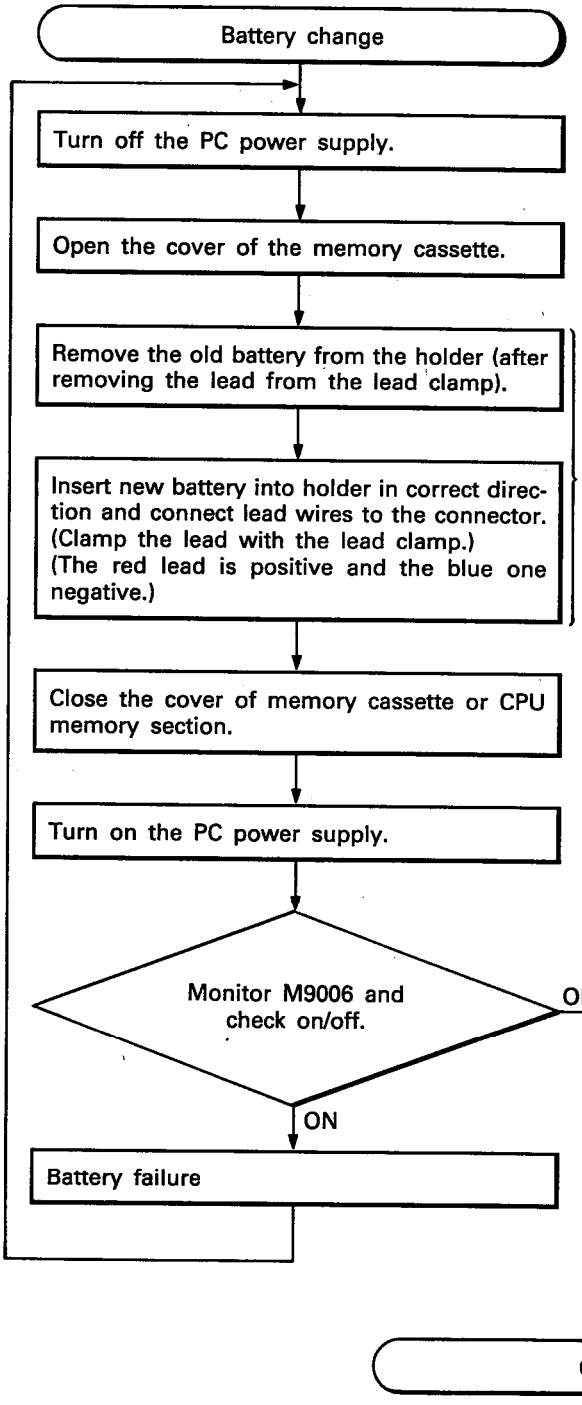
Preventive maintenance is as described below.

1) Even if the total power failure time is less than the guaranteed value in the above table, change the battery after four to five years.

2) When the total power failure time has exceeded the guaranteed value in the above table and M9006 has turned on, change the battery.

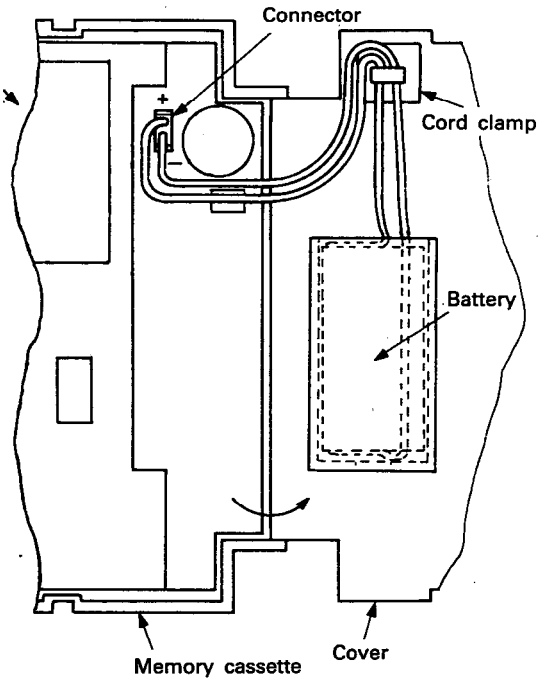
12.3.2 Battery changing procedure

When the service life of the battery has expired, change the battery using the following procedure.
Even if the battery is removed, the memory is backed by a capacitor for some time.
However, if the changing time exceeds the guaranteed value shown in the following table, the contents of the memory may be lost. Therefore, change the battery as fast as possible.



Memory Cassette Type	Capacitor Backup Time [Minute]	
	Guaranteed value (Min)	Actually applied value (Typ)
A3NMCA-0	18	45
A3NMCA-2	12	30
A3NMCA-4	9	20
A3NMCA-8	6	15
A3NMCA-16	4	10
A3NMCA-24	3	8

Table 12.4 Backup Time by Capacitor

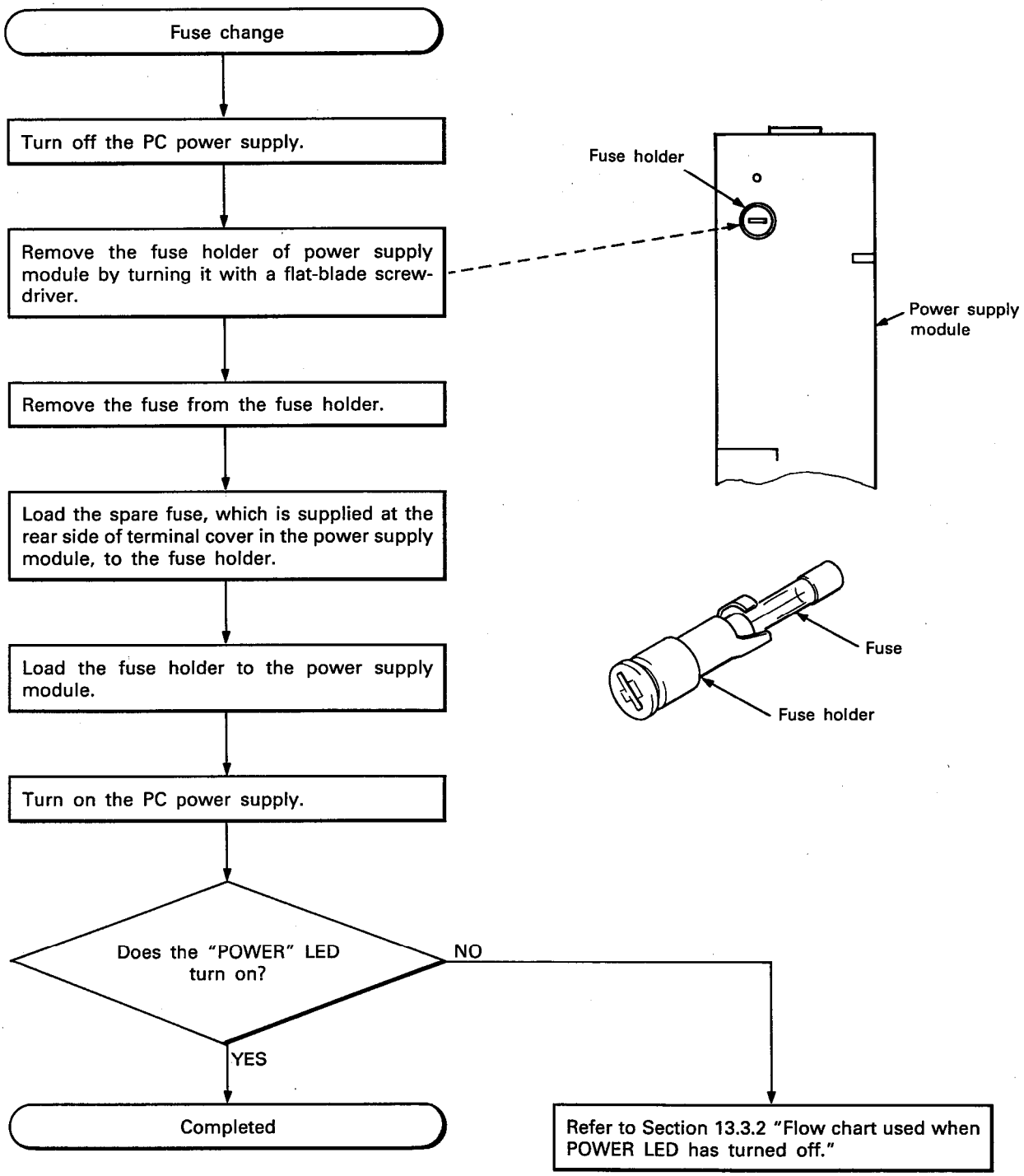


12.4 Replacement of Fuse

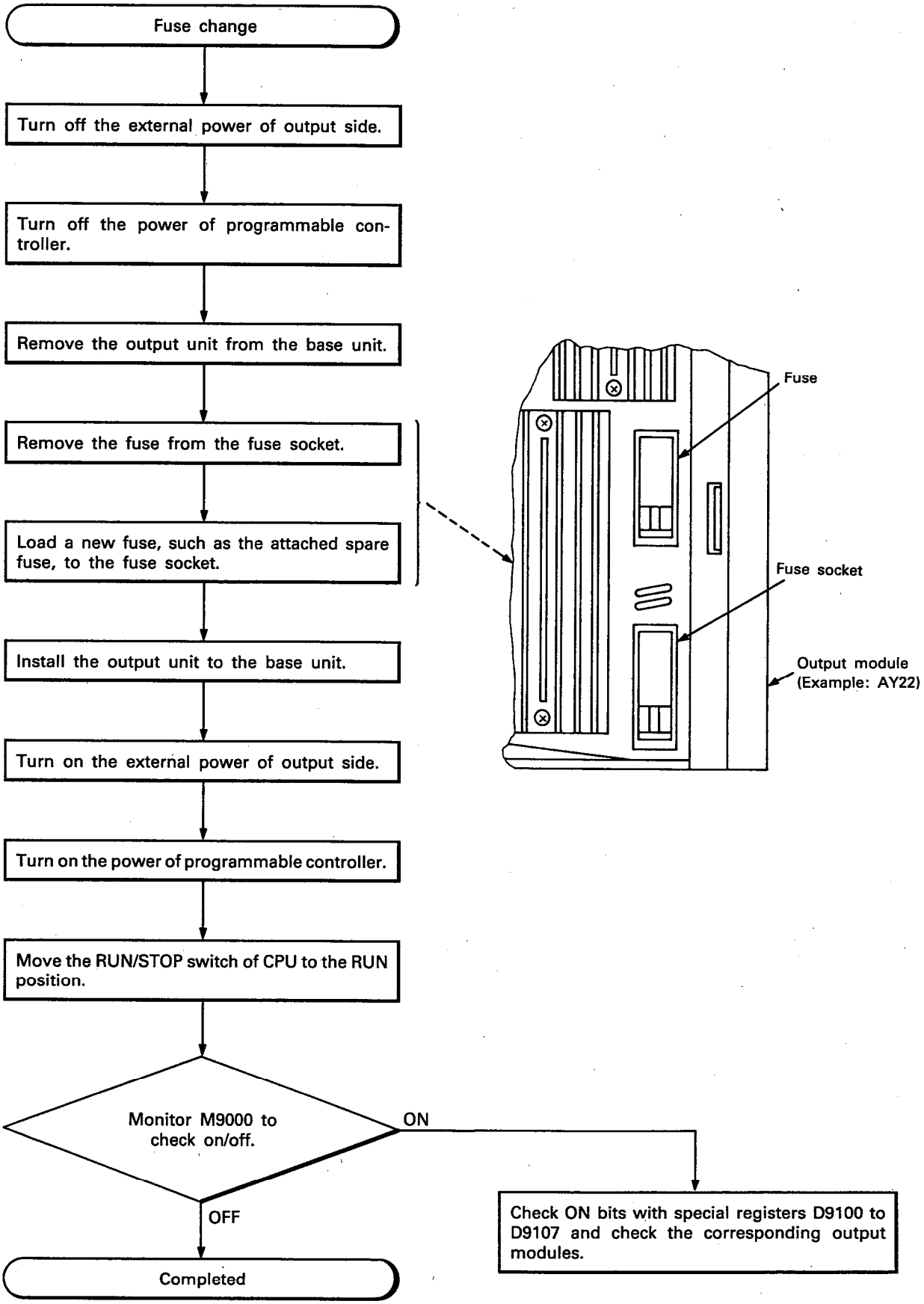
Even if the fuse does not blow, its element may be consumed due to rush current. Therefore, it is recommended to change the fuse periodically.

12.4.1 Replacement of fuse for power supply

The fuse changing procedure is explained.



12.4.2 Replacement of fuse for output module



13. TROUBLESHOOTING

13.1 Error Code List

When an error is generated when a programmable controller is started or while it is running, the self-diagnosis function will stop the CPU or system. An error message is displayed and the error code (including step number) corresponding to the contents of the error are stored in the register.
Two self-diagnosis functions are provided in the A3VTS system, one for diagnosis of each of the A3VCPUs and the other for diagnosis of the A3VTU. The following section explains the error descriptions provided by the diagnosis concerning the source of the errors, how to restore them, and how to read the error codes (error step).

13.1.1 Errors diagnosed by the A3VCPU

The self-diagnosis function is used in each of the three A3VCPUs for diagnosis of each of the A3VCPUs and A3VTUs.
The following explains the error numbers, error messages, and the means to restore errors.
In the following table, the numbers appearing in the far right column reflect the precedence a particular error has over other errors in being displayed, with those of the smaller numbers having the higher priority. If two errors of the same precedence occur, the one being generated earlier is given precedence.

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"A3VTU ERROR" (Checked continuously)	5	Stop	Data communication cannot be conducted with the A3VTU.	• When generated while installing an A3VCPU during system operation, reset the A3VCPU. • Check to see if the A3VTU has been properly installed. • Since it is possible that the A3VTU is locked up, try resetting it. • Since continued trouble indicates a hardware malfunction in the A3VTU or A3VCPU, consult Mitsubishi representative.	2
"BATTERY ERROR" (Checked continuously)	70	Run	(1) The battery voltage has reduced to less than the specified value. (2) The battery lead is disconnected.	(1) Change the battery. (2) When RAM or power failure compensation is used, connect the battery.	5
"CAN'T EXECUTE (I)" (Checked at the execution of IRET instruction)	15	Stop	The [IRET] instruction is present in the main routine program. (When present after the [FEND] instruction an error is not generated.)	Read the step containing the error using a peripheral device and remove the [IRET] instruction.	3

Table 13.1 Error Code List (Continue)

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"CAN'T EXECUTE (P)" (Checked at [CJ], [SCJ], [JMP], [CALLP] execution, STOP to RUN, PAUSE to RUN)	13	Stop	(1) There is no jump destination or plural destinations specified by the [CJ], [SCJ], [CALL], [CALLP] or [JMP] instruction. (2) There is a [CHG] instruction and no setting of subprogram. (3) Although there is no [CALL] instruction, the [RET] instruction exists in the program and has been executed. (4) The [CJ], [SCJ], [CALL], [CALLP] or [JMP] instruction has been executed with its jump destination located below the [END] instruction.	(1) Read the error step by use of peripheral equipment and correct the program at that step. (Make correction such as the insertion of jump destination or the changing of jump destinations to one.)	3
"CASSETTE ERROR" (Checked at power on, reset)	16	Stop	The memory cassette is not loaded.	Load the memory cassette and reset.	3
"CHK FORMAT ERR." (Checked at STOP to RUN, PAUSE to RUN)	14	Stop	(1) An instruction other than LDX, LDIX, ANDX, and ANIX, (including [NOP]) has been included in the [CHK] instruction circuit block. (2) Multiple [CHK] instructions are present. (3) The number of connect points within the [CHK] instruction circuit block exceeds 150. (4) The X device No. within the [CHK] instruction circuit block exceeds X7FE. (5) The [CHK] instruction circuit block is not preceded by a [CJ□] circuit block. (6) The D1 device (No.) of the [CHK D1 D2] instruction and the connect point device (No.) prior to the [CJ□] instruction do not match. (7) Pointer P254 is not appended to the top of the [CHK] instruction circuit block. P254 [CHK D1 D2]	(1) Check to see if (1) through (7) of the column on the left applies to the [CHK] instruction circuit block program. Use peripheral device to correct any mistakes, and begin operation again.	3
"DPRAM ERROR" (Checked at power on, reset)	6	Stop	Can not access the dual port RAM.	• When generated while installing an A3VCPU during system operation, reset the A3VCPU. • Check to see if the A3VTU has been properly installed. • Since it is possible that the A3VTU is locked up, try resetting it. • Since continued trouble indicates a hardware malfunction in the A3VTU or A3VCPU, consult Mitsubishi representative.	2

Table 13.1 Error Code List (Continue)

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"END NOT EXECUTE" (Checked at the execution of END instruction)	24	Stop	(1) When the END instruction is executed, another instruction code has been read due to noise, etc. (2) The END instruction has changed to another instruction code for some reason.	Perform reset and run. If the same error is displayed again, it is the CPU hardware error. Therefore, consult Mitsubishi representative.	3
"INSTRCT. CODE ERR." (Checked during instruction execution)	10	Stop	Instruction code, which cannot be decoded by CPU, is included in the program. (1) ROM including invalid instruction code, has been loaded. (2) Memory contents have been corrected.	(1) Read the error step by use of peripheral equipment and correct the program at that step. (2) In the case of ROM, rewrite the contents of the ROM or change the ROM.	3
"MISSING END INS." (Checked at M9056 or M9057 ON, STOP to RUN, PAUSE to RUN)	12	Stop	(1) There is no END (FEND) instruction in the program. (2) When subprogram has been set in parameters, there is no END instruction in the subprogram.	Write END at the end of the program/subprogram.	3
"OPE. CIRCUIT ERR." (Checked at power on, reset)	21	Stop	The operation circuit, which performs the sequence processing in the CPU, does not operate properly.	Since this is CPU hardware error, consult Mitsubishi, representative.	3
"OPERATION ERROR" (Checked at instruction execution)	50	Run (Stop)	(1) The result of BCD conversion has exceeded the specified range (9999 or 99999999). (2) Setting has been performed exceeding the specified device range and operation cannot be performed. (3) File registers are used in the program without performing the capacity setting of file registers.	Read the error step by use of peripheral equipment, and check and correct the program at that step. (Check device setting range, BCD conversion value, etc.)	4
"PARAMETER ERROR" (Checked at power on, reset, STOP to RUN, PAUSE to RUN)	11	Stop	(1) Capacity larger than the memory capacity of CPU has been set and then write to CPU has been performed. (2) The contents of parameters of CPU memory have changed due to noise or the improper loading of memory.	(1) Check the memory capacity of CPU with the memory capacity set by peripheral equipment and re-set incorrect portion by the peripheral equipment. (2) Check the loading of CPU memory and load it correctly. (3) Read the parameter contents of CPU memory, check and correct the contents, and write them to the memory again.	3
"RAN ERROR" (Checked at power on, reset)	20	Stop	The CPU has checked if write and read operations can be performed properly to the data memory area of CPU, and as a result, either or both has not been performed.	Since this is CPU hardware error, consult Mitsubishi, representative.	

Table 13.1 Error Code List (Continue)

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"SP. UNIT ERROR" (Checked at the execution of FROM and TO instructions)	46	Stop (Run)	Access (execution of FROM to TO instruction) has been made to a location where there is no special function module.	Read the error step by use of peripheral equipment, and check and correct the content of FROM or TO instruction at that step by use of peripheral equipment.	4
"WDT ERROR" (Checked continuously)	25	Stop	The END instruction cannot be executed with the program looped.	Check for an endless loop and correct the program.	1
"WDT ERROR" (Checked at the execution of END instruction)	22	Stop	Scan time exceeds watch dog error monitor time. (1) Scan time of user program has become excessive. (2) Scan time has lengthened due to instantaneous power failure which occurred during scan.	(1) Calculate and check the scan time of user program and reduce the scan time by use of CJ instruction, etc. (2) Monitor the content of special register D9005 by use of peripheral equipment. When the content is other than 0, line voltage is insufficient. Therefore, check the power and eliminate the voltage fluctuation.	3

Table 13.1 Error Code List

POINT

(1) When an "A3VTU ERROR" or "DPRAM ERROR" is generated, an error code is entered into special register D9008 of the A3VCPU generating the error. However, there are occasions when the error numbers and error codes are not set for special relays M9096 to M9098, special registers D9096 to D9098 of each A3VCPU.

(2) In the table, when Run (Stop) is indicated at the CPU Status, whether the CPU should Run or Stop can be selected with a parameter.

13.1.2 Errors diagnosed by the A3VTU

There is self-diagnosis that is conducted by the A3VTU on itself and that which is based on error messages from the dual power supply modules. Self-diagnosis is conducted on the three A3VCPUs and A3VTUs.
The following explains the error numbers, error messages, and the means to restore errors.
In the following table, the numbers appearing in the far right column reflect the precedence a particular error has over other errors in being displayed, with those of the smaller numbers having the higher priority. If two errors of the same precedence occur, the one being generated earlier is given precedence.

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"CIRCUIT ERROR" (Checked at power on, reset)	101	Stop	Faulty majority circuit.	There is a hardware malfunction in the A3VTU. Consult Mitsubishi representative.	1
"CONTROL -BUS ERR." (Checked at the execution of FROM and TO instructions)	40	Stop	FROM and TO instructions cannot be executed. (1) Malfunction in control bus to a special function module.	A hardware malfunction exists in either the special function module, CPU module, or base unit. Isolate the malfunction by replacing the units. Consult Mitsubishi representative.	1
"ERROR CPU A[ ]" (Checked continuously)	130	Operation continued if switching to other CPUs possible. Operation stopped if switching to other CPUs not possible.	(1) Parameters of each of the A3VCPUs do not match. (2) Synchronous communication cannot be conducted between the A3VTU and A3VCPU due to one of the following reasons. • A3VCPU is not installed. • A3VCPU has been reset. • A3VCPU is locked-up. • A3VCPU generated an error. • Programs are different.	(1) Check the parameters and programs of each A3VCPU and correct any mistakes. After correcting reset the A3VTU. (2) Ensure that the A3VCPU is properly installed. (3) Check if the error message LEDs on the front panel of the A3VCPU are displayed, and if so, remedy the errors according to the messages. (4) Reset the A3VCPU. (5) A possible hardware malfunction exists in either the A3VTU, base unit, or A3VCPU if none of the above measures restores normal operation. If so, replace the faulty module.	3
"ERROR CPU B[ ]" (Checked continuously)	131				
"ERROR CPU C[ ]" (Checked continuously)	132				
"FUSE BREAK OFF" (Checked at the execution of END instruction)	32	Run (Stop)	There is an output module of which fuse has blown.	(1) Check the fuse blow indicator LED of output module and change the fuse of module of which LED is on. (2) The check of fuse blow module can also be made by the peripheral equipment. Among special registers D9100 to D9107, the bit corresponding to the module of verify error is "1". Therefore, make checks by monitoring the registers.	2

Table 13.2 Error Code List (Continue)

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"HEAT ERROR" (Checked continuously)	170	Run	Either one or both of the dual power supply modules are overheating.	(1) Check to see if the operating ambient temperature is not excessively high, and that the amount of space available around the programmable controller is not less than minimum requirements. (2) If no problem is found in (1), a hardware malfunction exists in the power supply module. Consult Mitsubishi representative.	7
"I/O INT. ERROR" (Checked at the occurrence of interruption)	43	Stop	An interrupt was generated even though an interrupt module is not installed.	A hardware malfunction exists in one of the modules. Isolate the malfunction by replacing the units. Consult Mitsubishi representative.	1
"LINK F ERROR" (Checked continuously)	180	Run	An error has been generated in the F-LINK loop circuit. (Power may be OFF, or the link module or cable may be faulty.) Only the A3VTU of the master station is detected.	(1) Check the power supply module and, if it is OFF, turn to ON, and then press the reset button on the link module. (2) Check to see if there is a faulty cable or connector. Repair if necessary. (3) If (1) and (2) reveal normal, a hardware malfunction exists in the power supply module. Consult Mitsubishi representative.	4
"LINK R ERROR" (Checked continuously)	181	Run	An error has been generated in the R-LINK loop circuit. (Power may be OFF, or the link module or cable may be faulty.) Only the A3VTU of the master station is detected.		4
"LINK PARA. ERROR" (Checked at power on, reset, STOP to RUN, PAUSE to RUN)	47	Run	(1) The contents, which have been written to the parameter area of link by setting the link range in the parameter setting of A6GPP, A6PHP or A6HGP, are different from the link parameter contents for some reason. (2) The setting of the total number of slave stations is 0.	(1) Write parameters again and make check. (2) When the error is displayed again, it is the hardware error. Therefore, consult Mitsubishi representative.	6
"LINK UNIT ERROR" (Checked at power on, reset, STOP to RUN, PAUSE to RUN)	42	Stop	AJ71R22 or AJ71P22 is loaded in the master station.	Remove the AJ71R22 or PJ71P22 from the master station. After correction, perform reset and start at the initial operation.	1
"POWER ERROR" (Checked continuously)	150	Continued operation possible if other power supply module operating normally. If not, operation stops.	One of the two power supply modules malfunctioned. (Power OFF or hardware malfunction)	(1) Check that wiring to the power supply modules and that the power is ON. (2) If (1) is normal, a hardware malfunction exists in the power supply module. Consult Mitsubishi representative.	5

Table 13.2 Error Code List (Continue)

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"RAM ERROR□" □—DPRAM A □—DPRAM B □—DPRAM C □—Internal RAM □—Addressed RAM (Checked at power on, reset)	100	Stop	(1) Data read/write cannot be conducted between the A3VTU and A3VCPU 2-port RAM. (2) Data read/write cannot be conducted between the A3VTU and internal RAM.	A hardware malfunction exists. Consult Mitsubishi representative.	1
"ROM ERROR" (Checked at power on, reset)	—	Stop	OS-ROM malfunction.	A hardware malfunction exists in the A3VTU. Consult Mitsubishi representative.	1
"SOURC CPU DOWN" (Checked at power on, reset, STOP to RUN, PAUSE to RUN)	102	Stop	At the point of power application, when changing from STOP/PAUSE to RUN, or during CPU restore processing, all A3VCPUs originating transmission stop during data memory transmission.	Reset the A3VTU. If operation is not restored to normal, a hardware malfunction exists in the A3VCPU. Consult Mitsubishi representative.	1
"SP. UNIT DOWN" (Checked at the execution of FROM and TO instructions)	41	Stop	When the FROM or TO instruction is executed, access has been made to the special function module but the answer is not given. (1) The accessed special function module is defective.	Since this is the accessed special function unit error, consult Mitsubishi representative.	1
"SP.UNIT LAY.ERR." (Checked at power on, reset, STOP to RUN, PAUSE to RUN)	44	Stop	(1) Three or more computer link modules are loaded with respect to A3VTS one system. (2) Two or more units of AJ71P21 or AJ71R21 are loaded. (3) Two or more interrupt modules are loaded. (4) In the parameter setting of A6GPP, while I/O module is actually loaded, special function module has been set in the I/O assignment, and vice versa. (5) Malfunction in special function unit used in access execution.	(1) Remove the AJ71C24(S3) as it can no longer be used. For the AD51, use only one or two units. (2) Reduce the AJ71P21 or AJ71R21 to one or less. (3) Reduce the interrupt module to one. (4) Re-set the I/O assignment of parameter setting by use of A6GPP according to the actually loaded special function module.	1
"STATION No. □□*□□" Displays set station numbers of the right and left link modules in hexadecimal. (Checked at power on, reset)	190	Stop	The station numbers of the two link modules AJ71VP21/R21s are incorrect.	Reset the station numbers to the same value. Reset the A3VTU.	1

Table 13.2 Error Code List (Continue)

Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"STATION No. ERR." (Checked at starting up of link operation, reset of the link module)	191	Run	The station number of a link module AJ71VP21/R21 that has been newly installed during system operation differs from the station number of the other AJ71VP21/R21.	Reset the station number, and press the RESET button located on the front panel of the link module.	2
"TIME OVER CPU A"	110	Operation continued if switching to other CPUs possible. Operation stopped if switching to other CPUs not possible.	Timing instructions executed by the A3VTU during majority operation or single-module operation cannot be executed within the period allocated when a mistake in a program of a A3VCPU is present after one A3VCPU (two during majority operation) has executed operation, or when a hardware malfunction exists in a A3VCPU.	(1) Check the program between the A3VCPUs and correct mistaken portions. After finishing, reset the A3VTU. (2) If (1) is normal, a hardware malfunction exists in the A3VCPU. Consult Mitsubishi representative.	3
"TIME OVER CPU B"	111				
"TIME OVER CPU C"	112				
"UNIT VERIFY ERR." (Checked at the execution of END instruction)	31	Stop (Run)	I/O module data is different from that at power-on. (1) The I/O module (including the special function module) is incorrectly disengaged or has been removed, or a different module has been loaded.	(1) Among special registers D9116 to D9123, the bit corresponding to the module verify error is "1". Therefore, monitor the registers by use of peripheral equipment and check for the module with "1". (2) When the fault has been corrected reset CPU.	2
"VERIFY ERROR" (Checked when two units are operating)	140	Run	(1) Generated when an inconsistency is found in output (Y) after an output verification of a standby CPU and an operating CPU when both modules are operating. (2) There is a program error or a hardware malfunction in the A3VCPU.	(1) Check the program between the two CPUs and correct mistaken portions. After finishing, reset the A3VTU. (2) If (1) is normal, a hardware malfunction exists in the A3VCPU. Consult Mitsubishi representative.	3
"VOTE ERROR CPU A" (Checked during majority operation)	120	Operation continued if switching to other CPUs possible. Operation stopped if switching to other CPUs not possible.	Generated when, during majority operation, a program differs with that of another CPU or a hardware malfunction in the A3VCPU results in the CPU [ ] data being determined as a majority error.	(1) Check the program between the A3VCPUs and correct mistaken portions. After finishing, reset the A3VTU. (2) If (1) is normal, a hardware malfunction exists in the A3VCPU. Consult Mitsubishi representative.	3
"VOTE ERROR CPU B" (Checked during majority operation)	121				
"VOTE ERROR CPU C" (Checked during majority operation)	122				

Table 13.2 Error Code List (Continue)

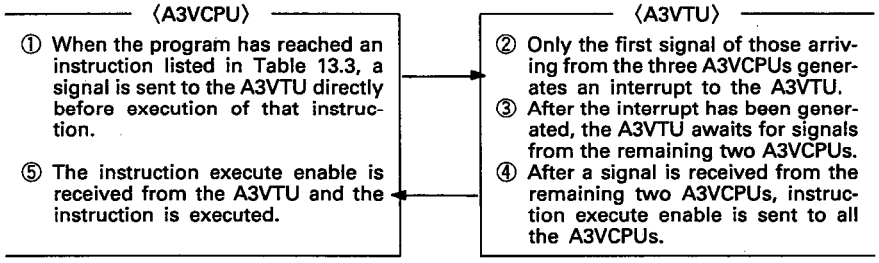
Error Message (Check timing)	Content of Special Register D9008 (BIN value)	CPU States	Error and Cause	Corrective Action	No.
"WDT ERROR" (Check continuously)	25	Stop	Infinite-loop execution on lock-up due to frequent occurrence of momentary power failure within a short period (approx. 200 ms) or a hardware malfunction in A3VTU.	(1) Check the contents of special register D9005 and reset the A3VTU. If the contents of D9005 is "0", a hardware malfunction exists in the A3VTU. Consult Mitsubishi representative.	1

Table 13.2 Error Code List

REMARKS

1. In the table, when Run (Stop) is indicated at the CPU Status, whether the CPU should Run or Stop can be selected with a parameter of each A3VCPU. This enables system operation and stop to be determined by the majority of the parameters of three A3VCPUs.
   Stopping A3VTU operation means stopping system operation.
2. Detailed information concerning the contents of error messages are shown below.

   (1) [TIME OVER CPU□]
   (a) The A3VTU provides timing so that A3VCPUs (two during single-module operation, three during majority operation) can synchronously execute the commands listed in Table 13.3. The following gives the procedure.



END	DFROP	DTOP	FEND
FROM	TO	SEG	CHG
FROMP	TOP	PR	STOP
DFRO	DTO	PRC	SUB
LRDP	LWTP		

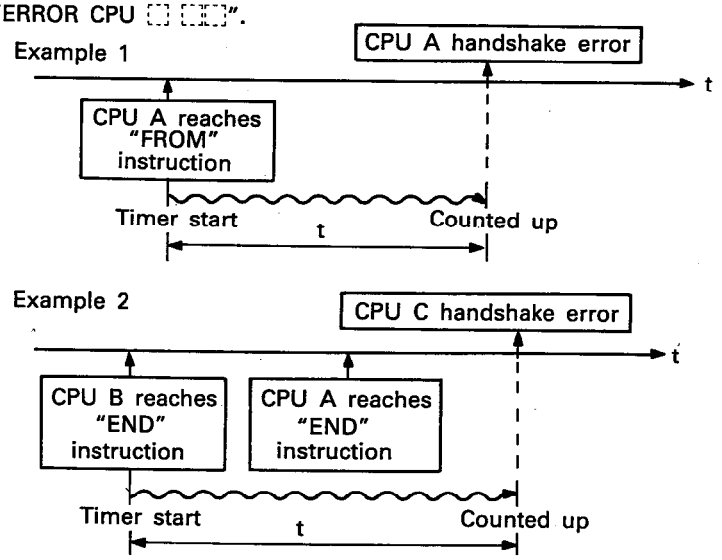
Table. 13.3 Instructions whose Execution is Based on A3VTU Timing

   (b) Single-module operation
   When the next instruction to be executed by the operating CPU is one of the above instructions and the standby CPU has yet to reach that instruction, or if the reverse is true, the standby CPU generates the error "TIME OVER CPU □" and operation continues with the operating CPU.

(c) Majority operation

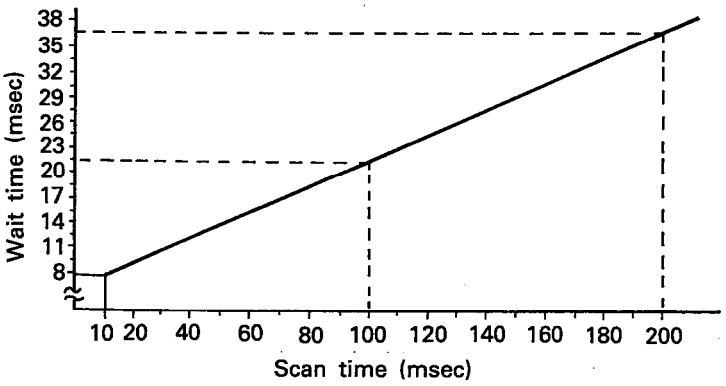
The error content differs depending on whether one of the above instructions is to be executed by one or two CPUs.

If the program of one CPU reaches that point of the program and the other two CPUs have not reached it within a determined time, the CPU that reached the instruction generates a handshake error, "ERROR CPU □ □□". If two CPUs reached that point of the program and the third has not, the CPU that did not reach the instruction generates a time check error, "TIME OVER CPU □" and is dropped from operation. If two CPUs reach a certain instruction and the third CPU reaches a different timing instruction, the third CPU generates a handshake error, "ERROR CPU □ □□".



(d) The A3VTU checks whether or not timing of instruction listed in Table 13.3 falls within determined limits.

The value of the time limits varies according to scan time as shown in the following figure.



(e) A3VTU synchronization does not take into account the CPU in the error or wait status.

(2) Majority decision error

(a) The A3VTU verifies the results of majority operations with operation results of each A3VCPU to check that they are the same. The majority decision error "VOTE ERROR CPU □" is generated with the A3VCPU which provides different operation result and the A3VTU forces operation of that A3VCPU to stop.

(b) The majority check verifies only the output (Y) data.
The following figure shows the contents of the output (Y) Majority check.

CPU A	CPU B	CPU C	Majority Decision Results	Check Results
1	1	1	1	No errors
1	1	0	1	Error in CPU C
1	0	1	1	Error in CPU B
1	0	0	0	Error in CPU A
0	1	1	1	Error in CPU A
0	1	0	0	Error in CPU B
0	0	1	0	Error in CPU C
0	0	0	0	No errors

(c) The following could be sources of a "Majority Decision Error": error in programming, malfunctioning A3VCPU, faulty input/output due to noise, etc. When the "Majority Decision Error" is generated, reset the A3VCPU one time and check if operation is restored to normal.

(3) CPU handshake error, "ERROR CPU[ ] [ ]"
Handshaking is normally monitored between the A3VTU and each A3VCPU, and an error is generated when handshaking fails to occur normally.
If a malfunction occurs in the A3VTU, the A3VCPU detects the malfunction and displays "A3VTU ERROR".
When one of the following malfunctions occurs in the A3VCPU, the A3VTU detects it and displays the message "A3VTU ERROR".
(a) During majority operation, when power is applied, when changing from STOP/PAUSE to RUN, or during CPU restore processing, the parameters of each CPU are checked to see if they agree.
- When power is applied or when changing from STOP/PAUSE to RUN
  - If the values of two of the CPUs agree, an error "ERROR CPU[ ] [ ]" is generated for the CPU with the value not agreeing.
  - If none of the three CPUs agrees, an error "ERROR CPU[ ] [ ]" is generated for CPU B and CPU C.
- During CPU restore processing
  - The parameters of all CPUs in either RUN/PAUSE/STOP status are checked to see if they agree with the parameters of the CPU being restored. If they are not in agreement, an error "ERROR CPU[ ] [ ]" is generated.

(b) During processing of an instruction listed in Table 13.3, a check is conducted by the A3VTU to determine whether or not the instruction was reached by each of the CPUs within a set time limit (See 2-(1)-(d).)
- Majority operation
  - If two of the CPUs reached the same instruction and the third CPU reaches a different instruction listed in Table 13.3, an error "ERROR CPU[ ] [ ]" is generated for the third CPU.
  - If each of the three CPUs reach different instructions, then an error "ERROR CPU[ ] [ ]" is generated for CPU B and CPU C.
- Single-module operation
  - If both of the CPUs reach different instructions, then error "ERROR CPU[ ] [ ]" is generated for the standby CPU.

(4) Dual power supply module error "POWER ERROR".
If a dual power supply module detects a malfunction during self-diagnosis, power is switched immediately to the other power supply module, a fault number is output to the A3VTU, and the "POWER" LED of the malfunctioning module is lit.
The A3VTU is provided with logical sum of the malfunction signals from all dual power modules installed in the base unit or extension base unit. Therefore, determine the malfunctioning power supply module by checking the "POWER" LED of each unit.

(5) Dual power supply module overheat error "HEAT ERROR"
If a dual power supply module detects an overheating during self-diagnosis, the "HEAT" LED of the overheating module is lit.
The A3VTU is provided with logical sum of the overheat from all dual power modules installed in the base unit or extension base unit. Therefore, determine the malfunctioning power supply module by checking the "HEAT" LED of each unit.
Since the overheat error is an alarm and not a malfunction, it is not necessary that an immediate replacement of a power supply module be made. However, if the reasons for the overheating condition are not remedied, the module may malfunction. It is therefore important that a fan be used to lower quickly the ambient temperature and that the cause of overheating be found and remedied.

3. How to read error codes
When an error has been generated, the error code can be read with the use of peripheral device.
When an error has been detected by an A3VCPU, connect a peripheral device to the malfunctioning A3VCPU and read the error code (error step) by putting the peripheral device in the test mode.
When an error has been detected by an A3VTU, the connect a peripheral device to the an A3VCPU and read the error code by monitoring the special registers D9096 to D9099.

13.2 Basic Troubleshooting

System reliability depends not only on reliable equipment but also on short down-fines in the event of faults.
Since the A3VTS system provides multiple power supply and CPU modules, operation can continue without stopping even when one module malfunctions.
However, it is important that modules be replaced or troubleshooting be conducted to determine the cause of failure in order to prevent the system from stopping in case of recurrence of the problem.
This section describes the basic points of troubleshooting.

(1) Visual checks

Check the following points.
1) Machine motions (in stop and operating statuses)
2) On or off of power
3) Status of I/O equipment
4) Conditions of wiring (I/O wires, cables)
5) Display states of various indicators (such as POWER LED, RUN LED, and I/O LED)
6) States of various setting switches (such as extension base)

After checking 1) to 6), connect the peripheral equipment and check the running status of PC and the contents of program.

(2) Trouble check

Since the system can continue normal operation even with a power supply module or CPU malfunctioning, it is sometimes difficult to determine the cause of the malfunction.
While some checks can be conducted without stopping system operation, there are some checks that can be made only with the operation stopped. If system operation cannot be immediately stopped, wait until it can be stopped (as soon as possible) and then conduct the following operations to determine how the malfunction changes.
1) Set the RUN key switch to the "STOP" position. (A3VTU, A3VCPU)
2) Perform reset by the RESET key switch. (A3VTU, A3VCPU)
3) Turn the power on and off.

(3) Narrow down the possible causes of teh trouble

In order to determine the cause of a malfunction as soon as possible, it is necessary to narrow the range of possibilities in which the malfunction may have occurred.
Assume the cause of malfunction from the following through steps (1) and (2).
1) Inside or outside of PC.
2) I/O module or another module.
3) Sequence program.

13.3 Troubleshooting

The multiplex configuration of the A3VTS system enables the system to continue operations even when a malfunction has occurred. However, if the cause of malfunction is left unremedied, it is possible that operation will stop with the next appearance of the next malfunction.
When a malfunction occurs, follow the troubleshooting flowchart provided below to determine the cause of the problem and remedy the same.

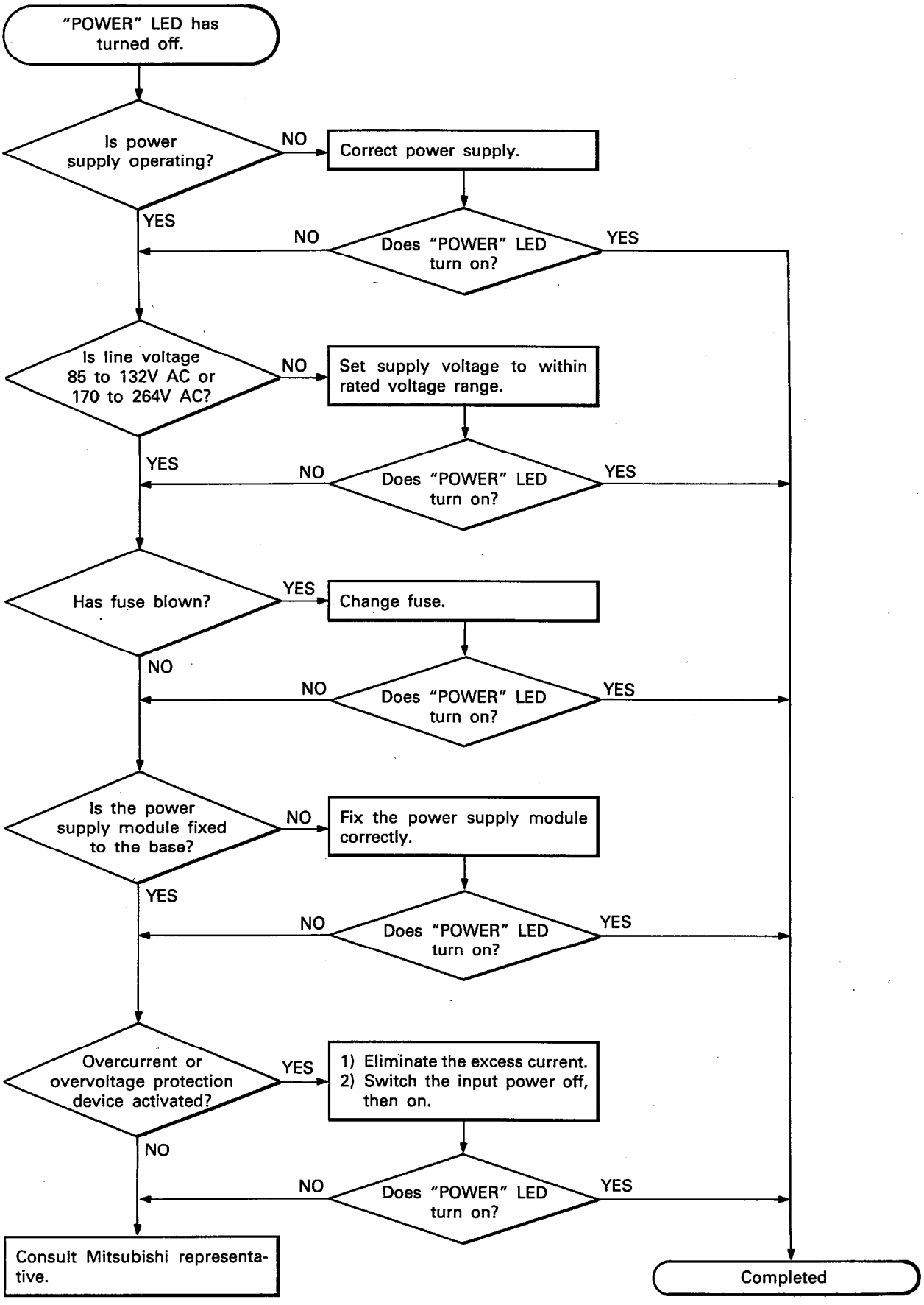
13.3.1 Troubleshooting flow charts

Details for fault finding may be found as follows.

Occurrence of error

Is "POWER" LED off?	⇨	To Section 13.3.2 "Flow chart used when "POWER" LED has turned off"
Is "RUN" LED off?	⇨	To Section 13.3.3 "Flow chart used when "RUN" LED has turned off"
Is "RUN" LED of the A3VTU or A3VCPU flickering?	⇨	To Section 13.3.4 "Flow chart used when "RUN" LED flickers"
Output module does not operate properly.	⇨	To Section 13.3.5 "Flow chart used when output load of output module does not turn on"
Input signal cannot be fetched.	⇨	To Section 13.3.6 "Flow chart used when input cannot be fetched from the input module"
Special function module does not operate properly.	⇨	To Section 13.3.7 "Flow chart used when special function module does not operate properly"
Program cannot be written.	⇨	To Section 13.3.8 "Flow chart used when program cannot be written"

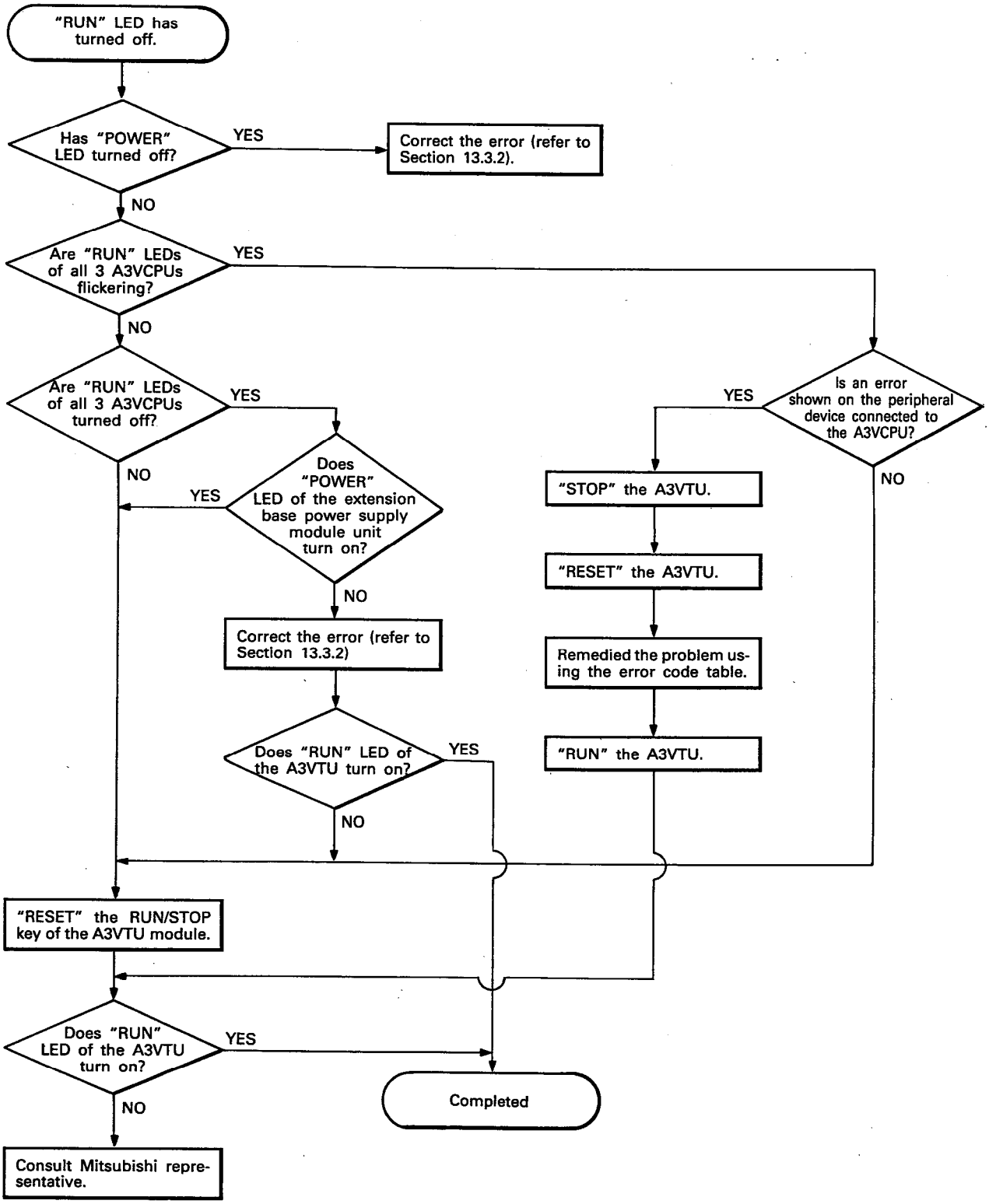
13.3.2 Flow chart used when "POWER" LED has turned off



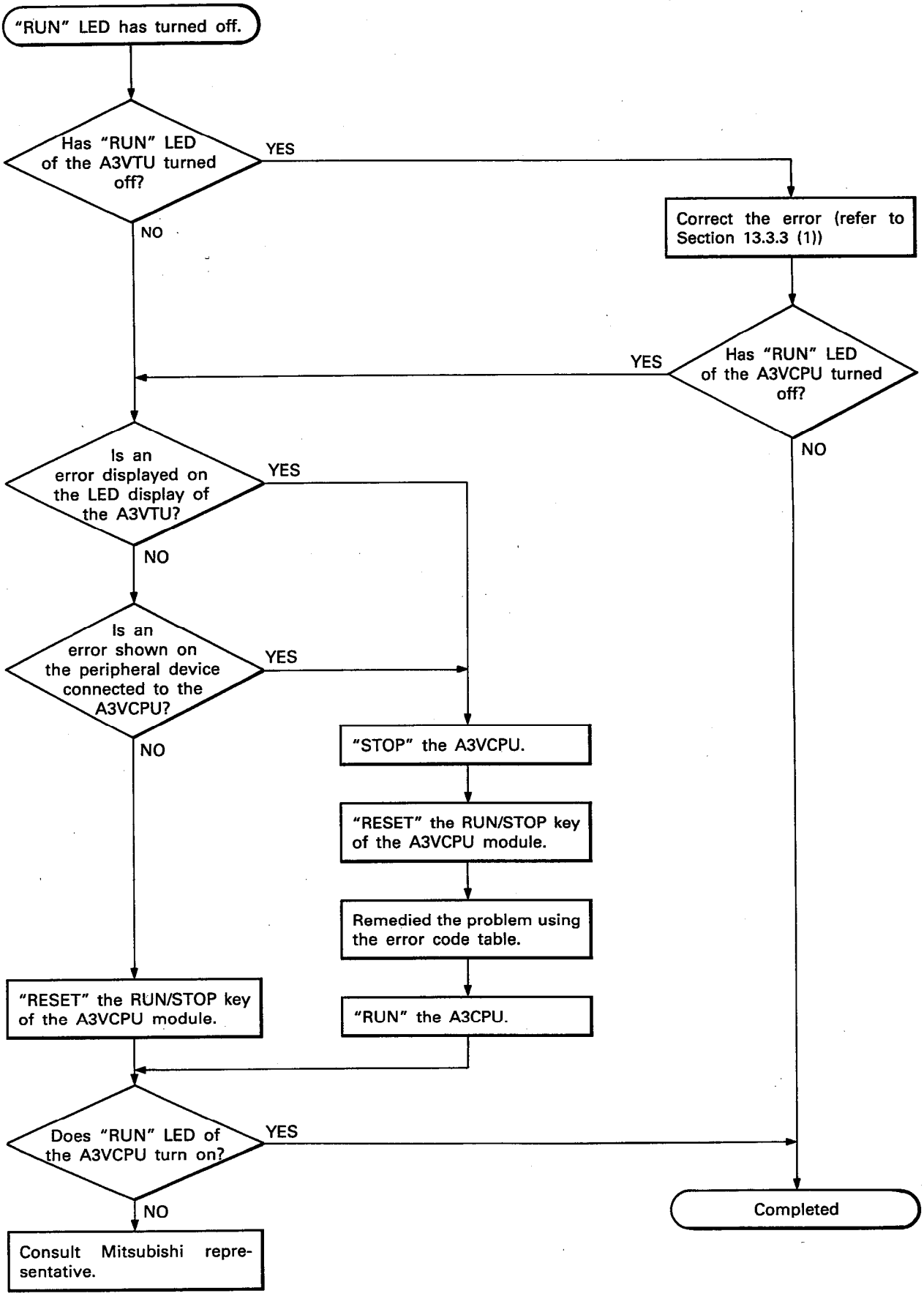
13.3.3 Flow chart used when "RUN" LED has turned off

"RUN" LEDs are provided on the A3VTU and A3VCPU. Flow charts are provided for both.

(1) Flow chart used when "RUN" LED has turned off on the A3VTU.

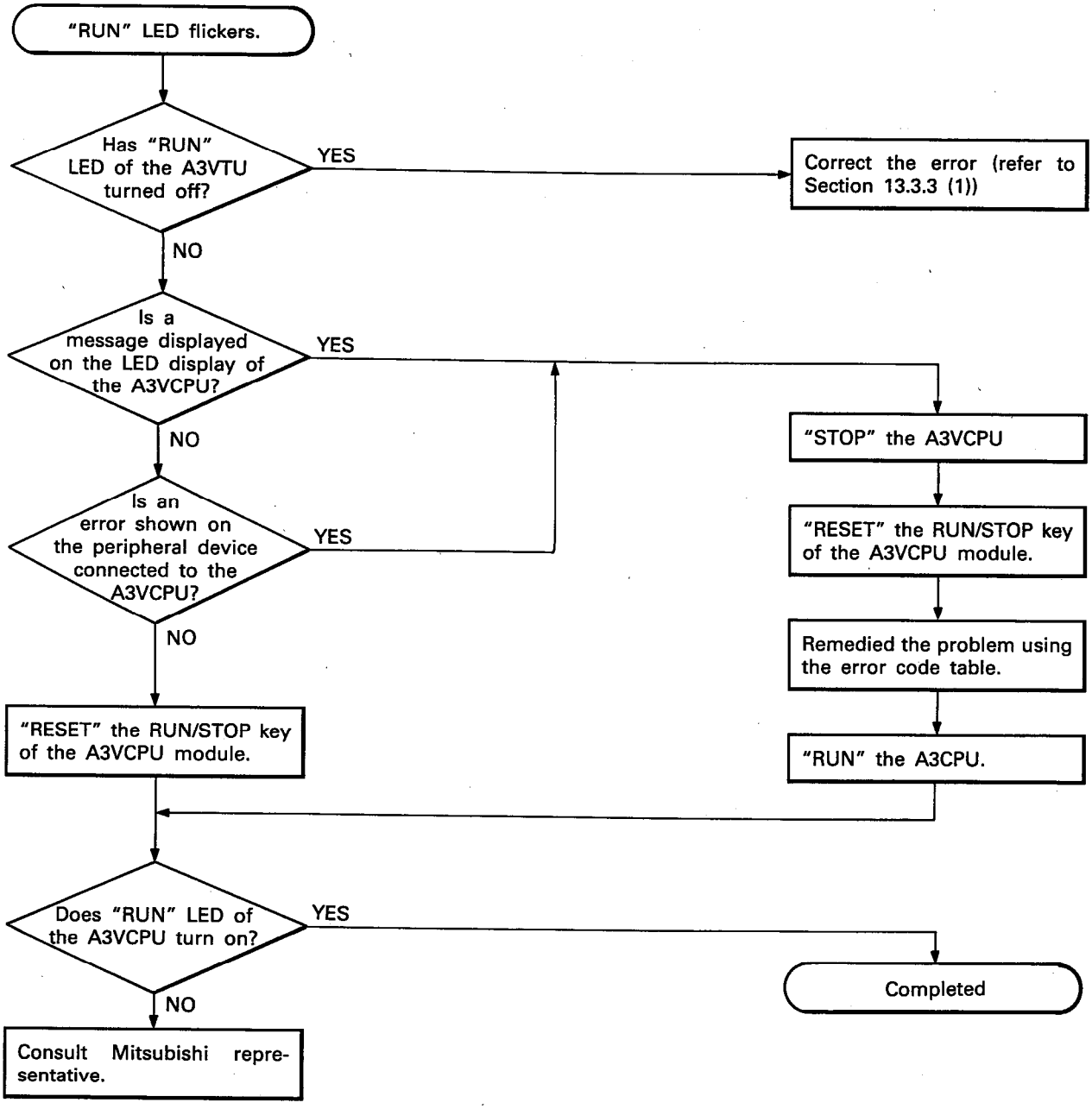


(2) Flow chart used when "RUN" LED has turned off on the A3VCPU.

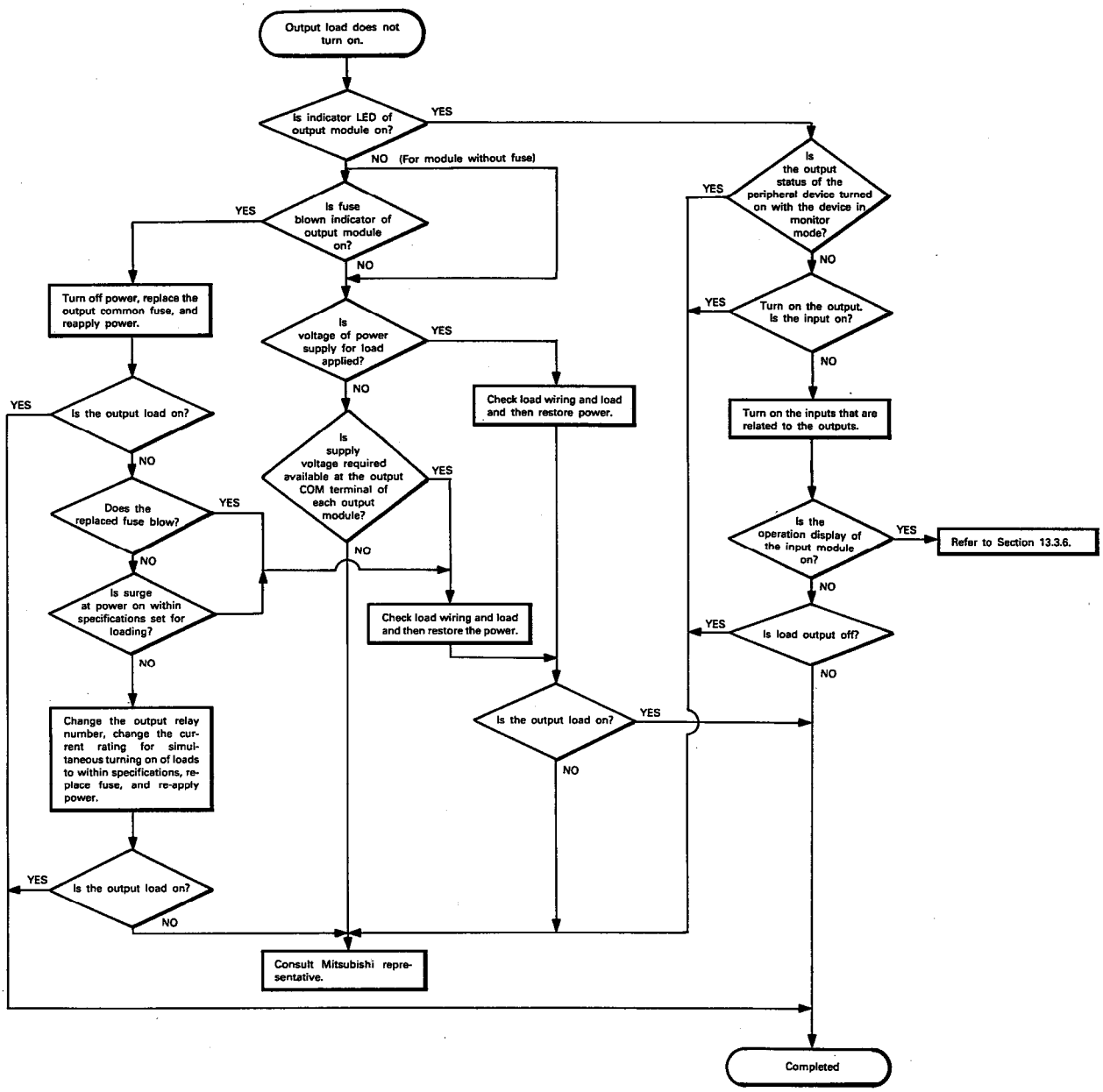


13.3.4 Flow chart used when "RUN" LED flickers

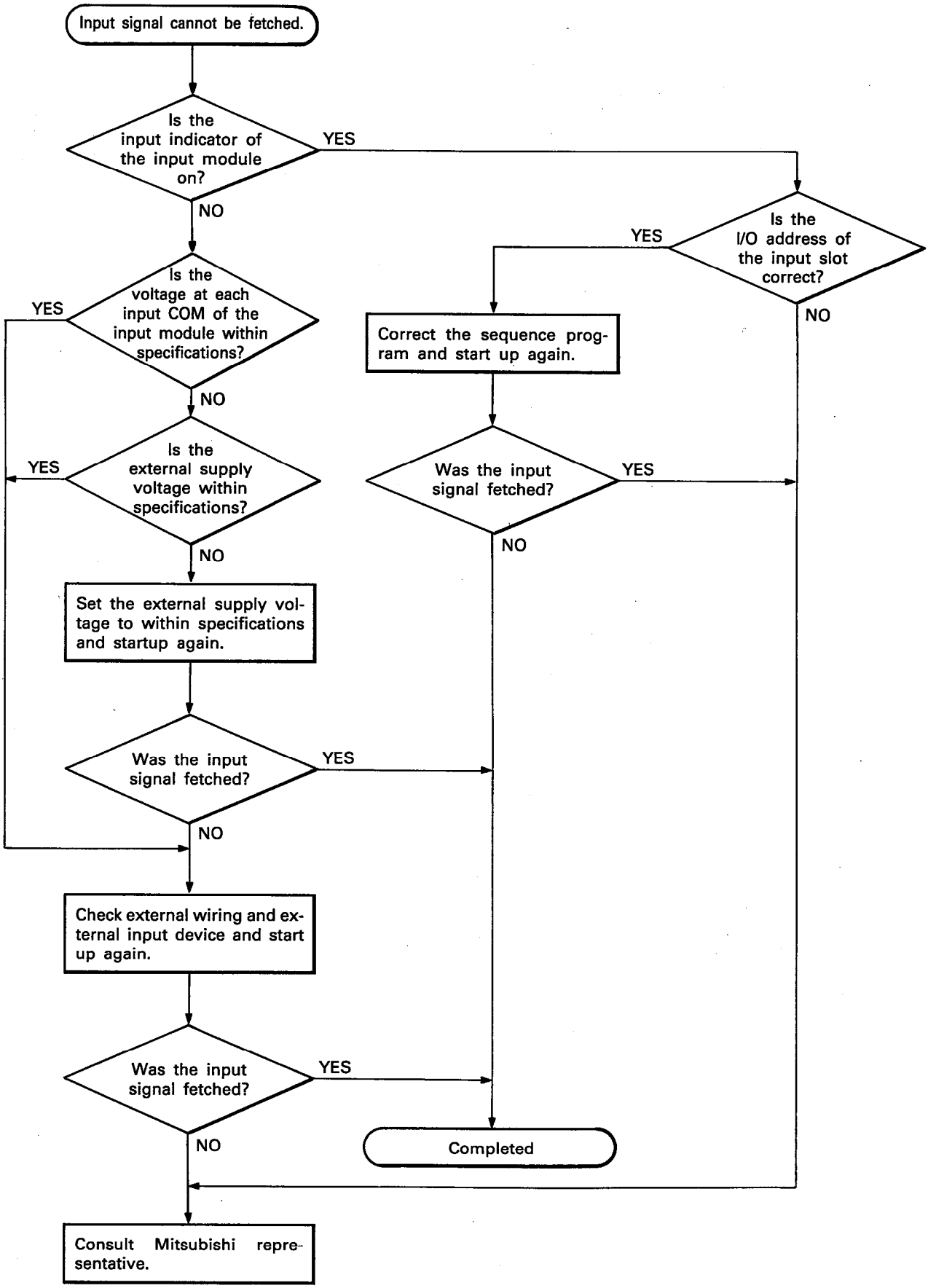
(1) Flow chart used when "RUN" LED of the A3VCPU flickers



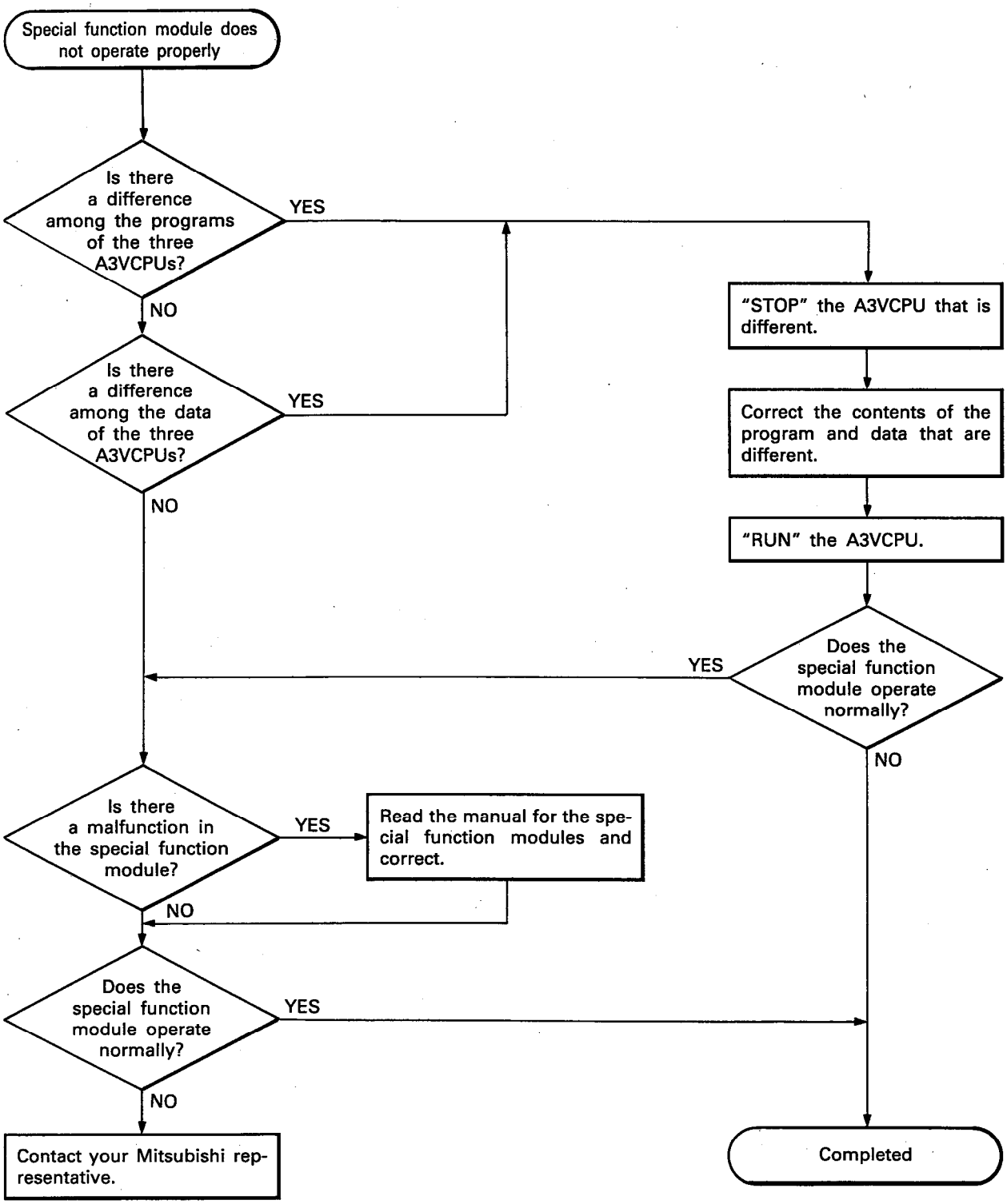
13.3.5 Flow chart used when output load of output module does not turn on



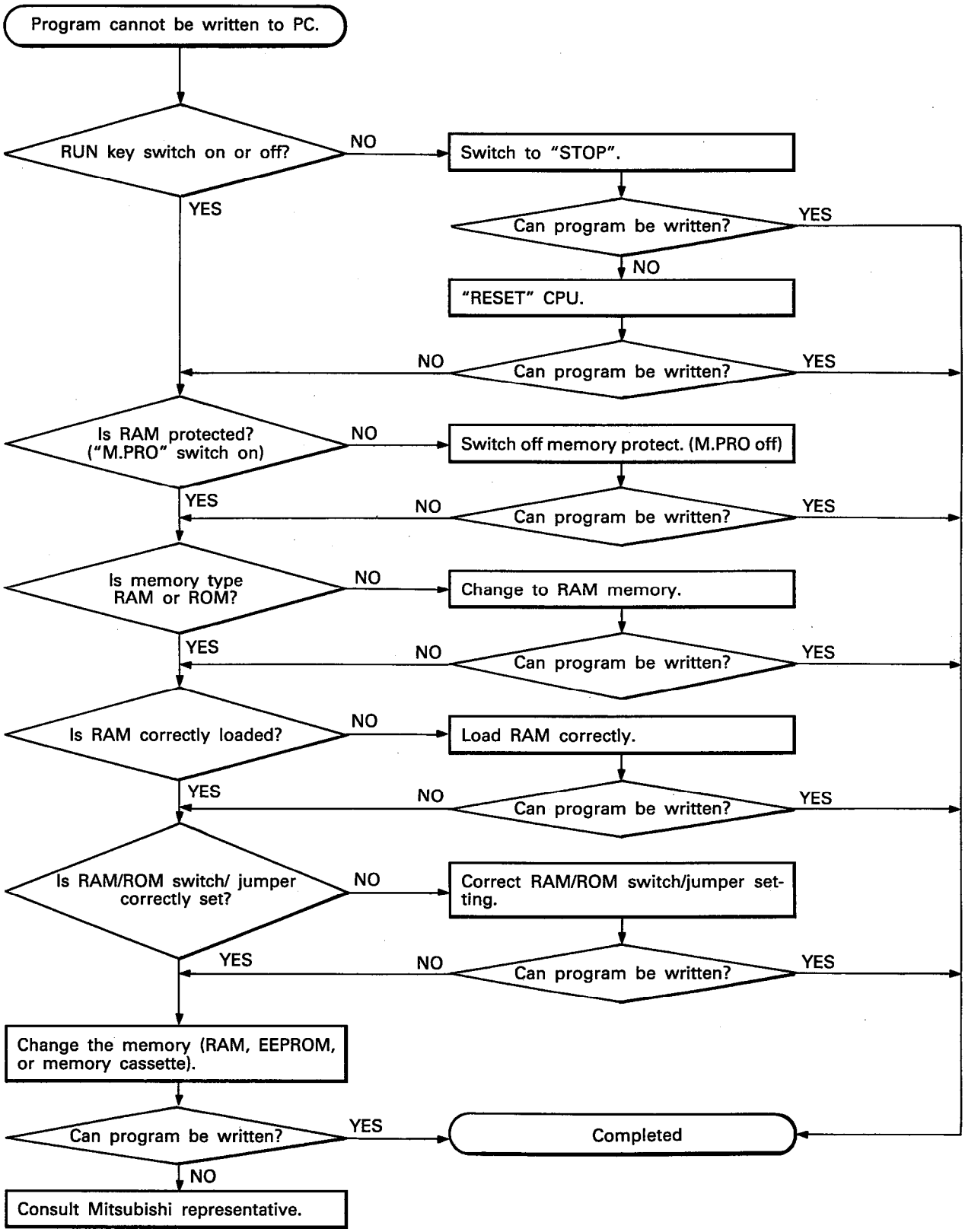
13.3.6 Flow chart used when input cannot be fetched from the input module



13.3.7 Flow chart used when special function module does not operate properly



13.3.8 Malfunction in program down load to PC



13.4 I/O Connection Troubleshooting

13.4.1 Input wiring troubleshooting

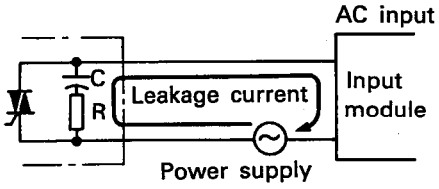
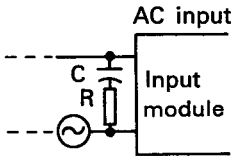
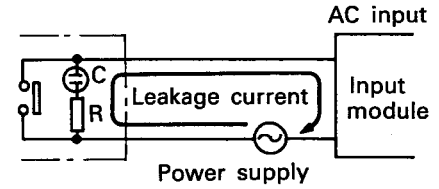
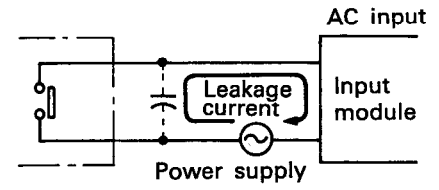
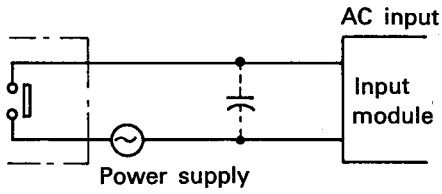
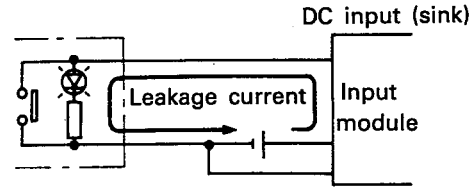
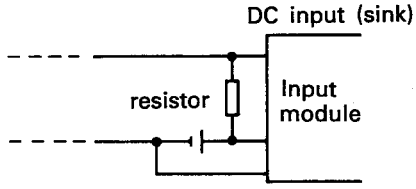
	Condition	Cause	Corrective Action
Example 1	Input signal does not turn off.	● Leakage current of input switch (such as drive by non-contact switch). 	● Connect an appropriate register which will make the voltage across terminals of input module lower than OFF voltage value.  It is recommended to use 0.1 to 0.47 μF + 47 to 120Ω (1/2W) for the constant of CR.
Example 2	Input signal does not turn off.	● Drive by a limit switch with neon lamp. 	● Same as Example 1. ● Or make up another independent display circuit.
Example 3	Input signal does not turn off.	● Leakage current due to line capacity of wiring cable. Line capacity C of twisted pair wire is approx. 100 PF/m(39.37inch). 	● Same as Example 1. ● However, leakage current is not generated when power supply is located on the input equipment side as shown below. 
Example 4	Input signal does not turn off.	● Drive by switch with LED indicator. 	● Connect a resistor which will make the voltage across input unit terminal and-common higher than OFF voltage, as shown below.  *The calculation example of connected resistor value is shown in the following page.

Table 13.3 Input Circuit Troubles and Corrective Actions (Continue)

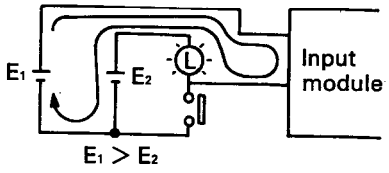
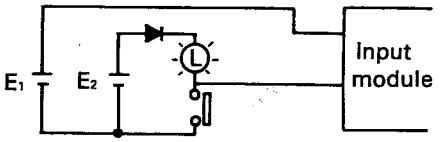
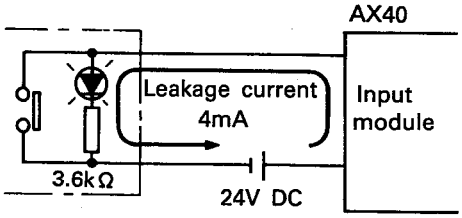
	Condition	Cause	Corrective Action
Example 5	Input signal does not turn off.	● Sneak path due to the use of two power supplies. 	● Use only one power supply. ● Connect a sneak path prevention diode. (Figure below) 

Table 13.3 Input Circuit Troubles and Corrective Actions

Calculation example for Example 4

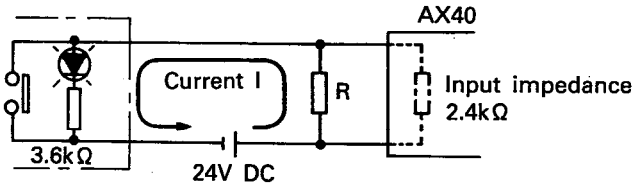


The switch with LED indicator is connected to AX40 and there is 4mA leakage current.

- The voltage V_{TB} across terminal and common is obtained by the following expression:

$V_{TB} = 4\ [mA] \times 2.4\ [k\Omega] = 9.6\ [V]$ (The voltage drop of LED is ignored.)

Since this voltage does not satisfy the OFF voltage of 6 [V] or lower, the input signal does not turn off. Therefor, connect a resistor as show below.



- Calculate the resistor value, R, as shown below:
  For an input voltage < 6V, current I must be:

$(24 - 6\ [V]\ ) \div 3.6\ [k\Omega] = 5mA$

Resistor R must be selected to give a current I > 5mA.

- Hence, for resistor, R

  $6\ [V] \div R > 5 - 2.5\ [mA]$
  $6\ [V] \div 2.5\ [mA] > R$
  $2.4\ [k\Omega] > R$

  For $R = 2k\Omega$, the power capacity must be:

  $W = (\text{applied voltage})^2 / R$ (or $W = (\text{maximum current})^2 \times R$)

  Resistor R terminal voltage is:

  $$\frac{2.4 \times 2}{2.4 + 2}\ [k\Omega] : \frac{2.4 \times 2}{2.4 + 2} + 3.6\ [k\Omega] = X : 24\ [V]$$
  $X = 5.58\ [V]$

  Therefore, the power capacity W of resistor R is

  $W = (5.58\ [V]\ )^2 / 2\ [k\Omega] = 0.015\ [W]$

- Use a safety factor of 3 to 5. Resistor should therefore be rated at 0.5 to 1W.

  A 2kΩ, 0.5 to 1W resistor should therefor be connected across the relevant input terminal and its COM.

13.4.2 Output circuit problems and corrective action

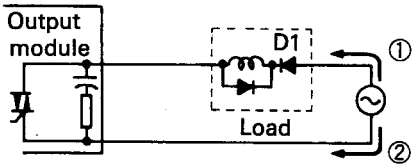
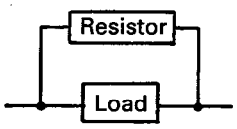
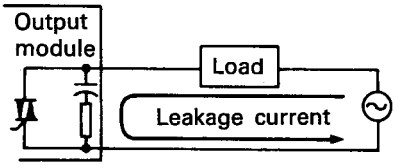
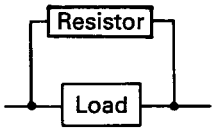
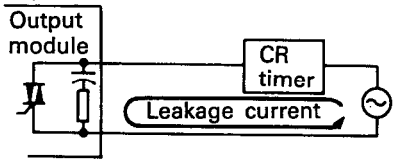
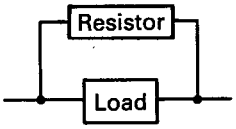
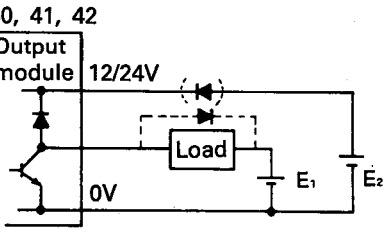
	Condition	Cause	Corrective Action
Example 1	When output in off, excessive voltage is applied to load.	● Load is half-wave rectified inside (seen in some solenoids). AY22, AY23  ● When the polarity of power supply is as shown by ①, C is charged. When the polarity is as shown by ②, voltage charged in C plus line voltage are applied across D1. Max. voltage in approx . 2.2E.	● Connect a resistor of several ten kΩ to several hundred kΩ across the load. It a resistor is used in this way, it dose not pose problem to output element but may sometimes cause the diode, which is built in the load, to deteriorate, resulting in burning etc. 
Example 2	Load does not turn off. (Triac output)	● Leakage current due to built-in noise suppression AY22, AY23 	● Connect C and R across the load. When wiring distance from output card to load is long, there may be a leakage current due to the line capacity.  It is recommended to use 0.1 to 0.47 μF + 47 to 120Ω (1/2W) for the constant of CR.
Example 3	When load is C-R type timer, time constant fluctuates. (Triac output)	AY22, AY23 	● After driving the relay, drive the C-R type timer by the same contact. Some timers have half-wave rectified internal circuits. Therefor, take precautions as indicated in example.  Calculate the CR constant depending on the load.
Example 4	Load does not turn off. (For direct current)	● Sneak path due to the use of two power supplies. AY40, 41, 42  ● When E1 < E2, snake path occurs.	● Reduce the power supplies from two to one. ● Connect a sneak path prevention diode. When the load is a relay or similar device, it is necessary to connect reverse-voltage absorbing diode to the load. (Shown by the dotted line in the figure at left)

Table 13.4 Output Circuit Failures and Corrective Actions

APPENDICES

APPENDIX 1 Table of Characteristics for the A3VTS, A3HCPU, A3NCPU, and A3CPU

The following table provides a list of characteristics for the A3VTS, A3HCPU, A3NCPU, and A3CPU. Detailed information concerning precautions and the differences related to the use of these CPUs in the A3VTS system is provided in Appendices 2 to 4.

1.1 Characteristics

Item \ Type		A3VTS	A3HCPU	A3NCPU	A3CPU
Control method		Storedome program, repetitive operation	Storedome program, repetitive operation		
I/O control method		Refresh method	Refresh method		Direct method
Program language		Special language for sequence control Relay symbol type, logic symbol type	Special language for sequence control Relay symbol type, logic symbol type		
Compatible with MELSAP language		Yes	No	Yes	
Number of instructions	Sequence instructions	22 types	22 types		
	Basic instructions	128 types	132 types		
	Application instructions	105 types	107 types	109 types	107 types
Processing speed (sequence instructions) (μ sec step)			Direct time: 0.2 to 2 Refresh time: 0.2 to 0.4	Direct time: 1.0 to 2.3 Refresh time: 1.0	1.25 to 2.25
I/O points		2048 types	2048 points		
Constant scan function (Set period of program execution)		Can be set in units of 10ms within a range of 10 to 1990ms.	Can be set in units of 10ms within a range of 10 to 1990ms.	Can be set in units of 10ms within a range of 10 to 1990ms.	None
Congested operation monitor timer (WDT)		Can be set in units of 10ms within a range of 0 to 2000ms.	Set at 200ms.	Can be set in units of 10ms within a range of 10 to 2000ms.	
Permissible momentary stop		Within 20ms.	Within 20ms.		
Current consumption (A)		A3VTU: 1 A3VCPU: 2.2	3.0	0.83	1.7
External dimensions mm (inch)		(250(9.84)×79.5(3.13)×121(4.76))×4 units	250(9.84)×79.5(3.13)×121(4.76)		
Weight kg (lb)		A3VTU: 0.78(1.72) A3VCPU: 0.84(1.85)	0.9(1.98)	0.8(1.76)	0.8(1.76)
Memory capacity		Maximum of 144K bytes	Maximum of 448K bytes	Maximum of 320K bytes	
Program capacity	Main sequence program	Maximum of 30K steps	Maximum of 30K steps		
	Sub-sequence program	Maximum of 30K steps	Maximum of 30K steps		
	Micro-computer program	Maximum of 58K bytes	Maximum of 58K bytes		
Internal relays (M)		1000 points (M0 to 999)	1000 points (M0 to 999)		
Latch relays (L)		1024 points (L1000 to 2047)	1024 points (L1000 to 2047)		
Step relays (S)		0 points (No initial status)	0 points (No initial status)		
		Total of 2048 points including M, L, S. (Set by parameters)	Total of 2048 points including M, L, S. (Set by parameters)		
Link relays (B)		1024 points (B0 to 3FF)	1024 points (B0 to 3FF)		
Timer (T)	Points	256 points	256 points		
	Specifications	100 ms timer: set period 0.1 to 3276.7 sec (t0 to 199) 10 ms timer: set period 0.01 to 327.67 sec (t200 to 255) 100 ms accumulating timer: set period 0.1 to 3276.7 sec (t0 to 199)	(Set by parameters)		
Counter (C)	Points	256 points	256 points		
	Specifications	Normal counter: set range 1 to 32767 (C0 to 255) Interrupt counter: None	Normal counter: set range 1 to 32767 (C0 to 255) Interrupt counter: set range 1 to 32767 (C224 to C255 can be set) Interrupt cycle counter	Normal counter: set range 1 to 32767 (C0 to 255) Interrupt counter: set range 1 to 32767 (C224 to C255 can be set) Counter used within the interrupt program.	
Data register (D)		1024 points (D0 to 1023)	1024 points (D0 to 1023)		
Link register (W)		1024 points (W0 to 3FF)	1024 points (W0 to 3FF)		
Annunciator (F)		256 points (F0 to 255)	256 points (F0 to 255)		
File register (R)		Maximum 8192 points (R0 to 8191)	Maximum 8192 points (R0 to 8191)		
Accumulator (A)		2 points (A0 to A1)	2 points (A0 to A1)		
Index register (V, Z)		2 points (V, Z)	2 points (V, Z)		

Table 1.1 Table of Characteristics (Continue)

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Item \ Type	A3VTS	A3HCPU	A3NCPU	A3CPU
Pointer (P)	256 points (P0 to 255)	256 points (P0 to 255)		
Interrupt pointer (I)	None	32 points (I0 to 31)		
Special function relay (M)	256 points (M9000 to 9255)	256 points (M9000 to 9255)		
Special register (D)	256 points (D9000 to 9255)	256 points (D9000 to 9255)		
Comment points	Maximum of 4032 points	Maximum of 4032 points		
Status latch function	Yes	Available		
Sampling trace function	Yes	Available		
Off line switch function	Yes (Y, M, L, B, F)	None	Yes (Y, M, L, B, F)	
Annunciator display function	F number display	F number display		
Remote RUN/PAUSE contact setting	Available	Available		
Operation mode switching when error occurs	Available	Available		
Output mode switching when STOP → RUN	Available	Available		
Keyword recording	Available	Available		
Print title recording	Available	Available		
Assignment change of I/O points	Available via GPP, PHP, HGP	Available via GPP, PHP, HGP		
Latch (held during power loss) range setting	B0 to 3FF, T0 to 255, C0 to 255, D0 to 1023, W0 to 3FF Latch range setting available			
Step operation	None	Step operation available in terms of break point stops and a stop at each instruction		
Clock	None	None	Year, month, hour, minute, second, day register can be written to and read from.	None

Table 1.1 Table of Characteristics

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APPENDIX 2 Precautions concerning the use of an A3VTS in system already using an A3CPU

When converting a system that is already configured with an A3CPU to the A3VTS system, certain precautions must be taken concerning hardware and the sequence program. This section describes these precautions.

2.1 Differences in instruction set between A3CPU and A3VTS

Instructions for the A3VTS (A3VCPU) and A3CPU other than those shown below are the same. For information concerning instructions not shown below, refer to the A3CPU Programming Manual.

Instruction	Description
SEG CHG	The contents of the instruction shown on the left vary between the A3VTS and A3CPU. For details see Appendix 2.4.3.
COM DI EI IRET RFRP RTOP	The instructions shown on the left cannot be used with the A3VTS. However, their inclusion in a program does not lead to error generation as they are ignored.

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2.2 Differences in special relays and special registers between A3CPU and A3VTS

The special relays and special registers of the A3VTS (A3VCPU) and A3CPU other than those shown below are the same. For information concerning the contents of the special relays and special registers, refer to the appropriate CPU User's Manual.

Device	Device No.	Name of Device No.	Description
Special relays	M9030 to M9034	Timing clock 0.1sec, 0.2sec, 1sec, 2sec, and 1 minute clock	The special relays listed on the left cannot be used. However, their inclusion in a program does not lead to error generation as they are ignored.
	M9050	Signal flow communication contact	
	M9018	Data link monitor switch	The special relays listed on the left are relays that have been added to the A3VTS. For detail information see Appendix 8 "Special Relay Table"
	M9091	Microcomputer sub-routine call error flag	
	M9092	Dual power supply module overheat error	
	M9093	Dual power supply module malfunction	
	M9096	A3VCPU(A) self-diagnosis error	
	M9097	A3VCPU(B) self-diagnosis error	
	M9098	A3VCPU(C) self-diagnosis error	
	M9099	A3VTU self-diagnosis error	
Special registers	D9006	Low battery	The special registers listed on the left are registers that have been added to the A3VTS. For detail information see Appendix 8 "Special Registers Table"
	D9020	Constant scan time	
	D9072	PC communication check	
	D9090	Microcomputer subroutine INPUT data area head device No.	
	D9091	Error code generated for microcomputer sub-routine call	
	D9094	Communication I/O number	
	D9095	Operation display for CPU section	
	D9096	Self-diagnosis error code for A3VCPU (A)	
	D9097	Self-diagnosis error code for A3VCPU (B)	
	D9098	Self-diagnosis error code for A3VCPU (C)	
	D9099	Self-diagnosis error code for A3VTU	

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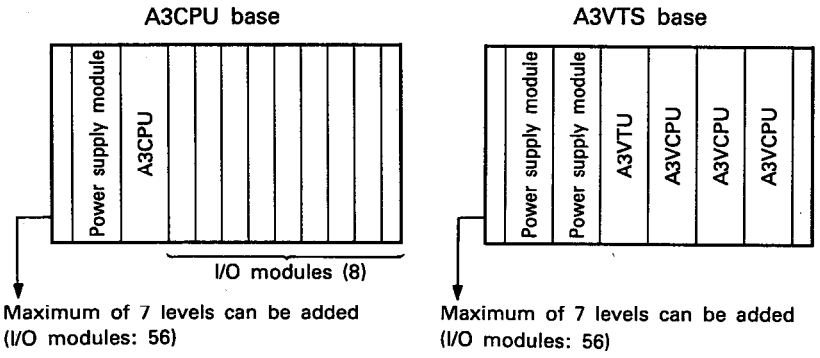
2.3 Cautions concerning module replacement

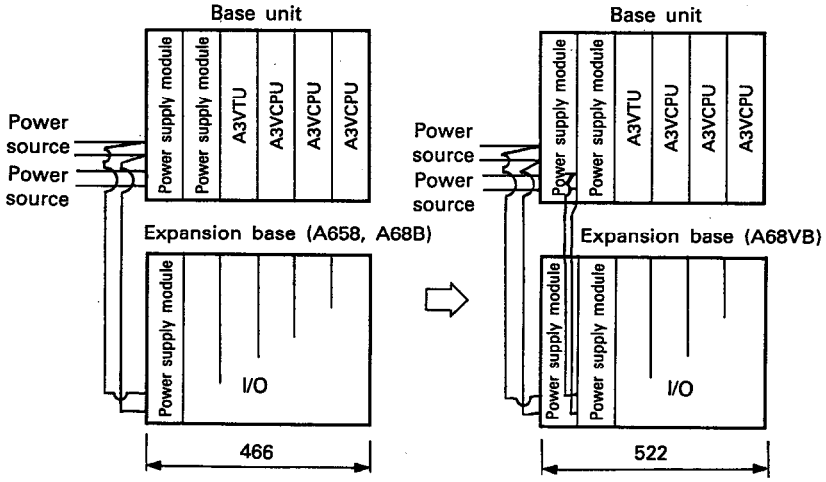
(1) When the A3CPU system is to be changed to the A3VTS system, the I/O modules cannot be installed in the base unit of the A3VTS system. This means that the maximum number of I/O modules that can be installed is limited to 56, 8 less than what would otherwise be possible.
If a full number of 64 slots is to be used for the I/O modules, change I/O module with more I/O points so that the total number of slots to be used is within 56.



(2) Some special function modules cannot be used in the A3VTS system. The special function modules listed below that were used in the existing systems cannot be used and must be removed.

AD57 (S1), AD58, AI61,AD51E (may be used under certain conditions), AJ71C24 (S3)

(3) When the system is changed to the A3VTS system, the base unit contains a dual power supply to supply the power in two systems, thus improving reliability in supplying power including power supply modules. However, since the power supply module installed in the expansion base unit is not duplexed, a malfunction in the power supply, including the power supply module could stop the system operation.
By changing the expansion base to the one for dual power supply modules, increased operation ratio and reliability can be attained. However, external dimensions will increase in size when such is done.



(4) Expansion base unit (A55B, A58B), in which the power supply module cannot be installed, cannot be used in the A3VTS system. If this is used in the existing system, change to an expansion unit in which the power supply modules can be installed.

2.4 Cautions concerning the use of sequence programs

Sequence programs created with the A3CPU can be used in the A3VTS system in principle. However, note that differences exist as shown below.

(1) Differences in I/O control methods

(2) Pulse processing program using the [SET] / [RST] instructions

(3) Instructions, special relays, and special registers

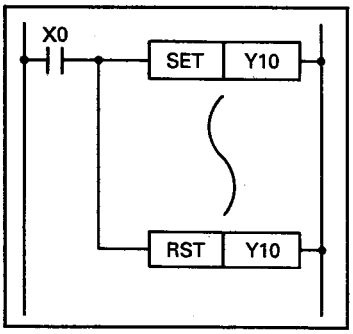
2.4.1 Differences in I/O control methods

The A3CPU uses direct control for input (X) and output (Y) while the A3VTS uses refresh control.
Care must be taken as the timing used for both methods vary. If there is a problem, use the segment I/O refresh instruction ([SEG] instruction) and write the program so that it takes a form as close to the direct method as possible in the required area.
Refer to Section 4.3 for detailed information concerning refresh control.

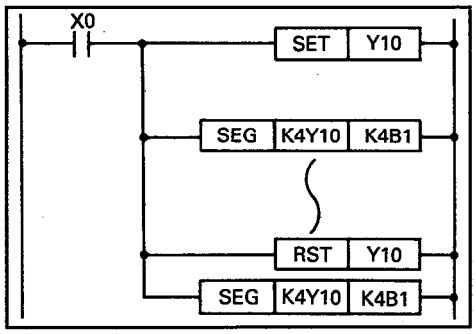
2.4.2 Pulse processing program using the [SET] / [RST] instructions

When using the [SET] / [RST] instructions to output a pulse signal to an external device when using refresh control for A3CPU output (Y), the segment I/O refresh instruction should be used in the manner shown in the following diagram.

A3CPU (Direct control)



A3VTS (Refresh control)



POINT

When using the AD61(S1) high-speed counter module, it is necessary to output a pulse signal specifically for the AD61.

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2.4.3 Instructions, special relays, and special registers

(1) Instructions

The instructions shown below either vary with those of the A3CPU or cannot be used in the A3VTS. Care must be exercised when they have been used in a present program. For detailed information concerning the instructions, see Appendix 5 and the A3CPU Programming Manual.

(a) SEG instruction

The specifications are different as follows:

	A3VTS	A3CPU
Instruction function	Refresh instruction for the segment I/O.	7 segment decode instruction.

(b) CHG instruction

The specifications are different as follows:

	A3VTS	A3CPU
Instruction function	The contents of the CHG instruction do not change during execution because the A3VTS does not have M9050.	The contents of the CHG instruction changes during execution because M9050 is set ON/OFF.

For details, refer to explanations for CHG instruction given in the ACPU Programming Manual. Contents of A3VTS are the same as those of A3CPU.

(c) COM, EI, DI, IRET, RFRP, and RTOP instructions

The COM, EI, DI, IRET, RFRP, and RTOP instructions are not used in the A3VTS. However, inclusion of these instructions in the program will not result in error generation.
(If the IRET is included in the main routine program, an error will be generated.)
Correct the program as necessary.

(2) Special relays and Special registers

Some of the special relays cannot be used and some are newly added.
Some special registers are newly added.
See Appendix 2.2 for information concerning the device numbers. For detailed information concerning each of the special relays and special relays, refer to the CPU User's Manual.

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APPENDIX 3 Cautions Concerning the Use of an A3VTS in System Already Using an A3NCPU

When converting the system that is already configured with an A3NCPU to the A3VTS system, certain cautions must be taken concerning hardware and the sequence program. This section describes these cautions.

3.1 Differences in instruction set between A3NCPU and A3VTS

Instructions for the A3VTS (A3VCPU) and A3NCPU other than those shown below are the same. For information concerning instructions not shown below, refer to the A3CPU Programming Manual.

Instruction	Description
SEG CHG PR	The contents of the instruction shown on the left vary between the A3VTS and A3NCPU. For details see Appendix 2.4.3.
COM DI EI IRET RFRP RTOP	The instructions shown on the left cannot be used with the A3VTS. However, their inclusion in a program does not lead to error generation as they are ignored.

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3.2 Differences between the special relays and special registers of the A3NCPU and A3VTS

The special relays and special registers of the A3VTS (A3VCPU) and A3NCPU other than those shown below are the same. For information concerning the contents of the special relays and special registers, refer to the appropriate CPU User's Manual.

Device	Device No.	Name of Device No.	Description
Special relays	M9025	Clock data set request	The special relays listed on the left cannot be used. However, their inclusion in a program does not lead to error generation as they are ignored.
	M9026	Clock data error	
	M9027	Clock data display	
	M9028	Clock data read request	
	M9030 to M9034	Timing clock 0.1sec, 0.2sec, 1sec, 2sec, and 1 minute clock	
	M9052	SEG instruction switch	
	M9053	EI/DI instruction switch	
	M9084	Error check	
	M9094	I/O change flag	
	M9018	Data link monitor switch	The special relays listed on the left are relays that have been added to the A3VTS. For detail information see Appendix 8 "Special Relay Table"
	M9091	Microcomputer routine call error flag	
	M9092	Dual power supply module overheat error	
	M9093	Dual power supply module malfunction	
	M9096	A3VCPU(A) self-diagnosis error	
	M9097	A3VCPU(B) self-diagnosis error	
	M9098	A3VCPU(C) self-diagnosis error	
	M9099	A3VTU self-diagnosis error	
Special registers	D9014	Method of I/O control	The special relays listed on the left cannot be used in the A3VTS. However, their inclusion in a program does not lead to error generation as they are ignored.
	D9025 to D9028	Clock data (year, month, day, hour, minute, second)	
	D9006	Low battery	The special relays listed on the left are relays that have been added to the A3VTS. For detail information see Appendix 8 "Special Relay Table"
	D9072	PC communication check	
	D9090	Microcomputer sub-routine INPUT data area head device No.	
	D9091	Error code generated for microcomputer sub-routine call	
	D9094	Communication I/O number	
	D9095	Operation display for CPU section	
	D9096	Self-diagnosis error code for A3VCPU (A)	
	D9097	Self-diagnosis error code for A3VCPU (B)	
	D9098	Self-diagnosis error code for A3VCPU (C)	
	D9099	Self-diagnosis error code for A3VTU	

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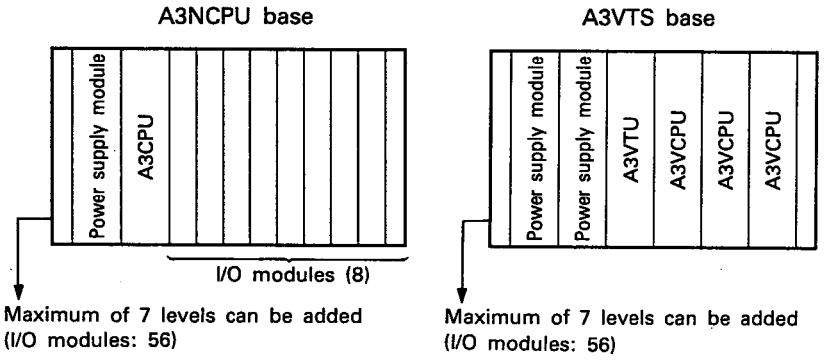
3.3 Cautions concerning module replacement

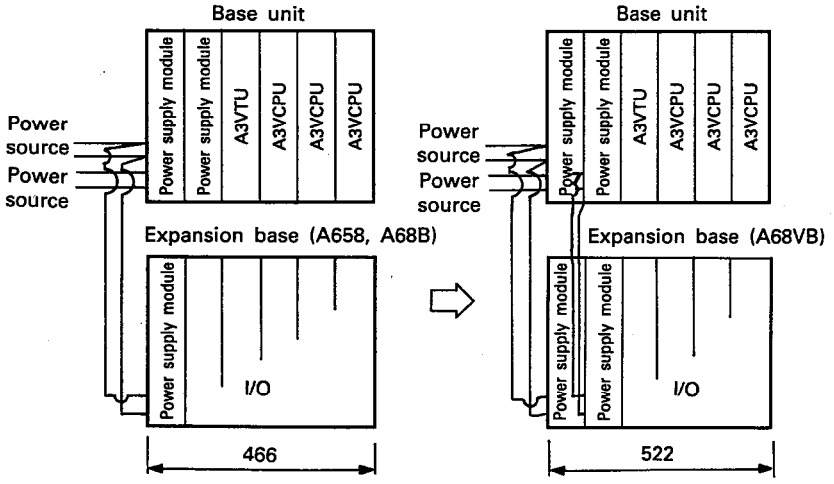
(1) When the A3NCPU system is to be changed to the A3VTS system, the I/O modules cannot be installed in the base unit of the A3VTS system. This means that the maximum number of I/O modules that can be installed is limited to 56, 8 less than what would otherwise be possible.
If a full number of 64 slots is to be used for the I/O modules, change I/O module with more I/O points so that the total number of slots to be used is within 56.



(2) Some special function modules cannot be used in the A3VTS system. The special function modules listed below that were used in the existing systems cannot be used and must be removed.

AD57 (S1), AD58, AI61, AJ71C23, AD51E (may be used under certain conditions), AJ71C24 (S3)

(3) When the system is changed to the A3VTS system, the base unit contains a dual power supply to supply the power in two systems, thus improving reliability in supplying power including power supply modules. However, since the power supply module installed in the expansion base unit is not duplexed, a malfunction in the power supply, including the power supply module could stop the system operation.
By changing the expansion base to the one for dual power supply modules, increased operation ratio and reliability can be attained. However, external dimensions will increase in size when such is done.



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(4) Expansion base unit (A55B, A58B), in which the power supply module cannot be installed, cannot be used in the A3VTS system. If this is used in the existing system, change to an expansion unit in which the power supply modules can be installed.

3.4 Cautions concerning the use of sequence programs

Sequence programs created with the A3NCPU can be used in the A3VTS system in principle. However, note that differences exist as shown below.

(1) Differences in I/O control methods

(2) Pulse processing program using the [SET] / [RST] instructions

(3) Data link processing

(4) Instructions, special relays, and special registers

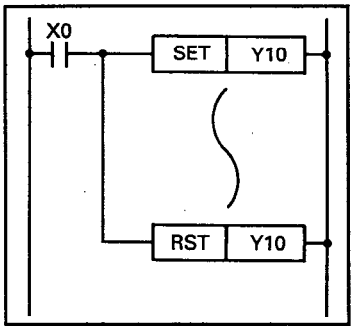
3.4.1 Differences in I/O control methods

The A3NCPU can switch between direct and refresh control for input (X) and output (Y).
No problem should occur when refresh control is used for both input and output. However, care must be taken when using direct control since the A3VTS uses refresh control and differences between input (X) fetch timing and output timing of output (Y) to external devices may differ.
If there is a problem, use the segment I/O refresh instruction ([SEG] instruction) and write the program so that it takes a form as close to the direct method as possible in the required area.
Refer to Section 4.3 for detailed information concerning refresh control.

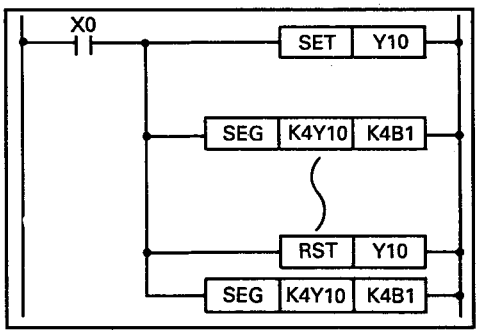
3.4.2 Pulse processing program with the [SET] / [RST] instruction

When using the [SET] / [RST] instructions to output a pulse signal to an external device when using refresh control for A3NCPU output (Y), the segment I/O refresh instruction should be used in the manner shown in the following diagram.

A3NCPU (Direct control)



A3VTS (Refresh control)



POINT

When using the AD61(S1) high-speed counter module, it is necessary to output a pulse signal specifically for the AD61.

3.4.3 Data link processing

The A3NCPU can change the timing for link refresh using the [EI] / [DI] instruction by using the sequence program to set the special relay M9053 ON. However, the A3VTS is not provided with this function and cannot use the [EI] / [DI] instruction. Link refresh is automatically set by the timing of the link scan as designated by the master station.

For details, refer to the A3VTS Data Link User's Manual.

3.4.4 Instructions, special relays, and special registers

(1) Instructions

The instructions shown below either vary with those of the A3NCPU or cannot be used in the A3VTS. Care must be exercised when they have been used in a present program. For detailed information concerning the instructions, see Appendix 5 and the A3CPU Programming Manual.

(a) [SEG] instruction

The specifications are different as follows:

	A3VTS	A3NCPU
Instruction function	Refresh instruction for the segment I/O.	When M9052 is OFF 7 segment decode instruction. When M9052 is ON Refresh instruction for the segment I/O.

(b) [CHK] instruction

The specifications are different as follows:

	A3VTS	A3NCPU
Instruction function	Becomes a malfunction check instruction for special formats	When the I/O control for both inputs and outputs is set to direct control, the instruction becomes a malfunction check for special formats. When the I/O control for either one or both of the inputs and outputs is set to refresh control, the instruction inverts the outputs of the designated bit device when executed.

(c) [PR] instruction

The specifications are different as follows:

	A3VTS	A3NCPU
Instruction function	Outputs 16 characters of ASCII code.	When M9049 is OFF The instruction outputs until the NULL code (00_H) is reached. When M9049 is ON The instruction outputs 16 characters of ASCII code.

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(d) [COM], [EI], [DI], [IRET], [RFRP], and [RTOP] instructions

The [COM], [EI], [DI], [IRET], [RFRP], and [RTOP] instructions are not used in the A3VTS. However, inclusion of these instructions in the program will not result in error generation.
(If the [IRET] is included in the main routine program, an error will be generated.)
Correct the program as necessary

(2) Special relays and Special registers

Some of the special relays and special registers cannot be used and some are newly added.
See Appendix 3.2 for information concerning the device numbers. For detailed information concerning each of the special relays and special registers, refer to the CPU User's Manual.

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APPENDIX 4 Cautions Concerning the Use of an A3VTS in System Already Using an A3HCPU

4.1 Differences in instruction set between A3HCPU and A3VTS

Instructions for the A3VTS (A3VCPU) and A3HCPU other than those shown below are the same. For information concerning instructions not shown below, refer to the A3CPU Programming Manual.

Instruction	Description
SEG PR CHG	The contents of the instruction shown on the left vary between the A3VTS and A3HCPU. For details see Appendix 4.4.3.
COM EI DI IRET RFRP RTOP	The instructions shown on the left cannot be used with the A3VTS. However, their inclusion in a program does not lead to error generation as they are ignored.

4.2 Differences in special relays and special registers between A3HCPU and A3VTS

The special relays and special registers of the A3VTS (A3VCPU) and A3HCPU other than those shown below are the same. For information concerning the contents of the special relays and special registers, refer to the appropriate CPU User's Manual.

Device	Device No.	Name of Device No.	Description
Special relays	M9030 to M9034	Timing clock 0.1sec, 0.2sec, 1sec, 2sec, and 1 minute clock	The special relays listed on the left cannot be used in the A3VTS. However, their inclusion in a program does not lead to error generation as they are ignored.
	M9052	SEG instruction switch	
	M9084	Error check	
	M9018	Data link monitor switch	The special relays listed on the left are relays that have been added to the A3VTS. For detail information see Appendix 8 "Special Relay Table"
	M9091	Microcomputer routine call error flag	
	M9092	Dual power supply module over-heat error	
	M9093	Dual power supply module mal-function	
	M9096	A3VCPU(A) self-diagnosis error	
	M9097	A3VCPU(B) self-diagnosis error	
	M9098	A3VCPU(C) self-diagnosis error	
	M9099	A3VTU self-diagnosis error	
Special registers	D9006	Low battery	The special relays listed on the left cannot be used in the A3VTS. For detail information see Appendix 8 "Special Relay Table"
	D9072	PC communication check	
	D9090	Microcomputer sub-routine INPUT data area head device No.	
	D9091	Error code generated for micro-computer sub-routine call	
	D9094	Communication I/O number	
	D9095	Operation display for CPU section	
	D9096	Self-diagnosis error code for A3VCPU (A)	
	D9097	Self-diagnosis error code for A3VCPU (B)	
	D9098	Self-diagnosis error code for A3VCPU (C)	
	D9099	Self-diagnosis error code for A3VTU	

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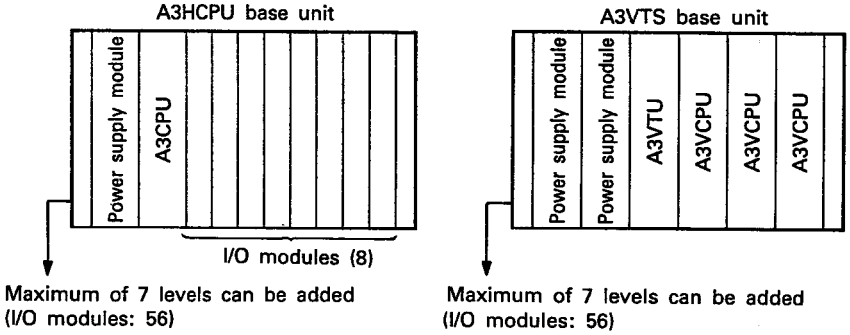
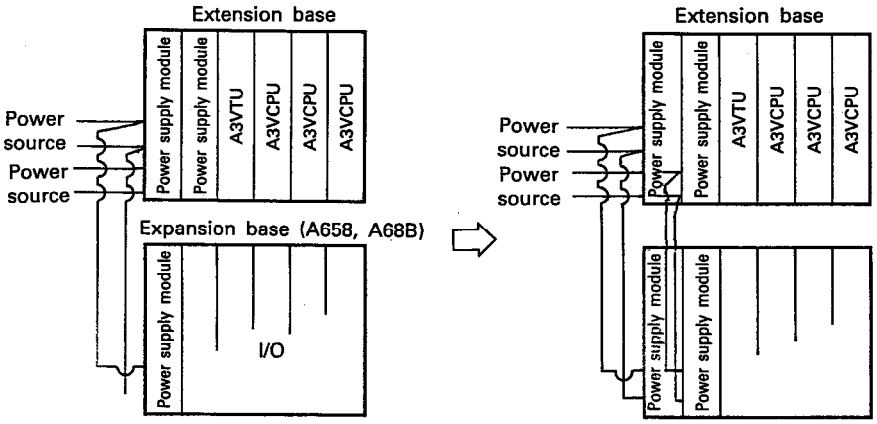
4.3 Cautions concerning module replacement

(1) When changing the A3HCPU system to the A3VTS system, the I/O modules cannot be installed in the base unit of the A3VTS system. This means that the maximum number of I/O modules that can be installed is limited to 56, 8 less than what would otherwise be possible.
If a full number of 64 slots is to be used for the I/O modules, change I/O modules with more I/O points so that the total number of slots to be used is within 56.



(2) Some special function modules cannot be used in the A3VTS system. The special function modules listed below that were used in the existing system cannot be used and must be removed.
AD57 (S1), AD58, AI61, AD51E (may be used under certain conditions), AJ71C24 (S3)

(3) When changing the system is changed to the A3VTS system, the base unit contains a dual power supply to supply the power in two systems, thus improving reliability in supplying power including power supply modules. However, since the power supply module installed in the extension base unit is not duplexed, a malfunction in the power supply, including the power supply module could stop the system operation.
By changing the extension base to the one for dual power supply modules, increased operating ratio and reliability can be attained. However, external dimensions will increase in size when such is done.



(4) Extension base unit (A55B, A58B), in which the power supply module cannot be installed, cannot be used in the A3VTS system. If this is used in the existing system, change to an extension unit in which the power supply modules can be installed.

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4.4 Cautions concerning the use of sequence programs

Sequence programs created with the A3HCPU can be used in the A3VTS system in principle. However, the time required for processing instructions will increase resulting in increased scan time as well. Also note that differences exist as shown below.

(1) Differences I/O control methods
(2) Pulse processing program using the [SET] / [RST] instructions
(3) Instructions, special relays, and special registers

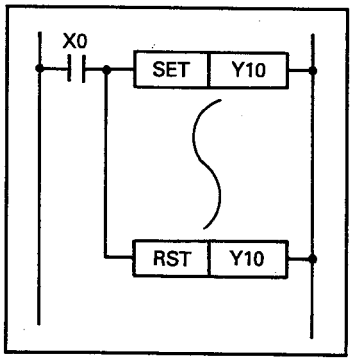
4.4.1 Differences in I/O control methods

The A3HCPU can switch between either direct or refresh control for input (X) and output (Y).
No problem should occur when refresh control is used for both input and output. However, care must be taken when using direct control since the A3VTS uses refresh control and differences between input (X) fetch timing and output timing of output (Y) to external modules may differ.
If there is a problem, use the segment I/O refresh instruction ([SEG] instruction) and write the program so that it takes a form as close to the direct method as possible in the required area.
Refer to Section 4.3 for detailed information concerning refresh control.

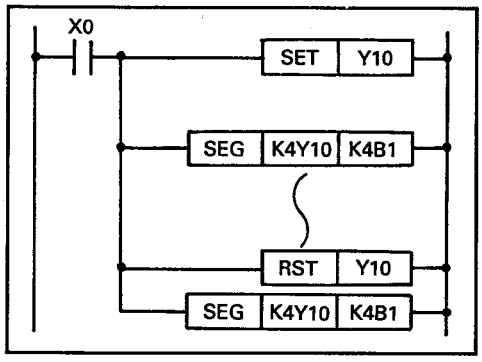
4.4.2 Pulse processing program using the [SET] / [RST] instructions

When using the [SET] / [RST] instructions to output a pulse signal to an external device when using refresh control for A3HCPU output (Y), the segment I/O refresh instruction should be used in the manner shown in the following diagram.

A3HCPU (Direct control)



A3VTS (Refresh control)



POINT

When using the AD61(S1) high-speed counter module, it is necessary to output a pulse signal specifically for the AD61.

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4.4.3 Instructions, special relays, and special registers

(1) Instructions

The instructions shown below either vary with those of the A3HCPU or cannot be used in the A3VTS. Care must be exercised when they have been used in a present program. For detailed information concerning the instructions, see Appendix 5 and the A3CPU Programming Manual.

(a) [SEG] instruction
The specifications are different as follows:

	A3VTS	A3HCPU
Instruction function	Refresh instruction for the segment I/O.	• When M9052 is OFF 7 segment decode instruction. • When M9052 is ON Refresh instruction for the segment I/O.

(b) [PR] instruction
The characteristics vary as shown below.

	A3VTS	A3HCPU
Instruction function	Outputs 16 characters of ASCII code.	The instruction outputs until the NUL code (00_H) is reached.

(c) [CHG] instruction
The specifications are different as follows:

	A3VTS	A3HCPU
Instruction function	The [CHG] instruction is executed only when the condition contacts are set from OFF to ON.	The [CHG] instruction is normally executed during the period in which the condition contracts of the [CHG] instruction are ON.

(d) [COM], [EI], [DI], [IRET], [RFRP], [RTOP] instructions
The COM, EI, DI, IRET, RFRP, and RTOP instructions are not used in the A3VTS. However, inclusion of these instructions in the program will not result in error generation. (If the [IRET] is included in the main routine program, an error will be generated.)
Correct the program as necessary.

(2) Special relays and Special registers
Some of the special relays cannot be used, however, their inclusion in a program will not result in error generation. Some special relays and special registers have been added. See Appendix 4.2 for information concerning the device numbers. For detailed information concerning each of the special relays and special relays, refer to the CPU User's Manual.

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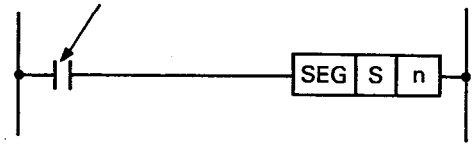
APPENDIX 5 SEG Instructions Used in the A3VTS

The SEG instruction as it is used in the A3VTS differs from when it is used in the A3HCPU, A3NCPU, and A3CPU.

SEG instruction·····I/O Segment refresh

	Usable Devices																				Digit Setting	No. of Steps	Sub-Set	Index	Carry Flag	Error Flag	
	Bit devices						Word (16-bit) devices									Constants		Points		Level							
	X	Y	M/S	L	B	F	T	C	D	W	R	A0	A1	Z	V	K	H	P	I	N					M9012	M9010	M9011
S	○	○																			○	7		—			

Segment refresh designation



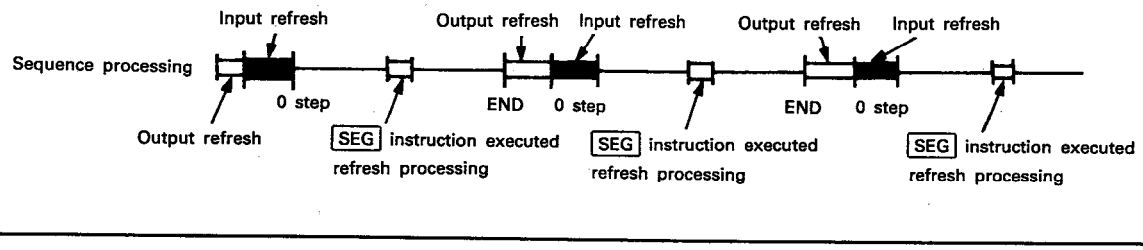
Set data

S	Set the head device number of the device executing segment I/O refresh.
n	Set in 8 point units the number of points executing the segment I/O refresh.

Functions

(1) Executes segment refresh processing of the I/O points contained within the number of bytes designated by D beginning from the device number designated by S (source).

(2) Segment refreshing is accomplished by the SEG instruction in a program only for the device points designated in the program. External data is fetched or outputs are given to an external device when refresh processing is executed. Thus segment refresh can be executed during a single scan at whatever point is necessary.



(3) Better program processing response time can be provided for inputs from external modules during sequence processing by fetching the ON/OFF status of the external inputs at the point at which the segment refresh instruction is executed. This can be done by executing segment I/O refresh in relation to input (X).

(4) When segment I/O fresh is executed in relation to output (Y), the ON/OFF status of output (Y) at the point the segment I/O refresh instruction is executed is output. Therefore, ON/OFF can be repeated during one scan by using the segment I/O refresh instruction.

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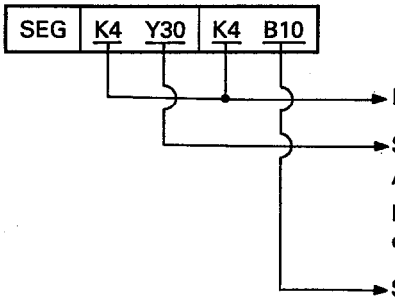
(5) The following shows how to set S (source) and n.



Be sure to set either K1, K2, K3, or K4. Which one is set will not affect processing.

Set the head device number that will execute the refresh.
Any setting between Y_n0 to Y_n7 (X_n0 to X_n7) will refresh the designated number of points from Y_n0 (X_n0). Any setting between Y_n8 to Y_nF (X_n8 to X_nF) will refresh the designated number of points from Y_n8 (X_n8).

Set the number of refresh points.
The number of refresh points is the set value times 8 points and is set in hexadecimal.

The maximum setting range is BFF (2048 points).

Relationship between the setting value and the number of refresh points

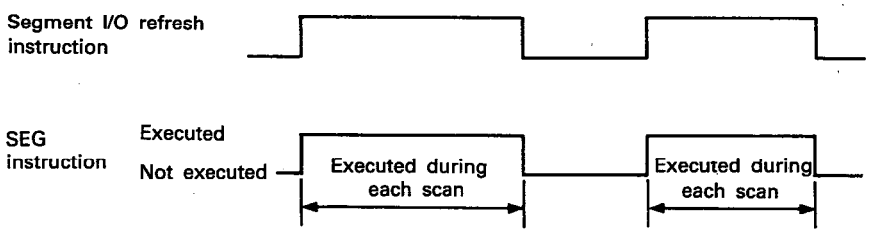
B1 = 8 points
B2 = 16 points
⋮
BA = 80 points
BB = 88 points
⋮
B10 = 128 points
⋮
BFF = 2048 points

POINT

(1) The "B" used in the refresh point setting has no relationship with the "B" of link relay "B". Link relay "B" can be used for up to 1024 points.
(2) When setting the number of refresh points to "B0" (0 points), all of the device numbers (installed units) set by the head device number are refreshed.

Execution Conditions

The following shows what conditions must exist for the SEG instruction to be executed.



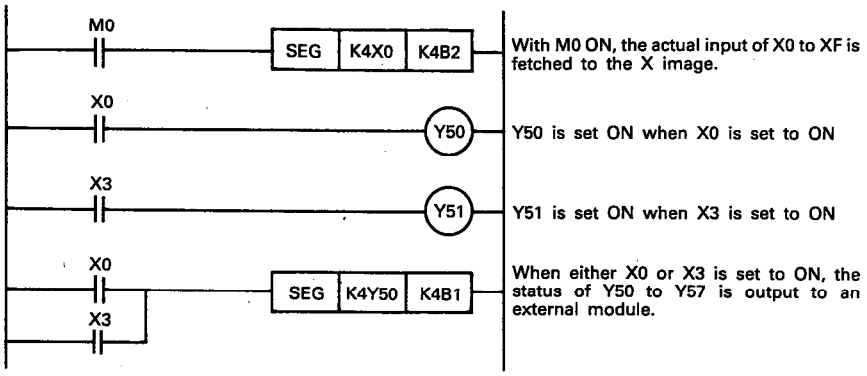
Operation Error

In the following examples, an error is generated during operation and the error flag is set to ON.
(1) A mistake has been made in the S (source) or n device. (Set to a value other than X, Y, or B.)
(2) The segment I/O refresh range exceeded X, Y7FF.

APP

Program Example

To fetch the actual input from X0 to XF to the X image when M0 is ON and after the next step, to set Y50 and Y51 ON in response to setting ON of X0 and X3 respectively.



APP

APPENDIX 6 System Operation Status

This section describes the system operation status for the independent operation mode and majority operation mode when the factors which determine the system operational status are combined.

6.1 System operation status in independent operation mode

There are four factors that determine operation status for a system in the independent operation mode. The following describes the system operational status when these factors are combined together.

Factors
- Position of the A3VTU RUN/STOP key switch
- Position of the A3VCPU RUN/STOP key switch
- Instruction from external source (Remote RUN/STOP contacts, remote PAUSE contacts, Remote RUN/PAUSE from peripheral device)
- ON/OFF status of M9040 (PAUSE enable coil)

(1) Determine the operation status of the system in the following status
1) Check the operation status of the A3VCPU.
2) Check the system operation status with information received from 1., the position of the RUN/STOP key switch, and the ON/OFF status of M9040.

(2) Operation status of the A3VCPU

RUN/STOP Key Switch of the VCPU \ GPP/PHP/HGP	Remote RUN						Remote STOP	Remote PAUSE
Remote RUN/STOP Contacts	OFF					ON		
STOP Instruction	Not executed				Executed			
M9040	OFF		ON					
Remote PAUSE Contact	OFF	ON	OFF	ON				
STOP	STOP							
RUN	RUN			PAUSE	STOP			PAUSE
REPAIR	RUN			PAUSE	STOP			PAUSE

(3) System operation status
The operation status of the system is determined by the operation status of the A3VCPU and the setting of RUN/STOP key switch of the A3VTU.
The table below shows system operation status.

A3VTU RUN/STOP Key Switch \ M9040 / Operation Status of the A3VCPU	OFF			ON		
	STOP	PAUSE	RUN	STOP	PAUSE	RUN
STOP	STOP					
PAUSE	STOP	PAUSE	RUN	STOP	PAUSE	PAUSE
RUN	STOP	PAUSE	RUN	STOP	PAUSE	RUN

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6.2 System operation status in majority operation mode

There are four factors that determine operation status for a majority system. The following describes the system operational status when these factors are combined together.

Factors
- Position of the A3VTU RUN/STOP key switch
- Position of the A3VCPU RUN/STOP key switches of the three modules.
- Instruction from external source (Remote RUN/STOP contacts, remote PAUSE contacts)
- ON/OFF status of M9040 (PAUSE enable coil)

(1) Determine the operation status of the system in the following status

1) Check the operation status of each of the three A3VCPU modules.
2) Check the system operation status with information received from 1., the position of the RUN/STOP key switch, and the ON/OFF status of M9040.

(2) Operation status of the A3VCPU

Check the status of each of the A3VCPUs using table 6.1-(2). (Neither error status nor WAIT status has any relationship with the system operation status.)

(3) System operation status

The operation status of the system is determined by the operation status of the A3VCPUs of each of the three stations, the RUN/STOP key switch of the A3VTU, and the ON/OFF status of M9040.
The table on the next page shows system operational status.

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A3VTU RUN/STOP Key Switch				STOP						PAUSE						RUN					
CPU C (A3VCPU) Operational Status	CPU B (A3VCPU) Operational Status	CPU A (A3NCPU) Operational Status		M9040 = OFF			M9040 = ON			M9040 = OFF			M9040 = ON			M9040 = OFF			M9040 = ON		
				STOP	PAUSE	RUN	STOP	PAUSE	RUN	STOP	PAUSE	RUN	STOP	PAUSE	RUN	STOP	PAUSE	RUN	STOP	PAUSE	RUN
M9040 = OFF	STOP	M9040 = OFF	STOP	⁄	⁄	⁄	⁄	⁄	⁄	⁄		○	⁄			⁄		○	⁄		○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
		M9040 = ON	STOP	⁄	⁄	⁄	⁄	⁄	⁄	⁄		○	⁄			⁄		○	⁄		○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
	PAUSE	M9040 = OFF	STOP	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
		M9040 = ON	STOP	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
	RUN	M9040 = OFF	STOP	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
		M9040 = ON	STOP	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
M9040 = ON	STOP	M9040 = OFF	STOP	⁄	⁄	⁄	⁄	⁄	⁄	⁄		○	⁄			⁄		○	⁄		○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
		M9040 = ON	STOP	⁄	⁄	⁄	⁄	⁄	⁄	⁄		○	⁄			⁄		○	⁄		○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
	PAUSE	M9040 = OFF	STOP	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
		M9040 = ON	STOP	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○						○			○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
	RUN	M9040 = OFF	STOP	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄	○	○	○	○	○	○	○	○	○	○	○	○
		M9040 = ON	STOP	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
			PAUSE	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○
			RUN	⁄	⁄	⁄	⁄	⁄	⁄			○				○	○	○	○	○	○

Table 6.1 Operation Status in Majority Operation Mode

System operational status·····⁄ : STOP, □ : PAUSE, ○ : RUN, ◎ : Majority operation

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APPENDIX 7 Instruction Table

7.1 Types of instructions

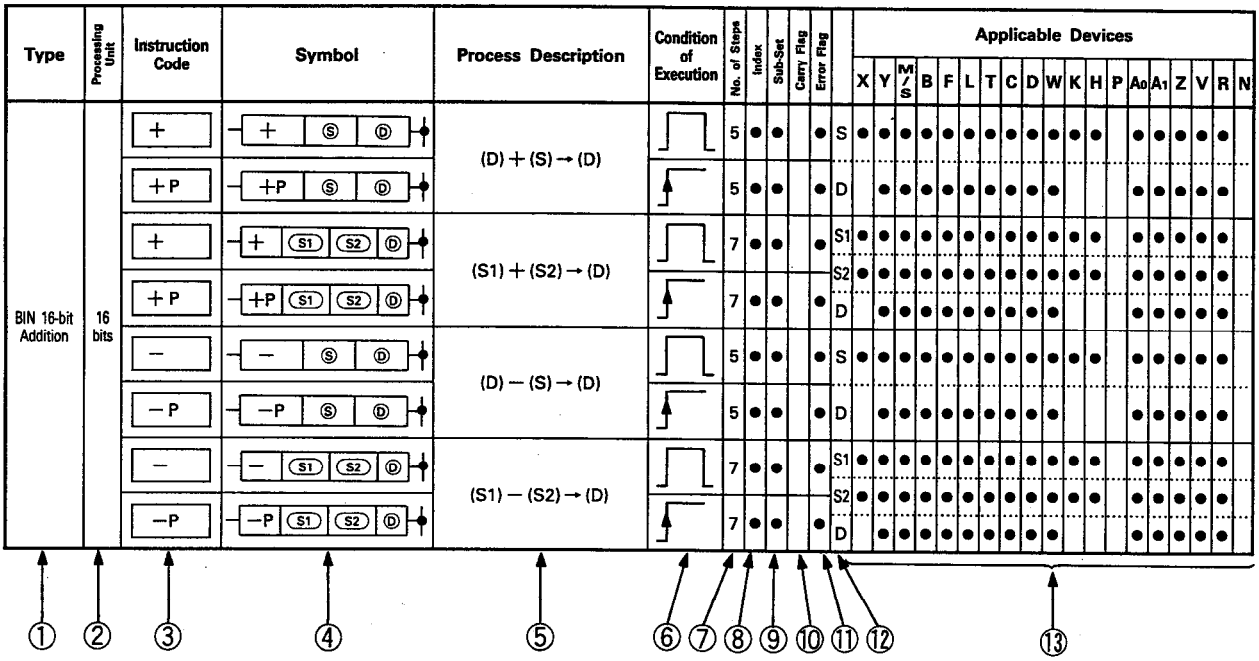
Type of Instruction		Description
Sequence instructions	Contact instruction	Start of operations, serial connections, parallel connections
	Connect instruction	Circuit block connections, write and read of arithmetic operation results
	Output instruction	Bit device output, pulse output, output reverse
	Shift instruction	Bit device shift
	Master control instruction	Master control
	Program branch instruction	Program jump, call of sub-routines, interrupt programs, etc.
	Program switching instruction	Main program ⟷ sub-program switching
	[FOR] to [NEXT] instruction	Program repetition between [FOR] and [NEXT] instructions
	Refresh instruction	Executes link and segment refreshes
	[END] instruction	Program [END]
	Other instructions	Instructions not listed above that include program halt and non-processing.
Basic instructions	Relational operation instruction	=, >, < and other relative symbols
	Arithmetic operation instruction	Arithmetic operations for [BIN] and [BCD] (addition, subtraction, multiplication, and division)
	[BCD] ⟷ [BIN] conversion instruction	[BCD] → [BIN] and [BIN] → [BCD] conversion
	Data transmit instruction	Transmits designated data
Application instructions	Logical operation instruction	Provides logic operations such as OR and AND
	Rotation instruction	Rotates designated data
	Shift instruction	Shifts designated data
	Data processing instruction	16-bit data search, decode, encode and other data processing functions
	[FIFO] instruction	[FIFO] table read/write
	Buffer memory access instruction	Special function module data read/write
	Local, remote I/O station access instruction	Local station data read/write
	Display instruction	ASCII code print, character LED display, etc.
	Others	WDT reset, carry flag set/reset and other instruction not listed above.

Table 7.1 Type of Instruction

7.2 Instruction table

7.2.1 How to read the tables

The instruction table lists all the instructions usable in the MELSEC-A series.
Those which cannot be used in the A3VTS are marked with an "X". All other instructions can be used in the A3VTS. The instruction tables given in Sections 7.2.2 to 7.2.4 use the following format.



Explanation

①·····Instructions are classified by applications.

②·····Indicates processing unit used when instruction is being executed.

Processing Unit	Device	Points
16 bits	X, Y, M, L, S, F, B	4 points per unit with maximum of 16 points
	T, C, D, W, R, A, Z, V	1 point
32 bits	X, Y, M, L, S, F, B	4 points per unit with maximum of 32 points
	T, C, D, W, R, A0, V	2 points

Fig. 7.1 Device Processing Units

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③·····Indicates the instruction symbol used in a program. A 16-bit instruction is the standard instruction. 32-bit and instructions executed only at OFF to ON rising edge become as shown in the following diagram.

32-bit instruction·····D is added to the head of instruction.

Example: + ——→ D+

16-bits instruction　　32-bits instruction

Instructions executed only at OFF → ON rising edge·····P is added to the END of the instruction.

Example: + ——→ +P

Instruction executed while ON status　　Instruction executed only at OFF → ON rising edge

④·····Shows symbol used on circuit.

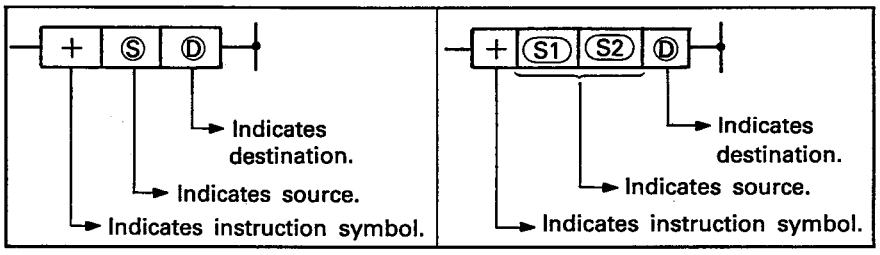
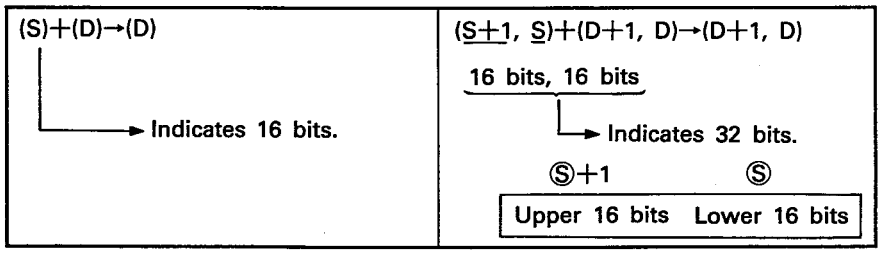


Fig. 4.2 Symbol Representations in Ladder

Destination indicates where data is going after operation. Source indicates from where the data was provided prior to operation.

⑤·····Indicates the contents of the processing used for an instruction.



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⑥·····The conditions of execution for each instruction are detailed as shown below.

Symbol	Condition of Execution
No symbol	An instruction to be executed unconditionally; this instruction is executed without regard to any ON/OFF conditions. If the prior condition is OFF, the instruction will conduct OFF processing.
	A modal type instruction to be executed during ON; this instruction is executed only while the prior condition stays ON. If the prior condition is OFF, the instruction is not executed and thus processing is not made.
	A one-shot type instruction to be executed during ON; this instruction is executed at the rising edge of the preceding condition. Once it has been executed, it is not executed again even when the condition stays ON.
	A one-shot type instruction to be executed during OFF; this instruction is executed at the falling edge of the preceding condition. Once it has been executed, it is not executed again even when the condition stays ON.

⑦·····This indicates the number of steps used for an instruction. When the number of steps varies depending on conditions, they are indicated in two steps.
For more detail, refer to the description of each instruction.

⑧·····● indicates an instruction to which an index (Z, V) can be added.

⑨·····● indicates an instruction which has subset instructions.

⑩·····● indicates that the instruction changes the carry flag.

⑪·····● indicates that the error flag is set to ON when an operation error is generated.

⑫·····Alphabetic letters at S (source) and D (destination) positions in the symbol chart are entered. The devices usable as a source or destination for that instruction are indicated in the corresponding columns.

⑬·····The devices which can be used for S and D indicated in column ⑫. The entry of a marker (●) indicates the usable device and the lack of a marker indicates that it cannot be used.

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7.2.2 Sequence instruction

(1) Contact instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Contact	–	LD		Begin logical operations (begin a contact logical operations)		1					●	●	●	●	●	●	●	●											
		LDI		Begin logical NOT operations (begin b contact logical operations)		1					●	●	●	●	●	●	●	●											
		AND		AND (a contact serial connections)		1					●	●	●	●	●	●	●	●											
		ANI		NAND (b contact serial connections)		1					●	●	●	●	●	●	●	●											
		OR		OR (a contact parallel connections)		1					●	●	●	●	●	●	●	●											
		ORI		NOR (b contact parallel connections)		1					●	●	●	●	●	●	●	●											

Table 7.2 Contact Instruction

(2) Connect instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Connect	–	ANB		AND for between logical blocks (serial connection of blocks)		1																							
		ORB		OR for between logic blocks (parallel connection of blocks)		1																							
		MPS	MPS MRD MPP	Stores results of logical operations		1																							
		MRD		Reads results of logical operations stored with MPS		1																							
		MPP		Reads and resets results of logical operations stored with MPS		1																							

Table 7.3 Connect Instructions

(3) Output instruction

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Output	–	OUT		Device output		1/3						●	●	●	●	●	●	●											
																			●		●								
		SET	SET D	Device set	✳	1					D	●	●			●													
						3					D		●	●	●															
		RST	RST D	Device reset	✳	1					D	●	●			●	●	●	●					●	●	●	●	●	
						3					D		●	●	●					●									
		PLS	PLS D	Generates 1 program cycle of pulses at rising edge of input signal	↑	3					D	●	●	●	●	●													
		PLF	PLF D	Generates 1 program cycle of pulses at falling edge of input signal	↓	3					D	●	●	●	●	●													
		CHK	CHK D1 D2	Reverses device output at I/O refresh		5					D1	●	●	●	●	●	●													
											D2	●	●	●	●	●	●	●	●						●	●	●	●	●	

Table 7.4 Output Instructions

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1. **The number of steps for the OUT, SET, and RST instructions varies (1 or 3) depending on the device. 3 step devices are the following: OUT instruction: F, M9000 to M9255, SET instruction: B, F, M9000 to M9255, RST instruction: B, F, W, M9000 to M9255**
2. **For the execute conditions of the output instruction, the asterisk "✳" indicates that the device operates as ⎍ for F (annunciator) and ⎍ otherwise.**

(4) Shift instruction

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Shift	–	SFT	SFT Ⓓ	1-bit shift for a device	⎍	3					D		●	●	●	●	●														
		SFTP	SFTP Ⓓ		⎍	3					D		●	●	●	●	●														

Table 7.5 Shift Instructions

(5) Master control instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Master control	–	MC	MC n Ⓓ	Begins master control		5					n																				●
											D			●	●	●	●	●													
		MCR	MCR n	Terminates master control		3					n																				●

Table 7.6 Master Control Instructions

(6) Program branch instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Jump	–	CJ	CJ P✳✳	Jump to P✳✳ after input conditions fulfilled	⎍	3	●			●														●						
		SCJ	SCJ P✳✳	Jump to P✳✳ in the next scan after input conditions fulfilled		3	●			●														●						
		JMP	JMP P✳✳	Jump to P✳✳ unconditionally		3	●			●														●						
Sub-routine call	–	CALL	CALL P✳✳	Execute sub-routine P✳✳ after input conditions fulfilled	⎍	3	●			●																				
		CALLP	CALLP P✳✳		⎍	3	●			●														●						
		RET	RET	Return to sequence program after sub-routine program		1																								
Interrupt program	–	EI	EI	Enables interrupt program run. Valid for A□N with M9053 off.		1																								
		DI	DI	Disables interrupt program run. Valid for A□N with M9053 off.		1																								
		IRET	IRET	Return from the interrupt program to the sequence program.		1																								
Micro-computer program call	–	SUB	SUB n	Executes the micro-computer program designated by n.	⎍	3	●			●	n							●	●	●	●	●	●		●	●	●	●	●	
		SUBP	SUBP n		⎍	3	●			●																				

Table 7.7 Program Branch Instructions

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(7) Program switch instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Switch	–	CHG	CHG	Switches between main- and sub-programs		1																							

Table 7.8 Program Switch Instructions

(8) FOR to NEXT Instruction

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
FOR to NEXT	–	FOR	FOR n	Executes program between FOR and NEXT for n times		3				●	n							●	●	●	●	●	●		●	●	●	●	●	
		NEXT	NEXT			1				●																				

Table 7.9 FOR to NEXT Instruction

(9) Refresh instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Link refresh	–	COM	COM	Link refresh, general data processing executed		3																							
Link refresh Enable /disable	–	EI	EI	Clears link refresh disabled status: when M9053 is ON		1																							
		DI	DI	Enables link refresh: when M9053 is ON		1																							
Segment refresh	–	SEG	SEG Ⓢ n	Executes a segment refresh of selected device only during 1 scan.		7																							

Table 7.10 Refresh Instructions

(10) END instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
END instruction	–	FEND	FEND	Always placed at end of main routine program to end processing.		1																							
	–	END	—	Always placed at end of sequence routine program to end processing.		1																							

Table 7.11 END Instructions

(11) Other instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
Stop	–	STOP	STOP	Results output after the input conditions are fulfilled, and stops the sequence program. When the RUN key switch is again set to "RUN", the sequence program begins execution again.		1																							
No processing	–	NOP	—	No processing For program erasure or spaces.		1																							

Table 7.12 Other Instructions

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7.2.3 Basic instructions

(1) Relational operation instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A_0	A_1	Z	V	R	N
16-bit data relations	16 bits	LD =	LD= S1 S2	(S1) = (S2): Conducting (S1) ≠ (S2): Non-conducting		5 7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		AND =	AND= S1 S2			5 7	●	●		●																				
		OR =	OR= S1 S2			5 7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		LD < >	LD<> S1 S2	(S1) ≠ (S2): Conducting (S1) = (S2): Non-conducting		5 7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		AND < >	AND<> S1 S2			5 7	●	●		●																				
		OR < >	OR<> S1 S2			5 7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		LD >	LD> S1 S2	(S1) > (S2): Conducting (S1) ≦ (S2): Non-conducting		5 7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		AND >	AND> S1 S2			5 7	●	●		●																				
		OR >	OR> S1 S2			5 7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		LD < =	LD<= S1 S2	(S1) ≦ (S2): Conducting (S1) > (S2): Non-conducting		5 7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		AND < =	AND<= S1 S2			5 7	●	●		●																				
		OR < =	OR<= S1 S2			5 7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		LD <	< S1 S2	(S1) < (S2): Conducting (S1) ≧ (S2): Non-conducting		5 7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		AND <	< S1 S2			5 7	●	●		●																				
		OR <	< S1 S2			5 7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		LD > =	>= S1 S2	(S1) ≧ (S2): Conducting (S1) < (S2): Non-conducting		5 7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		AND > =	>= S1 S2			5 7	●	●		●																				
		OR > =	>= S1 S2			5 7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
32-bit data relations	32 bits	LDD =	LDD= S1 S2	(S1+1, S1) = (S2+1, S2): Conducting (S1+1, S1) ≦ (S2+1, S2): Non-conducting		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		ANDD =	ANDD= S1 S2			11	●			●																				
		ORD =	ORD= S1 S2			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		LDD < >	LDD<> S1 S2	(S1+1, S1) ≠ (S2+1, S2): Conducting (S1+1, S1) = (S2+1, S2): Non-conducting		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		ANDD < >	ANDD<> S1 S2			11	●			●																				
		ORD < >	ORD<> S1 S2			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	

Table 7.13 Relational Operation Instructions (Continue)

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Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	Ao	A1	Z	V	R	N
32-bit data relations	32 bits	LDD >	LDD> S1 S2	(S1+1, S1) > (S2+1, S2): Conducting (S1+1, S1) ≦ (S2+1, S2): Non-conducting		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		ANDD >	ANDD> S1 S2			11	●			●																				
		ORD >	ORD> S1 S2			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		LDD < =	LDD<= S1 S2	(S1+1, S1) ≦ (S2+1, S2): Conducting (S1+1, S1) > (S2+1, S2): Non-conducting		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		ANDD < =	ANDD<= S1 S2			11	●			●																				
		ORD < =	ORD<= S1 S2			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		LDD <	D< S1 S2	(S1+1, S1) < (S2+1, S2): Conducting (S1+1, S1) ≧ (S2+1, S2): Non-conducting		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		ANDD <	D< S1 S2			11	●			●																				
		ORD <	D< S1 S2			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		LDD>=	D >= S1 S2	(S1+1, S1) ≧ (S2+1, S2): Conducting (S1+1, S1) < (S2+1, S2): Non-conducting		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		ANDD>=	D >= S1 S2			11	●			●																				
		ORD>=	D >= S1 S2			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	

Table 7.13 Relational Operation Instructions

(2) Arithmetic operation instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	Ao	A1	Z	V	R	N
BIN 16-bit addition/ subtraction	16 bits	+	+ S D	(D) + (S) → (D)		5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		+P	+P S D			5	●	●		●	D		●	●	●	●	●	●	●	●					●	●	●	●	●	
		+	+ S1 S2 D	(S1) + (S2) → (D)		7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		+P	+P S1 S2 D			7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											D		●	●	●	●	●	●	●	●					●	●	●	●	●	
		−	− S D	(D) − (S) → (D)		5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		−P	−P S D			5	●	●		●	D		●	●	●	●	●	●	●	●					●	●	●	●	●	
		−	− S1 S2 D	(S1) − (S2) → (D)		7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		−P	−P S1 S2 D			7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											D		●	●	●	●	●	●	●	●					●	●	●	●	●	
BIN 32-bit addition/ subtraction	32 bits	D+	D+ S D	(D + 1, D) + (S + 1, S) → (D + 1, D)		9	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		D+P	D+P S D			9	●	●		●	D		●	●	●	●	●	●	●	●					●		●		●	
		D+	D+ S1 S2 D	(S1 +1, S1) + (S2 + 1, S2) → (D + 1, D)		11	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		D+P	D+P S1 S2 D			11	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
											D		●	●	●	●	●	●	●	●					●		●		●	

Table 7.14 Arithmetic Operation Instructions (Continue)

APP

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices																		
												X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A_0	A_1	Z	V	R	N
BIN 32-bit addition/ subtraction	32 bits	D−	D− Ⓢ Ⓓ	(D+1, D) − (S+1, S) →(D+1, D)		9	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		D−P	D−P Ⓢ Ⓓ			9	●	●		●	D		●	●	●	●	●	●	●	●	●				●		●		●	
		D−	D− (S1) (S2) Ⓓ	(S1+1, S1) − (S2+1, S2) → (D+1, D)		11	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		D−P	D−P (S1) (S2) Ⓓ			11	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
											D		●	●	●	●	●	●	●	●	●				●		●		●	
BIN 16-bit multipli- cation/ division	16 bits	✳	✳ (S1) (S2) Ⓓ	(S1) × (S2) → (D+1, D)		7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		✳P	✳P (S1) (S2) Ⓓ			7	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		/	/ (S1) (S2) Ⓓ	(S1) ÷ (S2) → Quotient (D), Remainder (D+1)		7	●	●		●	D		●	●	●	●	●	●	●	●	●				●		●		●	
		/P	/P (S1) (S2) Ⓓ			7	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
BIN 32-bit multipli- cation/ division	32 bits	D✳	D✳ (S1) (S2) Ⓓ	(S1+1, S1) × (S2+1, S2) → (D+3, D+2, D+1, D)		11	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		D✳P	D✳P (S1) (S2) Ⓓ			11	●	●		●	D		●	●	●	●	●	●	●	●	●								●	
		D/	D/ (S1) (S2) Ⓓ	(S1+1, S1) ÷ (S2+1, S2) → Quotient (D+1, D), Remainder (D+3, D+2)		9	●	●		●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		D/P	D/P (S1) (S2) Ⓓ			9	●	●		●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
											D		●	●	●	●	●	●	●	●	●				●		●		●	
BCD 4-digit addition/ subtraction	BCD 4 digits	B+	B+ Ⓢ Ⓓ	(D) + (S) → (D)		7	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		B+P	B+P Ⓢ Ⓓ			7	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		B+	B+ (S1) (S2) Ⓓ	(S1) + (S2) → (D)		9	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		B+P	B+P (S1) (S2) Ⓓ			9	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		B−	B− Ⓢ Ⓓ	(S1) − (S2) → (D)		7	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		B−P	B−P Ⓢ Ⓓ			7	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		B−	B− (S1) (S2) Ⓓ	(S_1) − (S_2) → (D)		9	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		B−P	B−P (S1) (S2) Ⓓ			9	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
BCD 8-digit addition/ subtraction	BCD 8 digits	DB+	DB+ Ⓢ Ⓓ	(D+1, D) + (S+1, S) →(D+1, D)		9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DB+P	DB+P Ⓢ Ⓓ			9	●			●	D		●	●	●	●	●	●	●	●	●				●		●		●	
		DB+	DB+ (S1) (S2) Ⓓ	(S1+1, S1) + (S2+1, S2) → (D+1, D)		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DB+P	DB+P (S1) (S2) Ⓓ			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
											D		●	●	●	●	●	●	●	●	●				●		●		●	
		DB−	DB− Ⓢ Ⓓ	(D+1, D) − (S+1, S) →(D+1, D)		9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DB−P	DB−P Ⓢ Ⓓ			9	●			●	D		●	●	●	●	●	●	●	●	●				●		●		●	
		DB−	DB− (S1) (S2) Ⓓ	(S1+1, S1) + (S2+1, S2) →(D+1, D)		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DB−P	DB−P (S1) (S2) Ⓓ			11	●			●	S2	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
											D		●	●	●	●	●	●	●	●	●				●		●		●	

Table 7.14 Arithmetic Operation Instructions (Continue)

APP

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
BCD 4-digit multiplication/division	BCD 4 digits	B✳	B✳ S1 S2 D	(S1) × (S2) → (D + 1, D)		9	●			●	S1	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	
											S2	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	
		B✳P	B✳P S1 S2 D			9	●			●	D		●	●	●	●	●	●	●	●					●		●		●	
		B/	B/ S1 S2 D	(S1) ÷ (S2) → Quotient (D) remainder (D + 1)		9	●			●	S1	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	
											S2	●	●	●	●	●	●	●	●	●	●	●			●	●	●	●	●	
		B/P	B/P S1 S2 D			9	●			●	D		●	●	●	●	●	●	●	●					●		●		●	
BCD 8-digit multiplication/division	BCD 8 digits	DB✳	DB✳ S1 S2 D	(S1 + 1, S1) × (S2 + 1, S2) → (D + 3, D + 2, D + 1, D)		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●			●		●		●	
											S2	●	●	●	●	●	●	●	●	●	●	●			●		●		●	
		DB✳P	DB✳P S1 S2 D			11	●			●	D		●	●	●	●	●	●	●	●									●	
		DB/	DB/ S1 S2 D	(S1 + 1, S1) ÷ (S2 + 1, S2) → Quotient (D + 1, D) remainder (D + 3, D + 2)		11	●			●	S1	●	●	●	●	●	●	●	●	●	●	●			●		●		●	
											S2	●	●	●	●	●	●	●	●	●	●	●			●		●		●	
		DB/P	DB/P S1 S2 D			11	●			●	D		●	●	●	●	●	●	●	●									●	
BIN data increment	16 bits	INC	INC D	(D) + 1 → (D)		3	●	●		●	D		●	●	●	●	●	●	●	●					●	●	●	●	●	
		INCP	INCP D			3	●	●		●																				
	32 bits	DINC	DINC D	(D+1, D)+1→(D+1, D)		3	●	●		●	D		●	●	●	●	●	●	●	●					●		●		●	
		DINCP	DINCP D			3	●	●		●																				
BIN data increment	16 bits	DEC	DEC D	(D) − 1 → (D)		3	●	●		●	D		●	●	●	●	●	●	●	●					●	●	●	●	●	
		DECP	DECP D			3	●	●		●																				
	32 bits	DDEC	DDEC D	(D+1, D)−1→(D+1, D)		3	●	●		●	D		●	●	●	●	●	●	●	●					●		●		●	
		DDECP	DDECP D			3	●	●		●																				

Table 7.14 Arithmetic Operation Instructions

(3) BCD ↔ BIN conversion instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
BCD conversion	16 bits	BCD	BCD S D	BCD conversion (S) → (D); BIN (0 to 9999)		5	●	●		●	S	●	●	●	●	●	●	●	●	●					●	●	●	●	●	
		BCDP	BCDP S D			5	●	●		●	D		●	●	●	●	●	●	●	●					●	●	●	●	●	
	32 bits	DBCD	DBCD S D	BCD conversion (S1 + 1, S1) → (D + 1, D); BIN (0 to 99999999)		9	●			●	S	●	●	●	●	●	●	●	●	●					●		●		●	
		DBCDP	DBCDP S D			9	●			●	D		●	●	●	●	●	●	●	●					●		●		●	
BIN conversion	4 digits	BIN	BIN S D	BIN conversion (S) → (D); BCD (0 to 9999)		5	●	●		●	S	●	●	●	●	●	●	●	●	●					●	●	●	●	●	
		BINP	BINP S D			5	●	●		●	D		●	●	●	●	●	●	●	●					●	●	●	●	●	
	8 digits	DBIN	DBIN S D	BIN conversion (S1 + 1, S1) → (D + 1, D); BCD (0 to 99999999)		9	●			●	S	●	●	●	●	●	●	●	●	●					●		●		●	
		DBINP	DBINP S D			9	●			●	D		●	●	●	●	●	●	●	●					●		●		●	

Table 7.15 BCD ↔ BIN Conversion Instructions

APP

(4) Data transmit instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices																		
												X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A_0	A_1	Z	V	R	N
Transmit	16 bits	MOV	MOV (S) (D)	(S) → (D)		5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		MOVP	MOVP (S) (D)			5	●	●		●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
	32 bits	DMOV	DMOV (S) (D)	(S1+1, S) → (D+1, D)		7	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DMOVP	DMOVP (S) (D)			7	●	●		●	D		●	●	●	●	●	●	●	●	●				●		●		●	
Negation transmit	16 bits	CML	CML (S) (D)	$\overline{(S)}$ → (D)		5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		CMLP	CMLP (S) (D)			5	●	●		●	D		●	●	●	●	●	●	●	●	●				●		●		●	
	32 bits	DCML	DCML (S) (D)	$\overline{(S1+1, S)}$ → (D+1, D)		7	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DCMLP	DCMLP (S) (D)			7	●	●		●	D		●	●	●	●	●	●	●	●	●				●		●		●	
Block transmit	16 bits	BMOV	BMOV (S) (D) n	(S) (D) n		9	●			●	S	●	●	●	●	●	●	●	●	●	●								●	
		BMOVP	BMOVP (S) (D) n			9	●			●	D		●	●	●	●	●	●	●	●	●								●	
											n											●	●							
		FMOV	FMOV (S) (D) n	(S) (D) n		9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		FMOVP	FMOVP (S) (D) n			9	●			●	D		●	●	●	●	●	●	●	●	●								●	
											n											●	●							
Exchange	16 bits	XCH	XCH (D1) (D2)	(D1) ↔ (D2)		5	●	●		●	D1		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		XCHP	XCHP (D1) (D2)			5	●	●		●	D2		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
	32 bits	DXCH	DXCH (D1) (D2)	(D1+1, D1) → ← (D2+1, D2)		7	●	●		●	D1		●	●	●	●	●	●	●	●	●				●		●		●	
		DXCHP	DXCHP (D1) (D2)			7	●	●		●	D2		●	●	●	●	●	●	●	●	●				●		●		●	

Table 7.16 Data Transmit Instructions

APP

7.2.4 Application instructions

(1) Logical operation instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
AND operations	16 bits	WAND	WAND Ⓢ Ⓓ	(D) ∧ (S) → (D)	⌐¬	5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WANDP	WANDP Ⓢ Ⓓ		⌐↑	5	●	●		●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		WAND	WAND (S1) (S2) Ⓓ	(S1) ∧ (S2) → (D)	⌐¬	7	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WANDP	WANDP (S1) (S2) Ⓓ		⌐↑	7	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
	32 bits	DAND	DAND Ⓢ Ⓓ	(D+1, D) ∧ (S+1, S) → (D+1, D)	⌐¬	9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DANDP	DANDP (S1) (S2) Ⓓ		⌐↑	9	●			●	D		●	●	●	●	●	●	●	●	●				●		●		●	
OR operations	16 bits	WOR	WOR Ⓢ Ⓓ	(D) ∨ (S) → (D)	⌐¬	5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WORP	WORP Ⓢ Ⓓ		⌐↑	5	●	●		●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		WOR	WOR (S1) (S2) Ⓓ	(S1) ∨ (S2) → (D)	⌐¬	7	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WORP	WORP (S1) (S2) Ⓓ		⌐↑	7	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
	32 bits	DOR	DOR Ⓢ Ⓓ	(D+1, D) ∨ (S+1, S) → (D+1, D)	⌐¬	9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DORP	DORP Ⓢ Ⓓ		⌐↑	9	●			●	D		●	●	●	●	●	●	●	●	●				●		●		●	
Exclusive OR operations	16 bits	WXOR	WXOR Ⓢ Ⓓ	(S1) ⊻ (S2) → (D)	⌐¬	5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WXORP	WXORP Ⓢ Ⓓ		⌐↑	5	●	●		●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		WXOR	WXOR (S1) (S2) Ⓓ	(S1) ⊻ (S2) → (D)	⌐¬	7	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WXORP	WXORP (S1) (S2) Ⓓ		⌐↑	7	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
	32 bits	DXOR	DXOR Ⓢ Ⓓ	(D+1, D) ⊻ (S+1, S) → (D+1, D)	⌐¬	9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DXORP	DXORP Ⓢ Ⓓ		⌐↑	9	●			●	D		●	●	●	●	●	●	●	●	●				●		●		●	
Exclusive NOR operations	16 bits	WXNR	WXNR Ⓢ Ⓓ	$\overline{(D) \veebar (S)} \rightarrow (D)$	⌐¬	5	●	●		●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WXNRP	WXNRP Ⓢ Ⓓ		⌐↑	5	●	●		●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		WXNR	WXNR (S1) (S2) Ⓓ	$\overline{(S1) \veebar (S2)} \rightarrow (D)$	⌐¬	7	●			●	S1	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
											S2	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	
		WXNRP	WXNRP (S1) (S2) Ⓓ		⌐↑	7	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
	32 bits	DXNR	DXNR Ⓢ Ⓓ	$\overline{(D+1, D) \wedge (S+1, S)} \rightarrow (D+1, D)$	⌐¬	9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●	
		DXNRP	DXNRP Ⓢ Ⓓ		⌐↑	9	●	●		●	D		●	●	●	●	●	●	●	●	●				●		●		●	
Complements of 2	16 bits	NEG	NEG Ⓓ	$\overline{(D)} + 1 \rightarrow (D)$	⌐¬	3	●			●																				
		NEGP	NEGP Ⓓ		⌐↑	3	●			●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	

Table 7.17 Logical Operation Instructions

APP

(2) Rotation instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices																						
												X	Y	M / S	B	F	L	T	C	D	W	K	H	P	A_0	A_1	Z	V	R	N
Rotate right	16 bits	ROR	ROR n	Carry 15 A0 n 0 n-bit rotate to the right		3	●		●		n											●	●								
		RORP	RORP n			3	●		●													●	●								
		RCR	RCR n	A0 15 (16—n) n 0 Carry Carry n-bit rotate to the right		3	●		●		n											●	●								
		RCRP	RCRP n			3	●		●													●	●								
Rotate left		ROL	ROL n	A0 Carry 15 (16—n) 0 n-bit rotate to the left		3	●		●		n											●	●								
		ROLP	ROLP n			3	●		●													●	●								
		RCL	RCL n	A0 Carry 15 (16—n) n 0 Carry n-bit rotate to the left		3	●		●		n											●	●								
		RCLP	RCLP n			3	●		●													●	●								
Rotate right	32 bits	DROR	DROR n	A1 A0 Carry 15 0.15 n 0 n-bit rotate to the right		3	●		●		n											●	●								
		DRORP	DRORP n			3	●		●													●	●								
		DRCR	DRCR n	A1 A0 15 (16—n) 0.15 n 0 Carry Carry n-bit rotate to the right		3	●		●		n											●	●								
		DRCRP	DRCRP n			3	●		●													●	●								
Rotate left		DROL	DROL n	A1 A0 Carry 15 (16—n) 0.15 0 n-bit rotate to the left		3	●		●		n											●	●								
		DROLP	DROLP n			3	●		●													●	●								
		DRCL	DRCL n	A1 A0 Carry 15 (16—n) 0.15 n Carry n-bit rotate to the left		3	●		●		n											●	●								
		DRCLP	DRCLP n			3	●		●													●	●								

Table 7.18 Rotation Instructions

(3) Shift instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices																		
												X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A_0	A_1	Z	V	R	N
n-bit shift	16 bits	SFR	SFR Ⓓ n	15 n 0 / 15 to 0 Carry		5	●	●	●	●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		SFRP	SFRP Ⓓ n	15 0to0 0 Carry		5	●	●	●	●	n											●	●							
		SFL	SFL Ⓓ n	15 n 0 / 15 to 0 Carry		5	●	●	●	●	D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	
		SFLP	SFLP Ⓓ n	15 to 0 0 to 0 Carry		5	●	●	●	●	n											●	●							
1-bit shift	n bits	BSFR	BSFR Ⓓ n	n (D) to 0 Carry		7	●		●	●	D		●	●	●	●	●													
		BSFRP	BSFRP Ⓓ n			7	●		●	●	n											●	●							
		BSFL	BSFL Ⓓ n	n (D) to Carry 0		7	●		●	●	D		●	●	●	●	●													
		BSFLP	BSFLP Ⓓ n			7	●		●	●	n											●	●							
1-word shift	n words	DSFR	DSFR Ⓓ n	n (D) to 0		7	●			●	D							●	●	●	●								●	
		PSFRP	DSFRP Ⓓ n			7	●			●	n											●	●							
		DSFL	DSFL Ⓓ n	n (D) to 0		7	●			●	D							●	●	●	●								●	
		DSFLP	DSFLP Ⓓ n			7	●			●	n											●	●							

Table 7.19 Shift Instructions

APP

(4) Data processing instruction

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices																			
												X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A_0	A_1	Z	V	R	N
Data search	16 bits	SER	SER (S1) (S2) n	(S1) (S2) n; A0: Not found A1: No. of found search objectives		9	●			●	S1							●	●	●	●	●	●		●	●	●	●	●	●
											S2							●	●	●	●									●	
		SERP	SERP (S1) (S2) n			9	●			●	n											●	●								
Bit check		SUM	SUM (S)	15 (S) 0 → A0: No. of 1s		3	●			●																					
		SUMP	SUMP (S)			3	●			●	S	●	●	●	●	●	●	●	●	●	●				●	●	●	●	●	●	
	32 bits	DSUM	DSUM (S)	(S+1) (S) → A0: No. of 1s		3	●			●																					
		DSUMP	DSUMP (S)			3	●			●	S	●	●	●	●	●	●	●	●	●	●				●		●		●		
Decode/ encode	2^n bits	DECO	DECO (S) (D) n	8 → 256 decode; (S) n Decode (D) 2^n bits		9	●			●	S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	●
											D		●	●	●	●	●	●	●	●	●								●	
		DECOP	DECOP (S) (D) n			9	●			●	n											●	●								
		ENCO	ENCO (S) (D) n	256 → 8 encode; (S) 2^n bits Encode (D) n		9	●			●	S	●	●	●	●	●	●	●	●	●	●				●	●	●	●	●	●
											D							●	●	●	●				●	●	●	●	●	●
		ENCOP	ENCOP (S) (D) n			9	●			●	n											●	●								
7 segment decode	16 bits	SEG	SEG (S) (D)	(S) 3 0 7SEG (D) n 0 Decode; Valid for ACPU, A3H when M9052 is off.		7	●				S	●	●	●	●	●	●	●	●	●	●	●	●		●	●	●	●	●	●
											D		●	●	●	●	●	●	●	●	●				●	●	●	●	●	●
Bit set/reset		BSET	BSET (D) n	(D) 15 n 0 → 1		7	●			●	D							●	●	●	●				●	●	●	●	●	●
		BSETP	BSETP (D) n			7	●			●	n											●	●								
		BRST	BRST (D) n	(D) 15 n 0 → 0		7	●			●	D							●	●	●	●				●	●	●	●	●	●
		BRSTP	BRSTP (D) n			7	●			●	n											●	●								
Disperse/ unify		DIS	DIS (S) (D) n	4 bits; All 4 bits; S (D)+1 (D)+2 D; When n = 3		9	●			●	S							●	●	●	●	●	●		●	●	●	●	●	●
											D							●	●	●	●									●	
		DISP	DISP (S) (D) n			9	●			●	n											●	●								
		UNI	UNI (S) (D) n	4 bits; 4 bits; S (S)+1 (S)+2 D; When n = 3		9	●			●	S							●	●	●	●									●	
											D							●	●	●	●				●	●	●	●	●	●
		UNIP	UNIP (S) (D) n			9	●			●	n											●	●								
ASCII conversion	–	ASC	ASC Alphanumeric (D)	Alphanumeric is converted to ASCII code and written from (D) device to 4 points		13	●			●	D							●	●	●	●									●	

Table 7.20 Data Processing Instruction

APP

(5) FIFO instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices
Write	16 bits	FIFW	FIFW (S) (D)	(D) Pointer; (S); Pointer+1		7	●			●	S: X Y M/S B F L T C D W K H P A0 A1 Z V R N
		FIFWP	FIFWP (S) (D)			7	●			●	D: T C D W R
Read		FIFR	FIFR (D1) (D2)	(D2) Pointer; Pointer −1; (D1)		7	●			●	D1: X Y M/S B F L T C D W K H P A0 A1 Z V R N
		FIFRP	FIFRP (D1) (D2)			7	●			●	D2: T C D W R

Table 7.21 FIFO Instructions

(6) Buffer memory access instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices
Data read	1 word	FROM	FROM n1 n2 (D) n3	Reads data from a special function module		9	●			●	n1 n2: K H; D: X Y M/S B F L T C D W R; n3: K H
		FROMP	FROMP n1 n2 (D) n3			9	●			●	
	2 words	DFRO	DFRO n1 n2 (D) n3			9	●			●	
		DFROP	DFROP n1 n2 (D) n3			9	●			●	
Data write	1 word	TO	TO n1 n2 (S) n3	Writes data to a special function module		9	●			●	n1 n2: K H; S: X Y M/S B F L T C D W K H R; n3: K H
		TOP	TOP n1 n2 (S) n3			9	●			●	
	2 words	DTO	DTO n1 n2 (S) n3			11	●			●	
		DTOP	DTOP n1 n2 (S) n3			9	●			●	

Table 7.22 Buffer Memory Access Instructions

(7) Local, remote I/O station access instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag	Applicable Devices
Local station read/ write	1 word	LRDP	LRDP n1 (S) (D) n2	Reads local station data		11	●			●	n1: K H; S: T C D W; D: T C D W; n2: K H
		LWTP	LWTP n1 (S) (D) n2	Writes data to local station		11	●			●	
Remote station read/ write		RFRP	RFRP n1 n2 (D) n3	Reads data from special function unit of remote station		11	●			●	n1 n2: K H; D: T C D W; n3: K H
		RTOP	RTOP n1 n2 (D) n3	Writes data to special function unit of remote station		11	●			●	

Table 7.23 Local, Remote I/O Station Access Instructions

APP

(8) Display instructions

Type	Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
ASCII print	–	PR	PR (S) (D)	Reads 8 points of ASCII code (16 characters) from the designated device and outputs to an output module.		7	●			●	S							●	●	●	●								●	
											D		●																	
		PR	PR (S) (D)	Reads ASCII codes continuously from the designated device until a NULL (00H) code is reached and outputs them to an output module.		7	●			●	S							●	●	●	●								●	
											D		●																	
		PRC	PRC (S) (D)	Converts designated device comments to ASCII code and outputs them to an output module. Comments from device 1 is permissible.		7	●				S	●	●	●	●	●	●	●	●	●	●			●					●	
											D		●																	
Display	–	LED	LED (S)	(S) to (S)+7 → Display 16 characters		3	●			●	S							●	●	●	●	●							●	
		LEDA	LEDA Alphanumeric	Displays the designated alphanumeric characters on LED. (LEDA: First 8 characters, LEDB: Last 8 characters)		13																								
		LEDB	LEDB Alphanumeric			13																								
		LEDC	LEDC (S)	Displays comments of (S) device.		3	●			●	S	●	●	●	●	●	●	●	●	●	●			●					●	
Display reset	–	LEDR	LEDR	Resets LED display.		1																								

Table 7.24 Display Instructions

(9) Other instructions

Type		Processing Unit	Instruction Code	Symbol	Process Description	Condition of Execution	No. of Steps	Index	Sub-Set	Carry Flag	Error Flag		Applicable Devices: X	Y	M/S	B	F	L	T	C	D	W	K	H	P	A0	A1	Z	V	R	N
WDT reset		–	WDT	WDT	Resets WDT during sequence program		1																									
		–	WDTP	WDTP			1																									
Malfunction check		–	CHK	CHK (D1) (D2)	If malfunction (D1):ON (D2):Malfunction NO If normal (D1):OFF, (D2):0 A□N in I/O direct control		5					D1	●	●	●	●	●													
												D2	●	●	●	●	●	●	●	●	●				●	●	●	●	●		
Status latch	Set	–	SLT	SLT	Stores data in the status latch memory in the conditions set by the parameter settings.		1																									
	Reset		SLTR	SLTR	Clears the status latch and enables the SLT instruction again.		1																									
Sampling trace	Set	–	STRA	STRA	Stores the sampling data in the sampling trace memory in the conditions set by the parameter settings.		1																									
	Reset		STRAR	STRAR	Restarts sampling trace. (enables the STRA instruction.)		1																									
Carry	Set	– 1 bit	STC	STC	Sets the carry flag contact (M9012) to ON.		1																									
	Reset		CLC	CLC	Sets the carry flag contact (M9012) to OFF.		1																									
Timing clock		1 bit	DUTY	DUTY n1 n2 (D)	Generates the timing clock shown below. Special register (D) n1 scans n2 scans		7				●	n1											●	●								
												n2											●	●							
												D		●																	

Table 7.25 Other Instructions

APP

APPENDIX 8 Special Relay, Special Register List

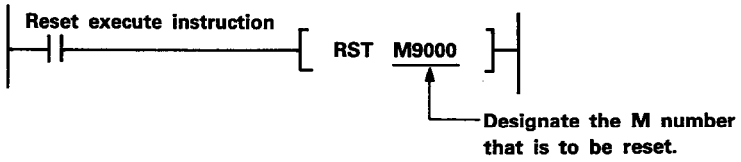
8.1 Special relay list

The special relays are internal relays that are used for predetermined purposes. The use of each of the special relays is divided into the types shown in the table below. These special relays should be used based on the uses given below.

	Type	Special Relay Application	Remarks
1	Relays turned ON/OFF by User	(1) Turned ON/OFF with the sequence program. (2) Turned ON/OFF forcibly with a peripheral device (GPP,HGP,PHP,PU) set to test mode.	Since a peripheral device can only be connected to the A3VCPU, individual A3VCPUs have different data from each other.
2	Relays turned ON by A3VCPU OS	(1) Used by the sequence program as a contact. (2) Monitored by a peripheral device (GPP,HGP,PHP,PU). ★(3) To turn OFF, either reset with the sequence program or reset forcibly with a peripheral device (GPP,HGP,PHP,PU) set to the test mode.	Since the OS of the A3CPU handles only its own special relays, individual A3VCPUs have different data in these special relays from each other.
3	Relays turned ON/OFF by A3VCPU OS	(1) Used by the sequence program as a contact. (2) Monitored by a peripheral device (GPP,HGP,PHP,PU). (3) User should not turn this relay ON/OFF.	
4	Relays turned ON by A3VTU OS	(1) Used by the sequence program as a contact. (2) Monitored by a peripheral device (GPP,HGP,PHP,PU). ★(3) To turn OFF, either reset with the sequence program or reset forcibly with a peripheral device (GPP,HGP,PHP,PU) set to the test mode.	Since the OS of the A3VTU provides special relay data to all of the A3VCPUs during operation, the data held by this type of relay is identical in all of the A3VCPUs. However, when the sequence program or the peripheral device (the peripheral device can be connected only to the A3VCPU) resets the data, the data held by individual A3VCPUs.
5	Relays turned ON/OFF by A3VTU [OPERATION/STOP]	(1) Used by the sequence program as a contact. (2) Monitored by a peripheral device (GPP,HGP,PHP,PU). (3) User should not turn this relay ON/OFF.	

POINT

(1) To reset the special relays using a sequence program in the procedure as indicated by an asterisk "★" in the above table, insert the circuit shown below into the sequence program and reset (OFF) the designated special relays by setting the reset execute instruction contact to ON.



(2) Because the peripheral device (GPP,HGP,PHP,PU) can be connected only to the A3VCPU, the monitor, forced ON/OFF, etc., can only be accessed via the A3VCPU. However, when operating the system in the majority operation mode, and if a special relay is forcibly turned ON/OFF, the A3VCPU which has been accessed for this operation has the data different from other A3VCPUs. If that data is connected to output (Y), the related A3VCPU will be dropped from operation.

(3) All special relays are reset when power is turned ON. Setting the reset switch at the front panel of a CPU module also resets all special relays.

(4) Relay numbers marked in the table with ✳ indicate special relays which are not transmitted to restored A3VCPU or the A3VCPU whose operation status has been change from PAUSE/STOP to RUN in the data memory transmit operation.

APP

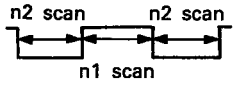
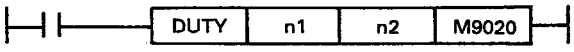
Number	Name	Stored Data	Description	Type Number
M9000	Fuse blown	0: Normal 1: Presence of fuse blow module	• Turned on when there is one or more output modules of which fuse has been blown. Remains on if normal status is restored.	4
M9002	I/O module verify error	0: Normal 1: Presence of error	• Turned on if the status of I/O module is different from entered status when power is turned on. Remains on if normal status is restored.	4
M9005	AC DOWN detection	0: AC is good 1: AC is down	• Turned on if power failure of within 20ms occurs. Reset when POWER switch is moved from OFF to ON position.	4
M9006	Battery low	0: Normal 1: Battery low	• Turned on when battery voltage reduces to less than specified. Turned off when battery voltage becomes normal.	5
*M9007	Battery low latch	0: Normal 1: Battery low	• Turned on when battery voltage reduces to less than specified. Remains on if battery voltage becomes normal.	4
*M9008	Self-diagnostic error	0: Absence of error 1: Presence of error	• Turned on when error is found as a result of self-diagnosis.	2
M9009	Annunciator detection	0: Absence of detection 1: Presence of detection	• Turned on when OUT F or SET F instruction is executed.Switched off when D9124 value is set to 0.	2
M9010	Operation error flag	0: Absence of error 1: Presence of error	• Turned on when operation error occurs during execution of application instruction. Turned off when error is eliminated.	3
*M9011	Operation error flag (latch)	0: Absence of error 1: Presence of error	• Turned on when operation error occurs during execution of application instruction. Remains on if normal status is restored.	2
M9012	Carry flag	0: Carry off 1: Carry on	• Carry flag used in application instruction.	2
M9016	Data memory clear flag	0: No processing 1: Output clear	• Clears all data memory (except special relays and special registers) in remote run mode from computer, etc. when M9016 is 1.	1
M9017	Data memory clear flag	0: No processing 1: Output clear	• Clears all unlatched data memory (except special relays and special registers) in remote run mode from computer, etc. when M9017 is 1.	1
M9020	User timing clock No. 0		• Relay which repeats on/off at intervals of predetermined scan. • When power is turned on or reset is performed, the clock starts with off. • Set the intervals of on/off [DUTY] instruction. 	5
M9021	User timing clock No. 1			
M9022	User timing clock No. 2			
M9023	User timing clock No. 3			
M9024	User timing clock No. 4			
M9036	Normally ON	ON OFF	• Used as dummy contacts of initialization and application instruction in sequence program. • M9036 and M9037 are switched on/off independently of the CPU RUN/STOP switch position. M9038 and M9039 are switched on/off in accordance with the RUN/STOP switch position, i.e. switched off when the switch is set to STOP. When the switch is set to other than STOP, M9038 is only switched on during 1 scan and M9039 is only switched off during 1 scan.	3
M9037	Normally OFF	ON OFF		
M9038	On only for 1 scan after run	ON OFF 1 scan		5
M9039	RUN flag (off only for 1 scan after run)	ON OFF 1 scan		
M9040	PAUSE enable coil	0: PAUSE disabled 1: PAUSE enabled	• When RUN key switch is at PAUSE position or remote pause contact has turned on and if M9040 is on, PAUSE mode is set and M9041 is turned on.	1
M9041	PAUSE status contact	0: During pause 1: Not during pause		3
M9042	Stop status contact	0: During stop 1: Not during stop		
*M9043	Sampling trace completion	0: During sampling trace 1: Sampling trace completion	• Turned on upon completion of sampling trace performed the number of times preset by parameter after [STRA] instruction is executed. Reset when [STRAR] instruction is executed.	
*M9044	Sampling trace	0→1 Same as the [STRA] 1→0 Same as the [STRAR]	• By setting M9044 ON/OFF, the [STRA] / [STRAR] instructions can be "pseudo-executed." (M9044 is turned ON/OFF forcibly by a peripheral device.) M9044: OFF → ON [STRA] instruction ON → OFF [STRAR] instruction For the sampling trace condition for this, the value contained in D9044 is used. {during scanning or timing → time (10 ms units)}	2

Table 8.1 Special Relay List (Continue)

Number	Name	Stored Data	Description	Type Number
*M9046	Sampling trace	0: Except during trace 1: During trace		3
*M9047	Sampling trace preparation	0: Sampling trace stop 1: Sampling trace start	• Sampling trace is not executed until M9047 is turned on. By turning off M9047, sampling trace is stopped.	1
M9051	CHG instruction execution disable	0: Disable 1: Enable		3
M9054	STEP RUN flag	0: Not during step run 1: During step run		
*M9055	Status latch completion flag	0: Uncompleted 1: Completed	• Turned on when status latch is completed. Turned off by reset instruction.	
M9056	Main program P, I set request	1: During P, I set request 0: Except during P, I set request	• Switch on upon completion of the transfer to another program (e.g. subprogram during RUN of the main program). Automatically switched off when P, I setting is complete.	3
M9057	Subprogram P, I set request	1: During P, I set request 0: Except during P, I set request		
M9091	Microcomputer sub-routine call error flag	0: No error 1: Error		2
M9092	Dual power supply module overheat error	0: Normal 1: Normal Overheated	• Set to ON when overheat of the dual power supply module is detected.	5
M9093	Dual power supply module malfunction	0: Normal 1: Malfunction or no AC supply	Set to ON when the dual power supply module has malfunctioned or ther is no AC supply.	5
M9096	A3VCPU (A) self-diagnosis error	0: No error 1: Error	Set to ON if the A3VCPU next to the A3VTU is the A3VCPU A and detects an error during self-diagnosis.	4
M9097	A3VCPU (B) self-diagnosis error	0: No error 1: Error	Set to ON if the next to the A3VCPU A is the A3VCPU B and detects an error during self-diagnosis.	4
M9098	A3VCPU (C) self-diagnosis error	0: No error 1: Error	Set to ON if the A3VCPU right end of the A3CPU is the A3VCPU C and detects an error during self-diagnosis.	4
M9099	A3VTU self-diagnosis error	0: No error 1: Error	Set to ON if the A3VTU detects an error during self-diagnosis.	4

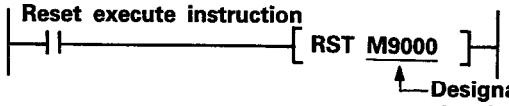
Table 8.1 Special Relay List

8.2 Special register list

	Type	Special Register Application	Remarks
1	Registers set by user	(1) Set with the sequence program. (2) Set with the peripheral device (GPP,HGP,PHP,PU) set to test mode.	• Peripheral device can be connected only to the A3VCPU. • When data is set in the A3VCPU by a peripheral device, individual A3VCPUs have different data from each other.
2	Registers set by A3VCPU OS	(1) The register data is read and used by the sequence program. (2) Monitored by the peripheral device (GPP,HGP,PHP,PU). ★ (3) To clear the data in a register, either reset with the sequence program or set the peripheral device (GPP,HGP,PHP,PU) to the test mode and forcibly reset it.	• Since the OS of the A3CPU handles only its own special registers, individual A3VCPUs have different data on this type of special registers from each other.
3	Registers set/reset by A3VCPU OS	(1) The register data is read and used by the sequence program. (2) Monitored by the peripheral device (GPP,HGP,PHP,PU). (3) User should not set the data to this register.	
4	Registers set by A3VTU OS	(1) The register data is read and used by the sequence program. (2) Monitored by the peripheral device (GPP,HGP,PHP,PU). ★ (3) To clear the data in a register, either reset with the sequence program or set the peripheral device (GPP,HGP,PHP,PU) to the test mode and forcibly reset it.	• Since the OS of the A3VTU provides special register data to all of the A3VCPUs during operation, the data held by this type of register is identical in all of the A3VCPUs. • However, when the sequence program or the peripheral device (the peripheral device can be connected only to the A3VCPU) resets the data, the data held by individual A3VCPUs.
5	Registers set/reset by A3VTU [OPERATION/STOP]	(1) The register data is read and used by the sequence program. (2) Monitored by the peripheral device (GPP,HGP,PHP,PU). (3) User should not set the data to this register.	

POINT

(1) To clear the special registers using a sequence program in the procedure as indicated by an asterisk "★" in the above table, insert the circuit shown below into the sequence program and clear the designated special registers by setting the reset execute instruction contact to ON.



Designate the M number that is to be reset.

(2) Because the peripheral device (GPP,HGP,PHP,PU) can be accessed only via the A3VCPU, the monitor, data write, etc., can only be connected to the A3VCPU. However, when operating the system in the majority operation mode, and if the data is written, the A3VCPU which has been accessed for this operation has the data different from other A3VCPUs. If that data is connected to output (Y), the related A3VCPU will be dropped from operation.

(3) All special registers are cleared when power is turned ON. Setting the reset switch at the front panel of a CPU module also clears all special registers.

(4) Register numbers marked in the table with * indicate special registers which are not transmitted to restored A3VCPU or the A3VCPU whose operation status has been change from PAUSE/STOP to RUN in the data memory transmit operation.

APP

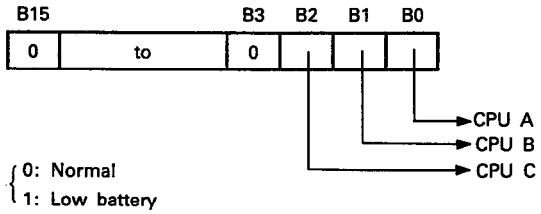
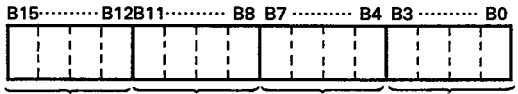
Number	Name	Stored Data	Description	Type Number
D9000	Fuse blown	Fuse blow module number	• When fuse flow modules are detected, the lowest number of detected units is stored in hexadecimal. (Example: When fuses of Y50 to 6F output modules have blown, "50" is stored in hexadecimal) The module number monitored by the peripheral is hexadecimal. (Cleared when all contents of D9100 to D9107 are reset to 0.)	3
D9002	I/O unit verify error	I/O module verify error module number	• If I/O module data is different from data entered are detected when the power is turned on, the first I/O number of the lowest number module among the detected modules stored in hexadecimal. (Storing method is the same as that of D9000.) The module number monitored by the peripheral is hexadecimal. (Cleared when all contents of D9116 of D9123 are reset to 0.)	3
D9005	AC DOWN counter	AC DOWN time count	• 1 is added each time input voltage becomes 80% or less of rating while the CPU unit is performing operation, and the value is stored in BIN code.	4
D9006	Low battery	Display CPU containing low battery	• When a battery is determined to be low, the bits corresponding to the CPU are set in D9006 as shown below.  	5
*D9008	Self-diagnostic error	Self-diagnostic error number	• When error is found as a result of self-diagnosis, error number is stored in BIN code.	2
D9009	Annunciator detection	F number at which external failure has occurred	• When one of F0 to 255 is turned on by [OUT F] or [SET F], the F number, which has been detected earliest among the F numbers which have turned on, is stored in BIN code. • D9009 can be cleared by [RST F] or [LEDR] instruction or moving INDICATOR RESET switch on CPU front to ON position. If another F number has been detected, the clearing of D9009 causes the next number to be stored in D9009. When D9125 to D9132 are cleared, D9009 is cleared.	3
*D9010	Error step	Step number at which operation error has occurred	• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Thereafter, each time operation error occurs, the contents of D9010 are renewed.	3
*D9011	Error step	Step number at which operation error has occurred	• When operation error has occurred during execution of application instruction, the step number, at which the error has occurred, is stored in BIN code. Since storage into D9011 is made when M9011 changes from off to on, the contents of D9010 cannot be renewed unless M9011 is cleared by user program.	3
D9014	I/O control mode	I/O control mode number	• The set mode is represented as follows: 3 = I/O in refresh mode	2

Table 8.2 Special Register List (Continue)

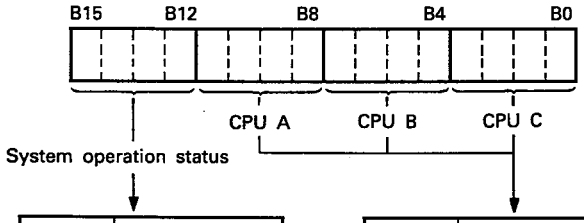
APP

<table>
<tr><th>Number</th><th>Name</th><th>Stored Data</th><th>Description</th><th>Type Number</th></tr>
<tr><td>D9015</td><td>CPU operating states</td><td>Operating states of CPU</td><td>
• The operating states of CPU as shown below are stored in D9015.


<table>
<tr><td colspan="2">CPU RUN/STOP switch: Remains unchanged in remote run/stop mode.</td></tr>
<tr><td>0</td><td>RUN</td></tr>
<tr><td>1</td><td>STOP</td></tr>
<tr><td>2</td><td>PAUSE*1</td></tr>
<tr><td>3</td><td>STEP RUN</td></tr>
</table>
<table>
<tr><td colspan="2">Remote RUN/STOP by parameter setting</td></tr>
<tr><td>0</td><td>RUN</td></tr>
<tr><td>1</td><td>STOP</td></tr>
<tr><td>2</td><td>PAUSE*1</td></tr>
</table>
<table>
<tr><td colspan="2">Status in program</td></tr>
<tr><td>0</td><td>Except below</td></tr>
<tr><td>1</td><td>STOP instruction execution</td></tr>
</table>
<table>
<tr><td colspan="2">Remote RUN/STOP by computer</td></tr>
<tr><td>0</td><td>RUN</td></tr>
<tr><td>1</td><td>STOP</td></tr>
</table>
*1 When the CPU is in RUN mode and M9040 is off, the CPU remains in RUN mode if changed to PAUSE mode.
POINT
D9015 actually contains the operation status of the CPU and cannot provide data to determine the status of the A3VTS system.
To determine the status of the A3VTS system, check D9095.
</td><td>3</td></tr>
</table>

Table 8.2 Special Register List (Continue)

APP

<table>
<tr><th>Number</th><th>Name</th><th>Stored Data</th><th>Description</th><th>Type Number</th></tr>
<tr><td>D9016</td><td>Program number</td><td>0: Main program (ROM)
1: Main program (RAM)
2: Subprogram (RAM)</td><td>• Indicates which sequence program is urn presently. One value of 0 to 2 is stored in BIN code.</td><td>3</td></tr>
<tr><td>D9017</td><td>Scan time</td><td>Minimum scan time (per 10ms)</td><td>• If scan time is smaller than the content of D9017, the value is newly stored at each END. Namely, the minimum value of scan time is stored into D9017 in BIN code.</td><td>3</td></tr>
<tr><td>D9018</td><td>Scan time</td><td>Scan time (per 10ms)</td><td>• Scan time is stored in BIN code at each END and always rewritten.</td><td>3</td></tr>
<tr><td>D9019</td><td>Scan time</td><td>Maximum scan time (per 10ms)</td><td>• If scan time is larger than the content of D9019, the value is newly stored at each END. Namely, the maximum value of scan time is stored into D9019 in BIN code.</td><td>3</td></tr>
<tr><td>D9072</td><td>PC communication check</td><td>Data written from AJ71C24</td><td>• In the self loopback test if the AJ71C24, the data is written by the AJ71C24 and read for verification.</td><td>5</td></tr>
<tr><td>D9090</td><td>Microcomputer sub-routine INPUT data area head device No.</td><td>Depends on the microcomputer package</td><td>• For details, refer to the microcomputer package manual.</td><td>1</td></tr>
<tr><td>D9091</td><td>Error code generated for microcomputer sub-routine call</td><td>Depends on the microcomputer package</td><td>• For details, refer to the microcomputer package manual.</td><td>2</td></tr>
<tr><td>*D9094</td><td>I/O address of input module to be replaced</td><td>Value of the head I/O address of the replacement input module excepting the least significant digit</td><td>• This register is used to latch input data yet to be communicated, when an input module is exchanged during RUN. The number excluding the least significant digit if the address is set in hexadecimal. The initial value is "−1" (FFFFH); reset to "−1" after module replacement.</td><td>1</td></tr>
<tr><td>D9095</td><td>Operation status of the A3VTS system and A3VCPUs</td><td>Contents of the operational status in four hexadecimal digits</td><td>• This register monitors the operation status of the A3VTS system and A3VCPUs.
 

<table>
<tr><th>Value (H)</th><th>Operation Status</th></tr>
<tr><td>A</td><td>RUN</td></tr>
<tr><td>B</td><td>STEP-RUN</td></tr>
<tr><td>C</td><td>PAUSE</td></tr>
<tr><td>D</td><td>STOP</td></tr>
<tr><td>E</td><td>Error</td></tr>
</table>
<table>
<tr><th>Value (H)</th><th>Operation Status</th></tr>
<tr><td>0</td><td>RUN</td></tr>
<tr><td>1</td><td>Standby</td></tr>
<tr><td>2</td><td>STEP-RUN</td></tr>
<tr><td>3</td><td>PAUSE</td></tr>
<tr><td>4</td><td>STOP</td></tr>
<tr><td>5</td><td>WAIT</td></tr>
<tr><td>6</td><td>Error</td></tr>
<tr><td>7</td><td>No operation right</td></tr>
</table></td><td>5</td></tr>
</table>

Table 8.2 Special Register List (Continue)

APP

Number	Name	Stored Data	Description	Type Number
D9096	CPU (A) self-diagnosis error	Self-diagnosis error number	• The number of an error generated during a self- diagnosis by CPU A is stored in BIN code. • D9096 is cleared when D9008 of CPU A is cleared.	5
D9097	CPU (B) self-diagnosis error	Self-diagnosis error number	• The number of an error generated during a self- diagnosis by CPU B is stored in BIN code. • D9097 is cleared when D9008 of CPU B is cleared.	5
D9098	CPU (C) self-diagnosis error	Self-diagnosis error number	• The number of an error generated during a self- diagnosis by CPU C is stored in BIN code. • D9098 is cleared when D9008 of CPU C is cleared.	5
D9099	A3VTU self-diagnosis error	Self-diagnosis error number	• The number of an error generated during a self- diagnosis by A3VTU is stored in BIN code.	4
D9100 D9101 D9102 D9103 D9104 D9105 D9106 D9107	Fuse blown module	Bit pattern in modules of 16 points of fuse blow modules	• Output module numbers (in units of 16 points), of which fuses have blown, are entered in bit pattern. (Preset output number when parameter setting has been performed.) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 D9100 0 0 0 1 (YC0) 0 0 0 1 (YB0) 0 0 0 0 0 0 0 0 D9101 1 (Y1F0) 0 0 0 0 0 1 (Y1A) 0 0 0 0 0 0 0 0 0 D9107 0 0 0 0 1 (Y7B0) 0 0 0 0 0 0 0 1 (Y730) 0 0 0 Indicates fuse blow. (If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)	4
D9116 D9117 D9118 D9119 D9120 D9121 D9122 D9123	I/O module verify error	Bit pattern in modules of 16 points of verify error modules	• When I/O module data is different from those entered at power-on have been detected, the I/O module numbers (in units of 16 points) are entered in bit pattern. (Preset I/O module numbers when parameter setting has been performed.) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 D9116 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 (X/Y0) D9117 0 0 0 0 0 0 0 1 (X/Y180) 0 0 0 0 0 0 0 0 D9123 0 1 (X/Y7F0) 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 Indicates I/O unit verify error. (If normal status is restored, clear is not performed. Therefore, it is required to perform clear by user program.)	
D9124	Annunciator detection quantity	Annunciator detection quantity	• When one of F0 to 255 is turned on by [OUT F□] or [SET F□], 1 is added to the contents of D9124. When [RST F□] or [LED R] instruction is executed, 1 is subtracted from the contents of D9124. (For A3CPU, it can be performed by use of INDICATOR RESET switch on front face of CPU module.) • Quantity, which has been turned on by [OUT F□] or [SET F□] is stored into D9124 in BIN code. The value of D9124 is maximum 8.	

Table 8.2 Special Register List (Continue)

APP

<table>
<tr><th>Number</th><th>Name</th><th>Stored Data</th><th>Description</th><th>Type Number</th></tr>
<tr>
<td>D9125
D9126
D9127
D9128
D9129
D9130
D9131
D9132</td>
<td>Annunciator detection number</td>
<td>Annunciator detection number</td>
<td>
• When one of F0 to 255 is turned on by [OUT F ⋯] or [SET F ⋯], F number, which has turned on, is entered into D9125 to D9132 in due order in BIN code.
• F number, which has been turned off by [RST F ⋯], is erased from D9125 to D9132, and the contents of data registers succeeding the data register, where the erased F number was stored, are shifted to the preceding data registers.
• By executing [LED R] instruction, the contents of D9125 to D9132 are shifted upward by one. (For A3NCPU, it can be performed by use of INDICATOR RESET switch on front of CPU unit.)
• When there are 8 annunciator detections, the 9th one is not stored into D9125 to 9132 even if detected.

<table>
<tr><th></th><th>SET F50</th><th>SET F25</th><th>SET F19</th><th>RET F25</th><th>SET F15</th><th>SET F70</th><th>SET F65</th><th>SET F38</th><th>SET F110</th><th>SET F151</th><th>SET F210</th><th>LED R</th><th>INDICATOR RESET</th><th></th></tr>
<tr><td>D9009</td><td>0</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>99</td><td>15</td></tr>
<tr><td>D9124</td><td>0</td><td>1</td><td>2</td><td>3</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>8</td><td>8</td><td>7</td></tr>
<tr><td>D9125</td><td>0</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>50</td><td>99</td><td>15</td></tr>
<tr><td>D9126</td><td>0</td><td>0</td><td>25</td><td>25</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>99</td><td>15</td><td>70</td></tr>
<tr><td>D9127</td><td>0</td><td>0</td><td>0</td><td>99</td><td>0</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>15</td><td>70</td><td>65</td></tr>
<tr><td>D9128</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>70</td><td>70</td><td>70</td><td>70</td><td>70</td><td>70</td><td>65</td><td>38</td></tr>
<tr><td>D9129</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>65</td><td>65</td><td>65</td><td>65</td><td>65</td><td>38</td><td>110</td></tr>
<tr><td>D9130</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>38</td><td>38</td><td>38</td><td>38</td><td>110</td><td>151</td></tr>
<tr><td>D9131</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>110</td><td>110</td><td>110</td><td>151</td><td>210</td></tr>
<tr><td>D9132</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>151</td><td>151</td><td>210</td><td></td></tr>
</table>

*When F50 is ON, F210 and F50 varies depending on sequence program timing.
</td>
<td>3</td>
</tr>
</table>

Table 8.2 Special Register List

APP

APPENDIX 9 Instructions Permissible to Use with the AD51E when Used in the A3VTS System

Not all AD51E functions (instructions) can be used when using the AD51E in the A3VTS system. The following provides details concerning the usage of these instructions.

(1) Basic instructions
All basic instructions can be used.

(2) System subroutines
Instructions that communicate with the CPU cannot be used in system subroutines.
The righthand column of the following table provides information concerning those instructions that may be used with the A3VTS system. Those marked with "○" may be and those marked with "×" may not be used.

	System Subroutine		Function	Channel	Address	Usable in the A3VTS System
1	SAI		ASCII (hexadecimal) to BIN	0	8060H	○
2	SIA		BIN to ASCII (hexadecimal)	0	8063H	○
3	SAN		ASCII (decimal) to BIN	0	8072H	○
4	SNA		BIN to ASCII (decimal)	0	8075H	○
5	SAF		ASCII to real numbers	0	8066H	○
6	SFA		Real numbers to ASCII	0	8069H	○
7	SBF		Integers to real numbers	0	806CH	○
8	SFB		Real numbers to integers	0	806FH	○
9	SBD4		BIN to 4-digit BCD	0	8042H	○
10	SDB4		4-digit BCD to BIN	0	8045H	○
11	SBD6		BIN to 6-digit BCD	0	8048H	○
12	SDB6		6-digit BCD to BIN	0	804BH	○
13	SBA		BIN addition (24 bits)	0	804EH	○
14	SBS		BIN subtraction (24 bits)	0	8051H	○
15	SBM		BIN multiplication (24 bits)	0	8054H	○
16	SBW		BIN division (24 bits)	0	8057H	○
17	SCA	— B	Write to clock device (year, month, day, hour, minute, second)	0	803CH	○
18	SCB	— B	Read from clock device (year, month, day, hour, minute, second)	0	803FH	○
19	SPC	— B	Programmable controller CPU discrimination	0	8078H	×
20	SKC	— B	RUN/STOP check of programmable controller CPU	0	8030H	×

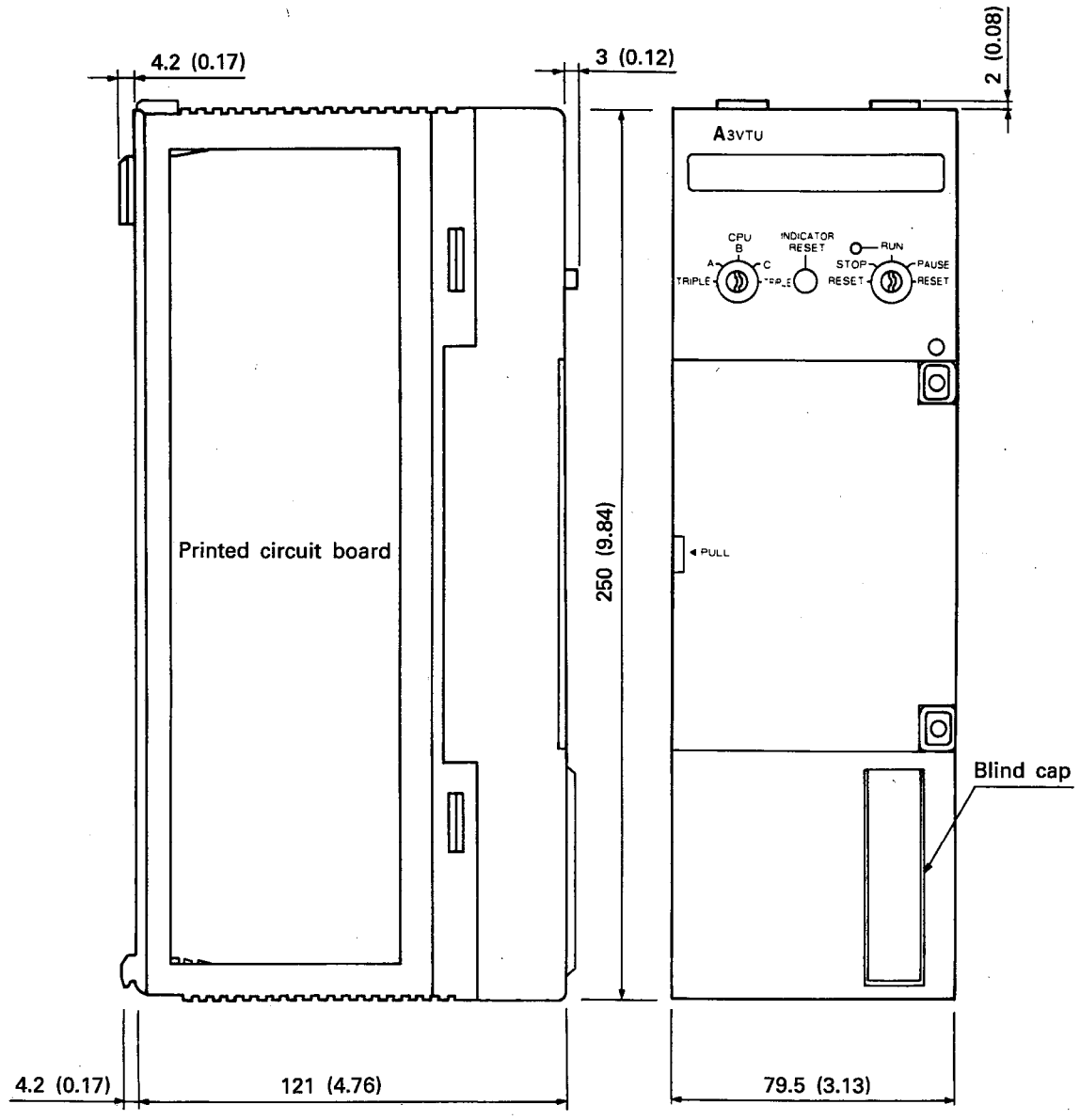
APP

	System Subroutine		Function	Channel	Address	Usable in the A3VTS System
21	SKR	— B	Programmable controller CPU remote RUN	0	8033H	×
22	SKP	— B	Programmable controller CPU remote STOP	0	8036H	×
23	SRB	A B	Receives data of a designated byte length sent to a designated channel.	0	8009H	○
24	SWB	A B	Receives data of a designated byte length from a designated channel.	0	800CH	○
25	SRC		Reads data byte size received via a designated channel.	0	800FH	○
26	SRF		Reads amount of bytes open in receive buffer of a designated channel.	0	8012H	○
27	SHX	— B	Controls data communication at a designated channel using the Xon/Xoff code.	0	8015H	○
28	SHD	— B	Controls data communication at a designated channel using the DR terminal.	0	8018H	○
29	SAE		Converts all data communicated via a designated channel to EBCDIC code.	0	801EH	○
30	SEA		Does not convert data communicated via a designated channel.	0	8021H	○
31	STC		Reads the number of bytes remaining in a buffer for a designated channel.	0	801BH	○
32	SRP		Reads the status of a designated channel.	0	8027H	○
33	SR2		Reads buffer memory.	0	8000H	○
34	SW2		Writes to buffer memory.	0	8003H	○
35	SADR		Reads the data memory of the programmable controller CPU.	0	807BH	×
36	SADW		Writes to data memory of the programmable controller CPU.	0	807EH	×
37	SADT		Writes to data memory of the programmable controller CPU at random.	0	8081H	×
38	SADM0		Records data read at random from data memory of the programmable controller CPU.	0	8084H	×
39	SADM1		Reads from data memory of the programmable controller CPU at random.	0	8087H	×
40	SAAR		Reads sequence program.	0	808AH	×
41	SAAW		Writes sequence program.	0	808DH	×
42	SAPR		Reads parameters of programmable controller CPU.	0	8090H	×
43	SAPW		Writes parameters of programmable controller CPU.	0	8093H	×
44	SAPS		Requests for analysis of CPU parameters.	0	8096H	×
45	SIT		Generates interrupt to programmable controller CPU.	0	802AH	×
46	SIR		Reads error code.	0	8024H	○
47	SC2		Sets retry time of SR2/SW2.	0	8006H	○

APP

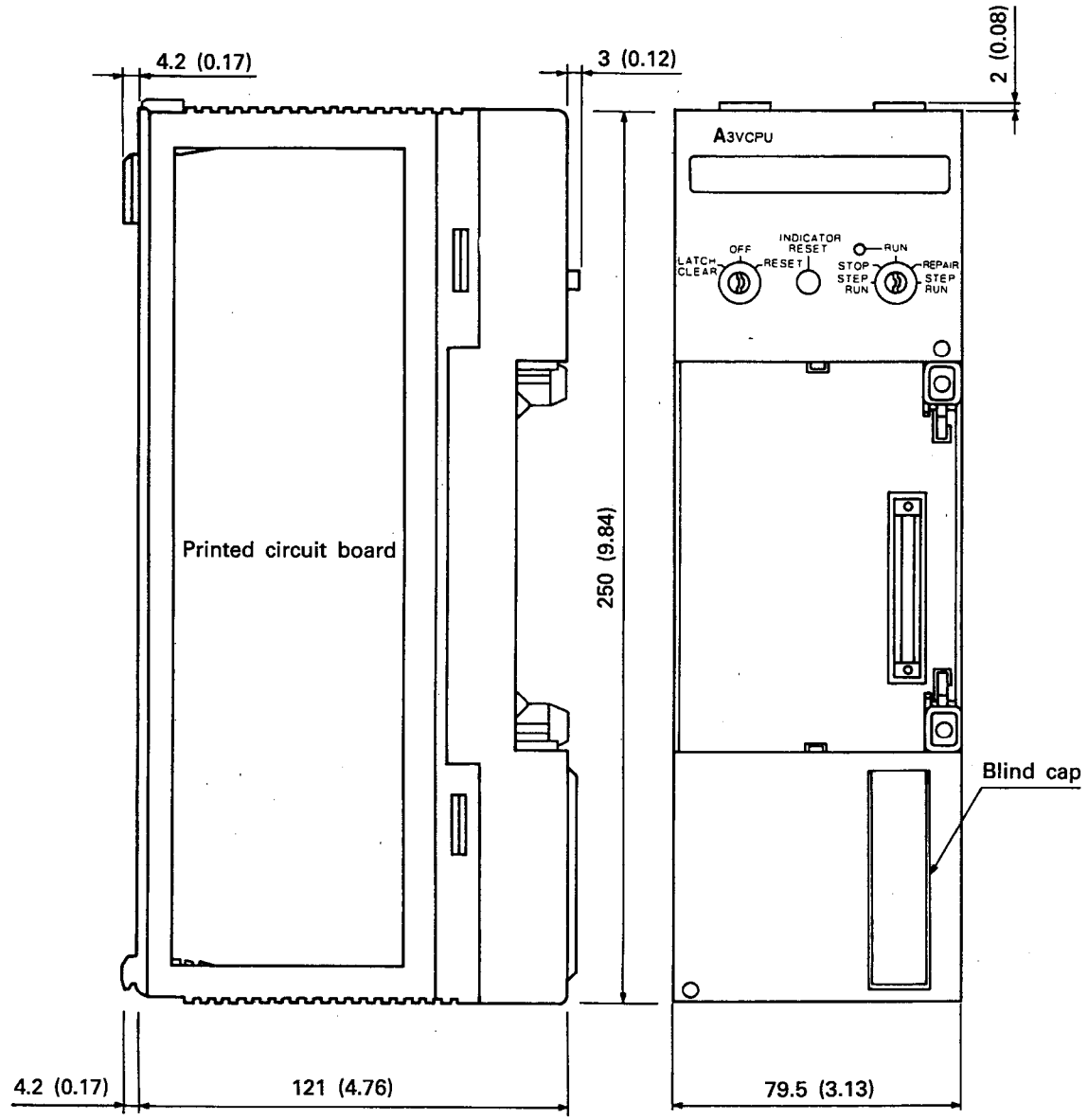
APPENDIX 10 Dimensions

10.1 Majority module (A3VTU)



Unit: mm (inch)

10.2 CPU module (A3VCPU)

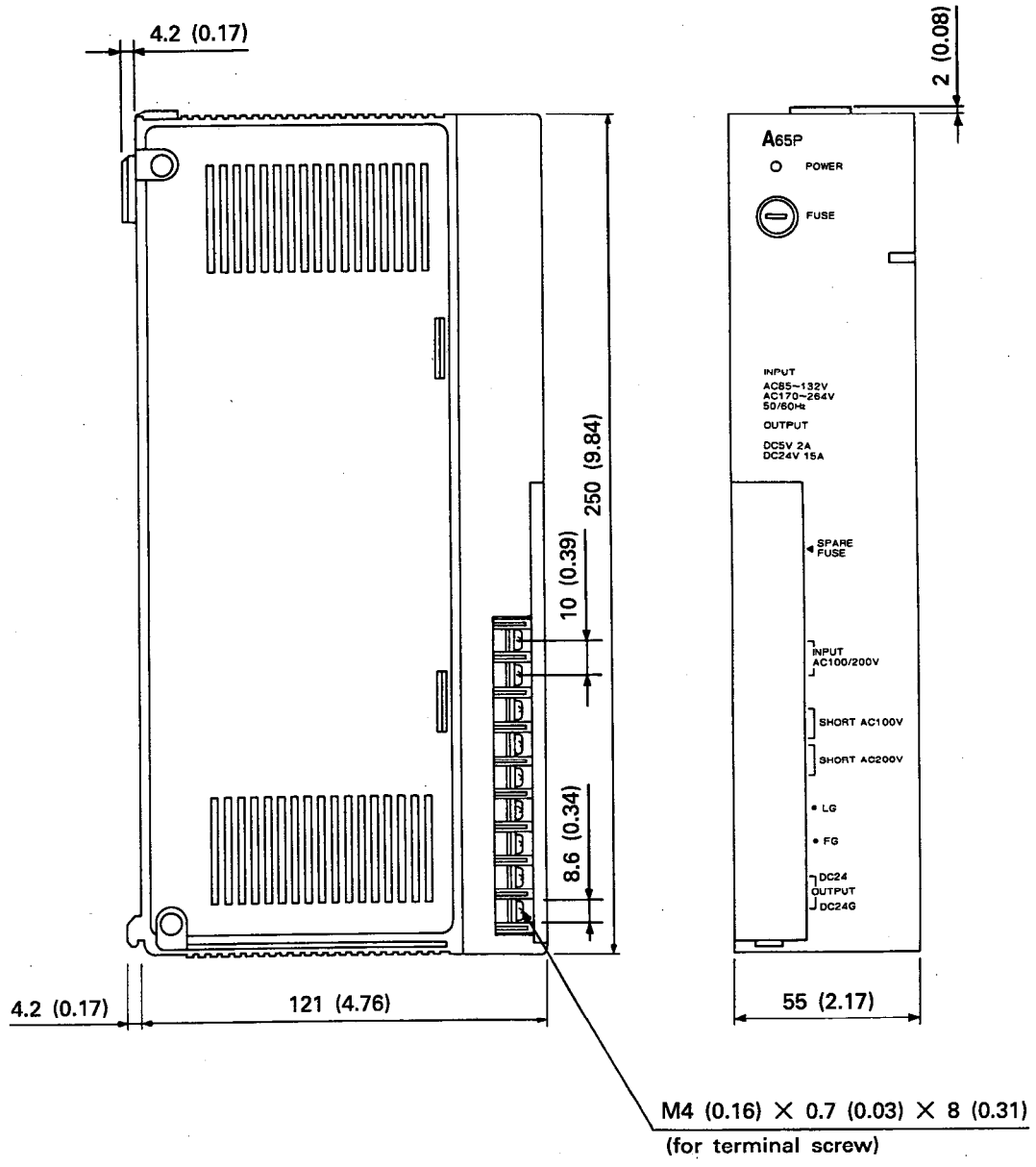


Unit: mm (inch)

APP

10.3 Power supply modules

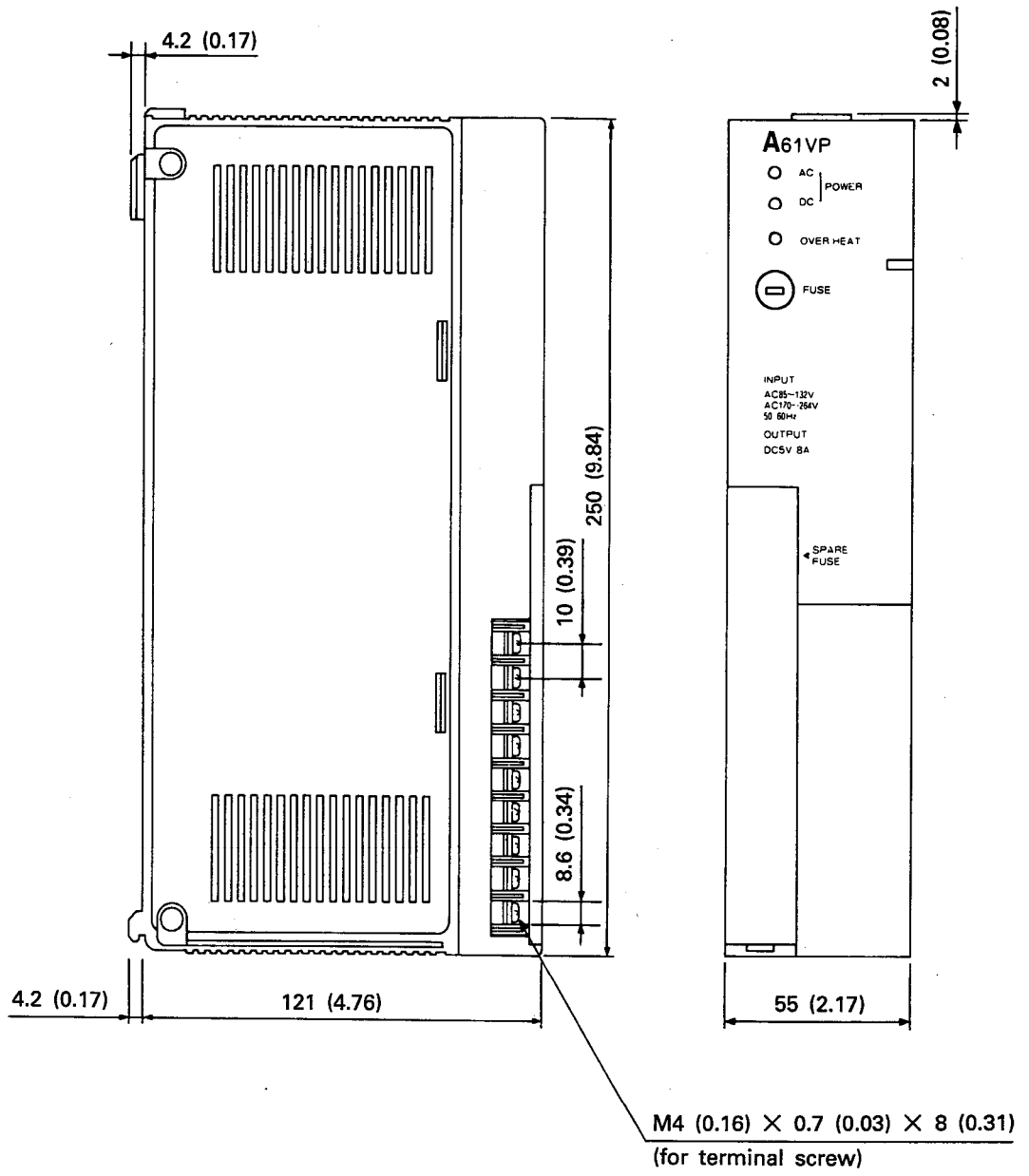
(1) Type A61P, A62P, A63P, A65P power supply modules



Unit: mm (inch)

APP

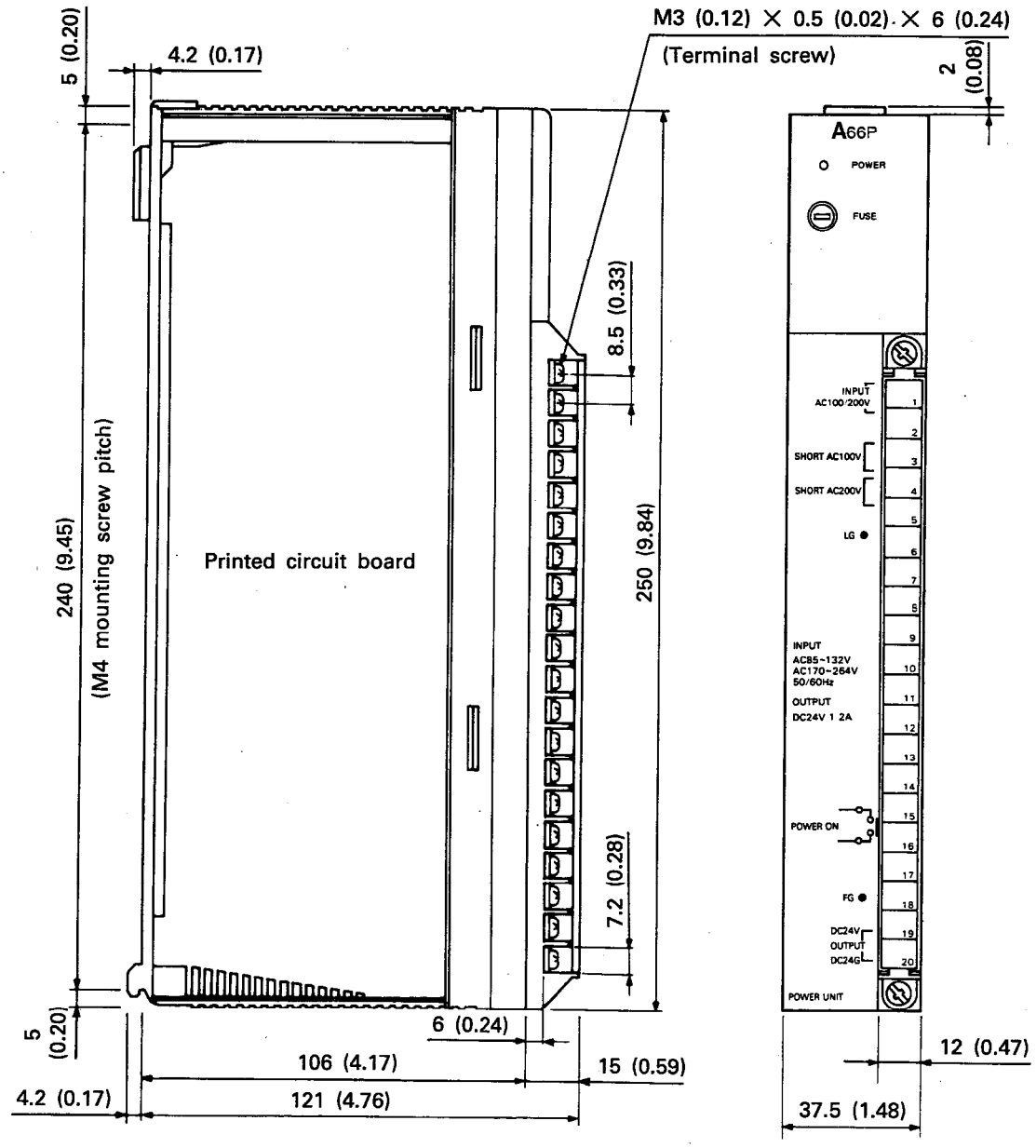
(2) Type A61VP power supply module



Unit: mm (inch)

APP

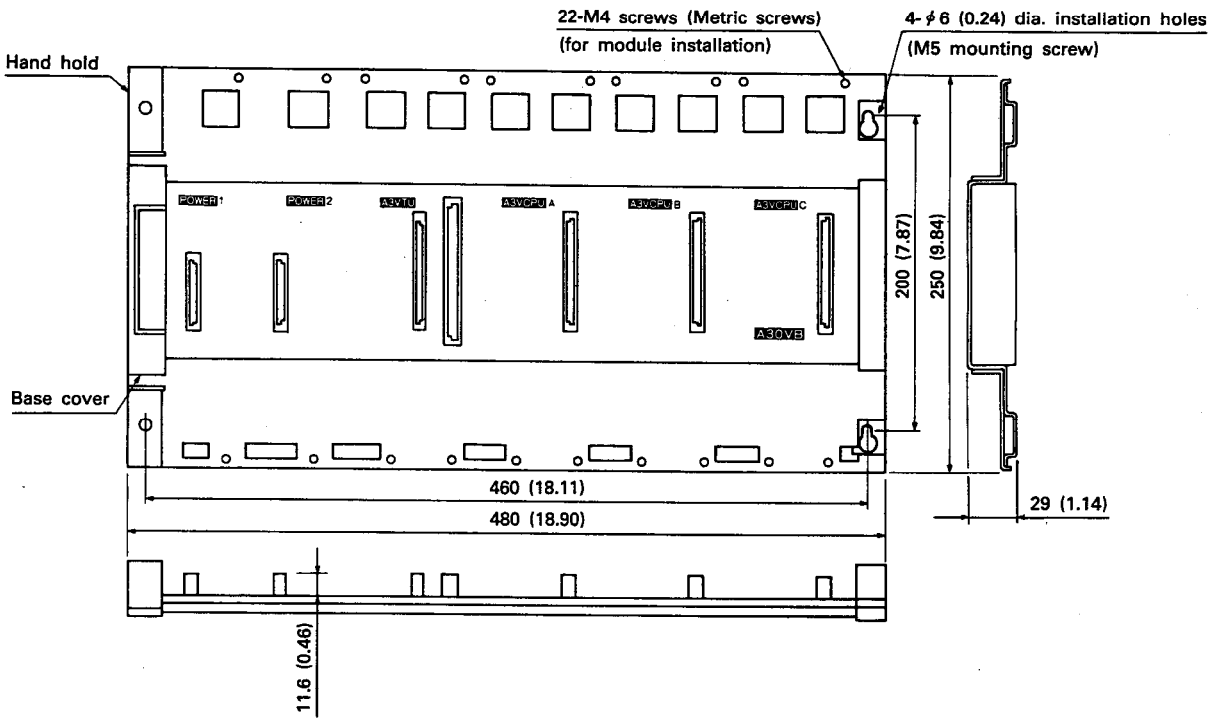
(3) Type A66P power supply module



Unit: mm (inch)

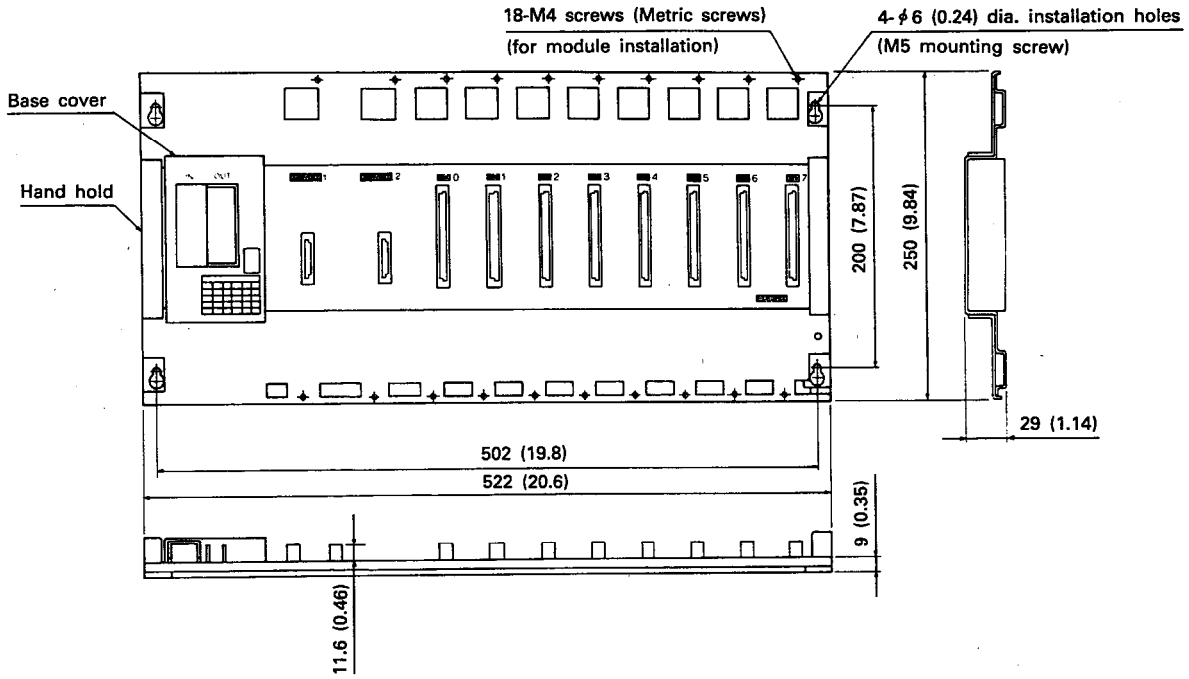
APP

10.4 Basic base unit (A30VB)



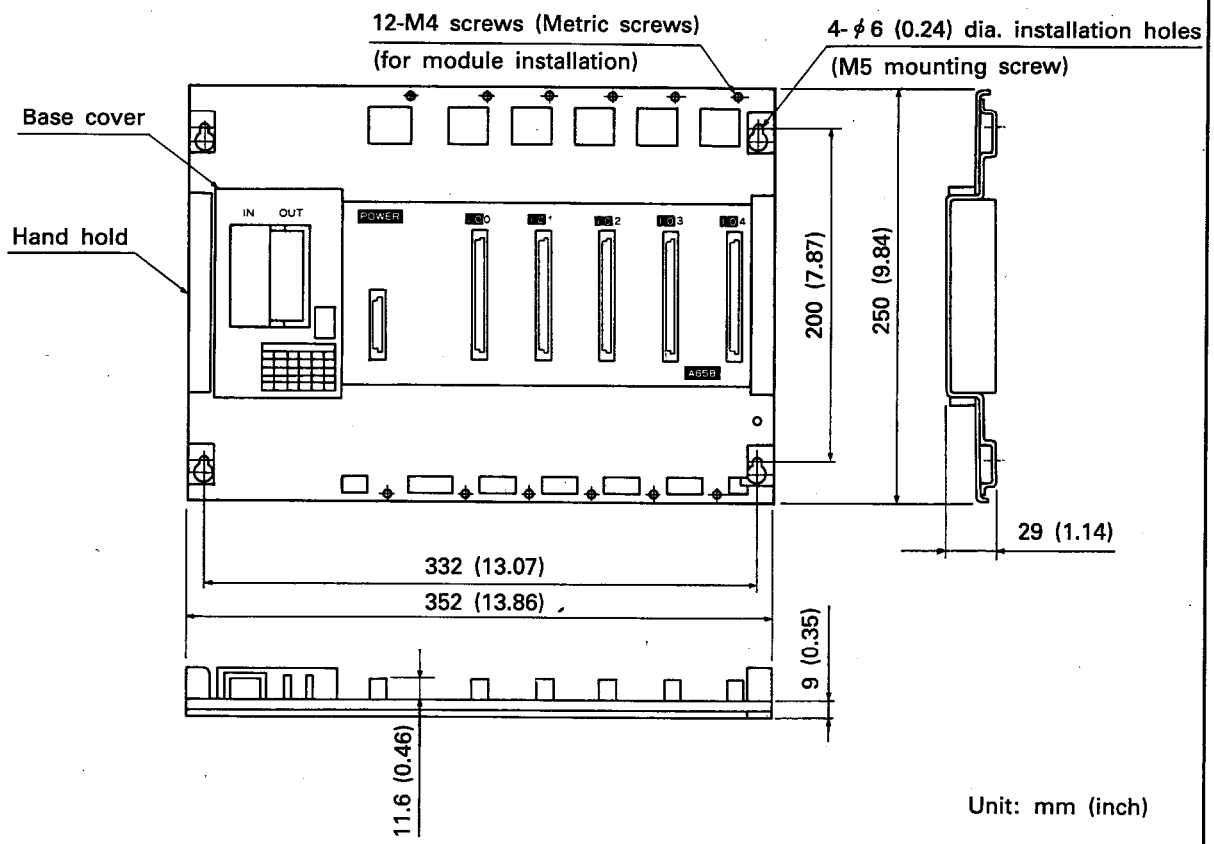
Unit: mm (inch)

10.5 Extension base units



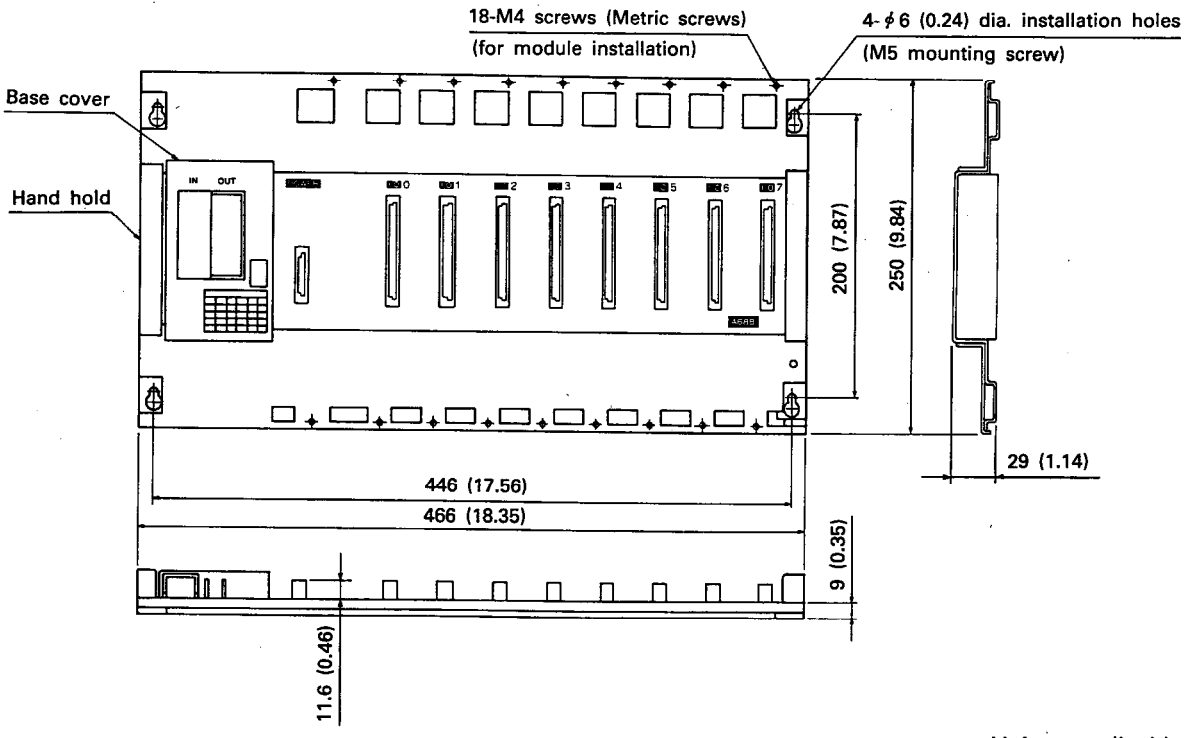
Unit: mm (inch)

(2) Type A65B base unit



Unit: mm (inch)

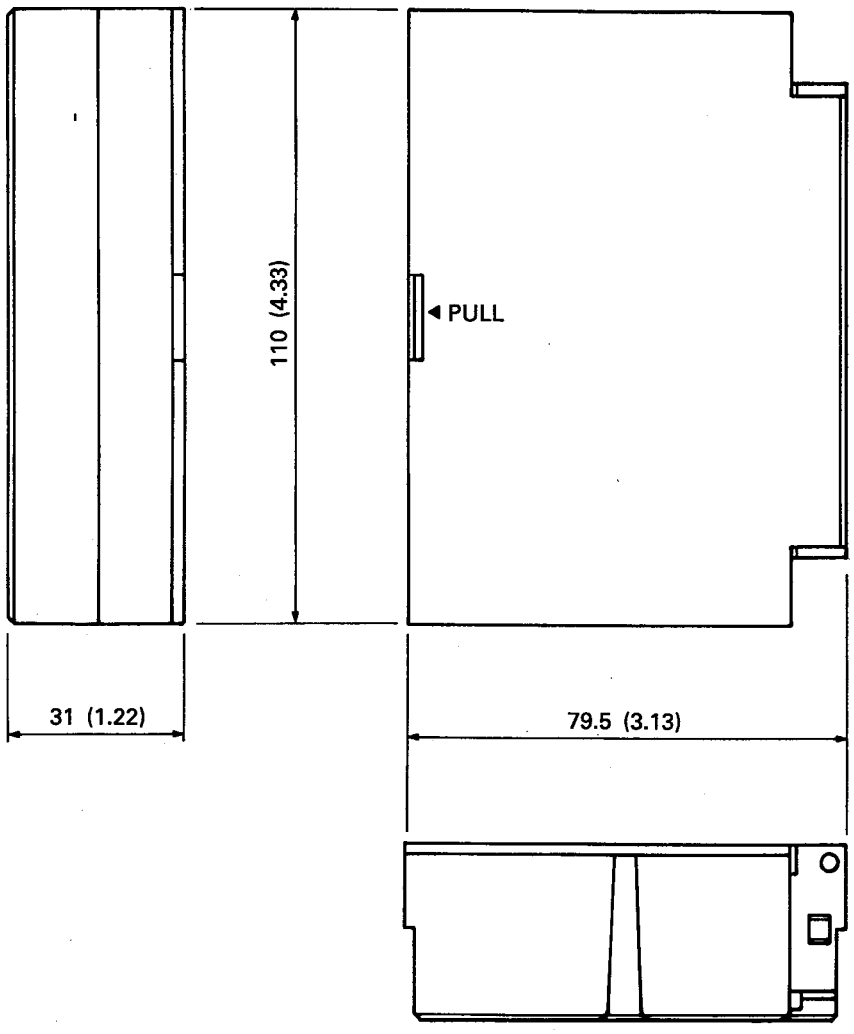
(3) Type A68B base unit



Unit: mm (inch)

APP

10.6 Memory cassettes (A3NMCA-□)



Unit: mm (inch)

APPENDIX 11 Processing Time List

The processing times required for instructions used in the A3VTS system is shown in the table provided on subsequent pages.

(1) Time required for refreshing is not included in the times shown for each instruction.
To calculate the amount of time required for the sequence program, it is necessary to add the refresh processing time that occurs following the execution of the [END] instruction. The following is an example of calculations made to determine the amount of time required for the sequence program and refresh processing.

Sequence program processing time =
(Processing time for a particular instruction) + [END] processing time +
Calculated from table Refresh processing time

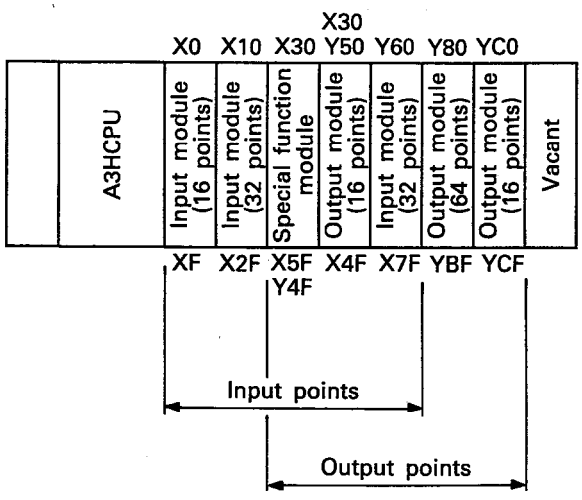
([END] processing time)

[END] processing time =
time required to execute [END] instruction +
the count processing time at T/C [END]

(Refresh processing time)

$$\text{Refresh time} = \frac{\text{Input points} + \text{output points}}{16} \times 111.4\ [\mu\text{sec}]$$

The number of input points and output points are determined by the location of the I/O modules and special function modules.



POINT

The number of I/O points for the special function module is 32 each for inputs and outputs.
Example) X30 to X4F, Y30 to Y4F

APP

The number of input points is the total of points of all modules installed between the input or special function module input/output installed in the lowest numbered slot and the one in the highest numbered slot.

Example) In the example shown in the above figure, the total number of points of the modules located between X0 and X7F is

Input points = 16 + 32 + 32 + 16 + 32 = 128 points

The number of output points is the total of points of all modules installed between the output or special function module input/output installed in the lowest numbered slot and the one in the highest numbered slot.

Example) In the example shown in the above figure, the total number of points of the modules located between Y30 and YCF is

Output points = 32 + 16 + 32 + 64 + 16 = 160 points

The following is an example of how refresh time is calculated.

Calculation of refresh time

The amount of refresh time required can be shortened by installed the input, output, and special function modules in blocks as shown in Fig. 7.1.

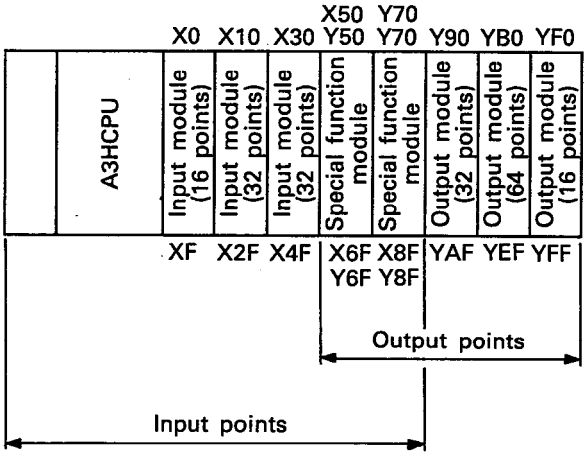


Fig. 7.1 Example of Modules Installed by Type

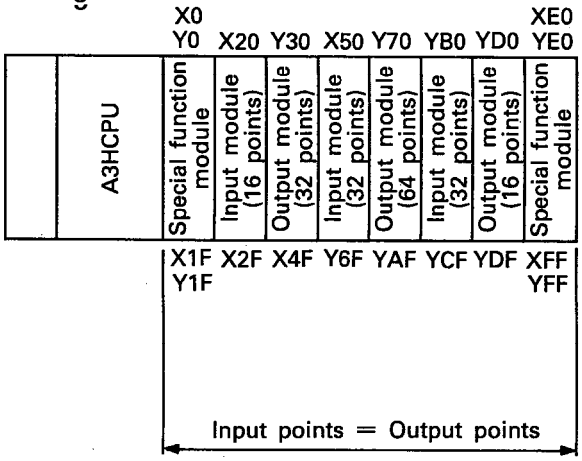


Fig. 7.2 Example of Modules Installed at Random

Refresh time for Fig. 7.1

Input points = 16 + 32 + 32 + 32 + 32 = 144 points

Output points = 32 + 32 + 32 + 64 + 16 = 176 points

$$\text{Refresh time} = \frac{144 + 176}{16} \times 111.4 = 2228 \ [\mu\text{sec}]$$

Refresh time for Fig. 7.2

Input points = Output points =

32 + 16 + 32 + 32 + 64 + 32 + 16 + 32 = 256 points

$$\text{Refresh time} = \frac{256 + 256}{16} \times 111.4 = 3564.8 \ [\mu\text{sec}]$$

APP

(2) Non-execution times for basic and application instructions

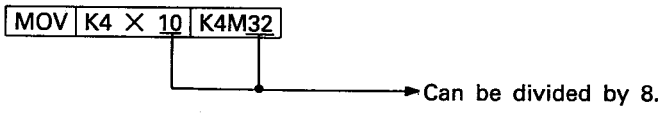
Non-execution processing time = (number of instruction steps + 1) X 1.0 (μsec)

(3) Processing time for Type A and Type B of basic and application instructions

Type A

Type A are those instructions that meet all of the following criteria.

1) Indexing qualifiers are not used.
2) File register is not used.
3) The number of digits designated for use when using bit devices is either K4 or K8.
   (K4 for 16-bit instructions
   K8 for 32-bit instructions)
4) The designated device numbers used in bit devices can be divided by "8".
   Example)



Type B

Type B are those instructions that meet any of the following criteria.

1) Indexing qualifiers are used.
2) File register is used.
3) The number of digits designated for use when using bit devices is either K1 to K3 and K5 to K7.
4) The designated device numbers used in bit devices cannot be divided by "8".
   Example)

APP

11.1 Sequence instructions

Instruction	Condition (Device)					Processing Time (μ sec)	Comments
LD LDI AND	X					1.0	
ANI OR ORI	Y, M. L, S, B, F, T, C					1.0	
ANB	———						
ORB	———						
OUT	Y	ON/OFF status unchanged {OFF to OFF, ON to ON}				1.0	
		ON/OFF status changed {OFF to ON, ON to OFF}				1.0	
	M (Excluding special M), L, B, S	ON/OFF status unchanged {OFF to OFF, ON to ON}				1.0	
		ON/OFF status changed {OFF to ON, ON to OFF}				1.0	
	Special M					37.1	
	F	Not executed				61.1	
		Executed				663.1	
	T	Instruction execution time				1.0	
		Processing time at END	Not executed			38.0	
			Executed	After time-up		11.2	
				When to be added	K	23.8	
					D	29.5	
	C	Instruction execution time				1.0	
		Processing time at END	Not executed			0	
			Executed	When not counted		0	
				After count-up		0	
				When to be counted	K	25.1	
					D	29.5	
SET	Y	Not executed				1.0	
		Executed	ON/OFF status unchanged (ON to ON)			1.0	
			ON/OFF status changed (OFF to ON)			1.0	
	M, L, S	Not executed				1.0	
		Executed	ON/OFF status unchanged (ON to ON)			1.0	
			ON/OFF status changed (OFF to ON)			1.0	
	Special M, B	Not executed				3.0	
		Executed				32.3	
	F	Not executed				3.0	
		Executed				637.7	

APP

Instruction	Condition (Device)			Processing Time (μsec)	Comments
RST	Y	Not executed		1.0	
		Executed	ON/OFF status unchanged (ON to ON)	1.0	
			ON/OFF status changed (OFF to ON)	1.0	
	M, L, S	Not executed		1.0	
		Executed	ON/OFF status unchanged (ON to ON)	1.0	
			ON/OFF status changed (OFF to ON)	1.0	
	Special M, B	Not executed		3.0	
		Executed		32.1	
	F	Not executed		3.0	
		Executed		477.1	
	T, C	Not executed		3.0	
		Executed		43.1	
	D, W, A0, A1, V, Z	Not executed		3.0	
		Executed		27.5	
	R	Not executed		3.0	
		Executed		34.6	
NOP	———			1.0	
END	———			17000	
MC	Y	Not executed		43.1	
		Executed		39.4	
	M, L, S, F, B	Not executed		43.1	
		Executed		39.4	
MCR	———			26.4	
PLS	Y	Not executed		59.3	
		Executed	On	61.9	
			Off	60.3	
PLF	M, L, S B, F	Not executed		59.1	
		Executed	On	62.2	
			Off	60.6	
SFT	Y	Not executed		3.0	
		Executed		37.6	
SFTP	M, L, S B, F	Not executed		3.0	
		Executed		37.6	
MPS	———			1.0	
MRD	———				
MPP	———				

APP

11.2 Basic instructions

11.2.1 Relational instructions

Instruction			Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction Type / Device Used			All devices	All devices	
LD=	S1	S2	70	108	
AND=	S1	S2	61	96	
OR=	S1	S2	67	104	
LDD=	S1	S2	133	140	
ANDD=	S1	S2	124	131	
ORD=	S1	S2	133	140	
LD< >	S1	S2	69	106	
AND< >	S1	S2	60	101	
OR< >	S1	S2	66	99	
LDD< >	S1	S2	131	137	
ANDD< >	S1	S2	129	135	
ORD< >	S1	S2	129	135	
LD>	S1	S2	67	105	
AND>	S1	S2	60	101	
OR>	S1	S2	66	99	
LDD>	S1	S2	133	139	
ANDD>	S1	S2	131	137	
ORD>	S1	S2	131	137	

APP

Instruction			Processing Time (μsec) Type A All devices	Processing Time (μsec) Type B All devices	Remarks
LD<=	S1	S2	71	108	
AND<=	S1	S2	61	96	
OR<=	S1	S2	69	104	
LDD<=	S1	S2	137	143	
ANDD<=	S1	S2	128	133	
ORD<=	S1	S2	137	143	
LD<	S1	S2	69	136	
AND<	S1	S2	59	99	
OR<	S1	S2	66	100	
LDD<	S1	S2	133	139	
ANDD<	S1	S2	131	137	
ORD<	S1	S2	131	137	
LD>=	S1	S2	70	109	
AND>=	S1	S2	61	96	
OR>=	S1	S2	69	104	
LDD>=	S1	S2	137	142	
ANDD>=	S1	S2	127	133	
ORD>=	S1	S2	137	143	

11.2.2 BIN arithmetic operation instructions

Instruction				Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction Type / Device Used				All devices	All devices	
+	S	D		44	78	
+P	S	D		44	78	
D+	S	D		69	130	
D+P	S	D		69	130	
+	S1	S2	D	77	109	
+P	S1	S2	D	77	109	
D+	S1	S2	D	99	139	
D+P	S1	S2	D	99	139	
−	S	D		45	78	
−P	S	D		45	78	
D−	S	D		69	131	
D−P	S	D		69	131	
−	S1	S2	D	79	111	
−P	S1	S2	D	79	111	
D−	S1	S2	D	99	139	
D−P	S1	S2	D	99	139	
*	S1	S2	D	94	123	
*P	S1	S2	D	94	123	
D*	S1	S2	D	341	387	
D*P	S1	S2	D	341	387	

APP

Instruction (Instruction Type / Device Used)				Processing Time (μsec) Type A All devices	Processing Time (μsec) Type B All devices	Remarks
⁄	S1	S2	D	102	117	
⁄P	S1	S2	D	102	117	
D⁄	S1	S2	D	393	431	
D⁄P	S1	S2	D	393	431	
INC	D			29	65	
INCP	D			29	65	
DINC	D			42	81	
DINCP	D			42	81	
DEC	D			31	68	
DECP	D			31	68	
DDEC	D			42	84	
DDECP	D			42	84	

APP

11.2.3 BCD arithmetic operation instructions

Instruction				Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction / Device Used				All devices	All devices	
B+	S	D		123	138	
B+P	S	D		123	138	
DB+	S	D		175	181	
DB+P	S	D		175	181	
B+	S1	S2	D	129	143	
B+P	S1	S2	D	129	143	
DB+	S1	S2	D	187	193	
DB+P	S1	S2	D	187	193	
B−	S	D		125	140	
B−P	S	D		125	140	
DB−	S	D		175	181	
DB−P	S	D		175	181	
B−	S1	S2	D	133	149	
B−P	S1	S2	D	133	149	
DB−	S1	S2	D	185	193	
DB−P	S1	S2	D	185	193	
B*	S1	S2	D	299	313	
B*P	S1	S2	D	299	313	
DB*	S1	S2	D	941	946	
DB*P	S1	S2	D	941	946	

APP

Instruction				Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction Type / Device Used				All devices	All devices	
B/	S1	S2	D	235	249	
B/P	S1	S2	D	235	249	
DB/	S1	S2	D	896	901	
DB/P	S1	S2	D	896	901	

11.2.4 BCD to BIN conversion instructions

Instruction			Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction Type / Device Used			All devices	All devices	
BCD	S	D	82	114	
BCDP	S	D	82	114	
DBCD	S	D	219	225	
DBCDP	S	D	219	225	
BIN	S	D	79	110	
BINP	S	D	79	110	
DBIN	S	D	215	221	
DBINP	S	D	215	221	

APP

11.2.5 Data transmit instructions

Instruction				Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction Type / Device Used				All devices	All devices	
MOV	S	D		47	80	
MOVP	S	D		47	80	
DMOV	S	D		67	92	
DMOVP	S	D		67	92	
XCH	D1	D2		60	116	
XCHP	D1	D2		60	116	
DXCH	D1	D2		107	157	
DXCHP	D1	D2		107	157	
CML	S	D		43	85	
CMLP	S	D		43	85	
DCML	S	D		74	95	
DCMLP	S	D		74	95	
BMOV	S	D	n	399	416	
BMOVP	S	D	n	399	416	
FMOV	S	D	n	229	243	
FMOVP	S	D	n	229	243	

APP

11.2.6 Program branch instructions

Instruction	Processing Time (μsec)	Remarks
CJ P✳✳	39.2	Indexing qualifiers are not used.
	47.7	Indexing qualifiers are used.
SCJ P✳✳	71.2	Indexing qualifiers are not used.
	80.5	Indexing qualifiers are used.
JMP P✳✳	39.2	
*1 FEND	17000	
CALL P✳✳	69.7	Indexing qualifiers are not used.
	78.2	Indexing qualifiers are used.
CALLP P✳✳	69.7	Indexing qualifiers are not used.
	78.2	Indexing qualifiers are used.
RET	50.2	
FOR n	53.2	
NEXT	40.7	
STOP	———	
*1 CHG	16260	
SUB n	2473	Indexing qualifiers are not used.
	2486	Indexing qualifiers are used.
SUBP n	2473	Indexing qualifiers are not used.
	2486	Indexing qualifiers are used.

POINT

Processing time for T/C count (processing time at END) and refresh time are not included in processing time for *1 FEND and CHG instructions.

APP

11.3 Application instructions

11.3.1 Display instructions

Instruction		Processing Time (μ sec)	Remarks
LED	S	202.7	
LEDC	S	264.7	
LEDA	ASCII characters	201.7	
LEDB	ASCII characters	210.7	
LEDR		637.7	

11.3.2 Logic operation instructions

Instruction	Processing Time (μsec) Type A	Processing Time (μsec) Type B	Remarks
Instruction Type / Device Used	All devices	All devices	
WAND S D	59.5	112.5	
WANDP S D	59.5	112.5	
DAND S D	139.5	151.5	
DANDP S D	139.5	151.5	
WAND S1 S2 D	95.5	127.5	
WANDP S1 S2 D	95.5	127.5	
WOR S D	60.5	112.5	
WORP S D	60.5	112.5	
DOR S D	139.5	151.5	
DORP S D	139.5	151.5	
WOR S1 S2 D	96.5	143.5	
WORP S1 S2 D	96.5	143.5	
WXOR S D	59.5	112.5	
WXORP S D	59.5	112.5	
DXOR S D	139.5	151.5	
DXORP S D	139.5	151.5	
WXOR S1 S2 D	96.5	143.5	
WXORP S1 S2 D	96.5	143.5	
WXNR S D	63.5	113.5	
WXNRP S D	63.5	113.5	

APP

Instruction				Processing Time (μsec) Type A All devices	Processing Time (μsec) Type B All devices	Remarks
DXNR	S	D		141.5	151.5	
DXNRP	S	D		141.5	151.5	
WXNR	S1	S2	D	97.5	143.5	
WXNRP	S1	S2	D	97.5	143.5	
NEG	D			49.5	65.5	
NEGP	D			49.5	65.5	

11.3.3 Rotation instructions

The values for processing time are those for when n = 3.

Instruction	Processing Time (μ sec)	Remarks
ROR n	51.5	Indexing qualifiers are not used.
	56.5	Indexing qualifiers are used.
RORP n	51.5	Indexing qualifiers are not used.
	56.5	Indexing qualifiers are used.
RCR n	58.5	Indexing qualifiers are not used.
	63.5	Indexing qualifiers are used.
RCRP n	58.5	Indexing qualifiers are not used.
	63.5	Indexing qualifiers are used.
ROL n	53.5	Indexing qualifiers are not used.
	58.5	Indexing qualifiers are used.
ROLP n	53.5	Indexing qualifiers are not used.
	58.5	Indexing qualifiers are used.
RCL n	56.5	Indexing qualifiers are not used.
	62.5	Indexing qualifiers are used.
RCLP n	56.5	Indexing qualifiers are not used.
	62.5	Indexing qualifiers are used.
DROR n	69.5	Indexing qualifiers are not used.
	74.5	Indexing qualifiers are used.
DRORP n	69.5	Indexing qualifiers are not used.
	74.5	Indexing qualifiers are used.
DRCR n	71.5	Indexing qualifiers are not used.
	77.5	Indexing qualifiers are used.
DRCRP n	71.5	Indexing qualifiers are not used.
	77.5	Indexing qualifiers are used.
DROL n	69.5	Indexing qualifiers are not used.
	74.5	Indexing qualifiers are used.
DROLP n	69.5	Indexing qualifiers are not used.
	74.5	Indexing qualifiers are used.

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Instruction	Processing Time (μsec)	Remarks
DRCL n	67.5	Indexing qualifiers are not used.
	73.5	Indexing qualifiers are used.
DRCLP n	67.5	Indexing qualifiers are not used.
	73.5	Indexing qualifiers are used.

11.3.4 Shift instructions

Instruction	Type A	Type B	Remarks
	Processing Time (μsec)		
Instruction Type / Device Used	All devices	All devices	
SFR D n	73.5	99.5	When n = 5
SFRP D n	73.5	99.5	When n = 5
BSFR D n	123.5	141.5	When n = 5
	129.5	151.5	When n = 15
BSFRP D n	123.5	141.5	When n = 5
	129.5	151.5	When n = 15
DSFR D n	117.5	123.5	When n = 5
	179.5	187.5	When n = 15
DSFRP D n	117.5	123.5	When n = 5
	179.5	187.5	When n = 15
SFL D n	73.5	109.5	When n = 5
SFLP D n	73.5	109.5	
BSFL D n	133.5	145.5	When n = 5
	137.5	155.5	When n = 15
BSFLP D n	133.5	145.5	When n = 5
	137.5	155.5	When n = 15
DSFL D n	117.5	124.5	When n = 5
	181.5	189.5	When n = 15
DSFLP D n	117.5	124.5	When n = 5
	181.5	189.5	When n = 15

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11.3.5 Data processing instructions

Instruction	Processing Time (μ sec) Type A All devices	Processing Time (μ sec) Type B All devices	Remarks
SER S1 S2 n	199.5	231.5	When n = 5
	321.5	353.5	When n = 15
SERP S1 S2 n	199.5	231.5	When n = 5
	321.5	353.5	When n = 15
SUM S	114.5	128.5	
SUMP S	113.5	129.5	
DSUM S	199.5	203.5	
DSUMP S	199.5	203.5	
DECO S D n	163.5	193.5	When n = 2
	247.5	279.5	When n = 8
DECOP S D n	163.5	193.5	When n = 2
	247.5	279.5	When n = 8
SEG S D	D = B1 91.5	D = B100 977.5	
ENCO S D n	163.5	195.5	When n = 2
	301.5	331.5	When n = 8
ENCOP S D n	163.5	199.5	When n = 2
	301.5	331.5	When n = 8
BSET D n	89.5	106.5	When n = 5
	92.5	111.5	When n = 15
BSETP D n	89.5	106.5	When n = 5
	92.5	111.5	When n = 15

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Instruction	Processing Time (μsec) Type A All devices	Processing Time (μsec) Type B All devices	Remarks
BRST D n	96.5	110.5	When n = 5
	99.5	114.5	When n = 15
BRSTP D n	96.5	110.5	When n = 5
	99.5	114.5	When n = 15
UNI S D n	108.5	142.5	When n = 1
	130.5	164.5	When n = 4
UNIP S D n	108.5	142.5	When n = 1
	130.5	164.5	When n = 4
DIS S D n	137.5	169.5	When n = 1
	153.5	183.5	When n = 4
DISP S D n	137.5	169.5	When n = 1
	153.5	183.5	When n = 4

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11.3.6 FIFO instructions

Instruction			Processing Time (μsec) Type A All devices	Processing Time (μsec) Type B All devices	Remarks
FIFW	S	D	100.5	131.5	
FIFWP	S	D	100.5	131.5	
FIFR	D1	D2	117.5	147.5	
FIFRP	D1	D2	117.5	147.5	

11.3.7 ASCII conversion instruction

Instruction			Processing Time (μsec)	Remarks
ASC	ASCII characters	D	120	

11.3.8 Special function module instructions

Instruction	Processing Time (μ sec)	Remarks
FROM n1 n2 D n3	3347	When n3 = 1
	12605	When n3 = 1000
FROMP n1 n2 D n3	3347	When n3 = 1
	12605	When n3 = 1000
DFRO n1 n2 D n3	3051	When n3 = 1
	12595	When n3 = 500
DFROP n1 n2 D n3	3051	When n3 = 1
	12595	When n3 = 500
TO n1 n2 S n3	3247	When n3 = 1
	22590	When n3 = 1000
TOP n1 n2 S n3	3247	When n3 = 1
	22590	When n3 = 1000
DTO n1 n2 S n3	3523	When n3 = 1
	19340	When n3 = 500
DTOP n1 n2 S n3	3523	When n3 = 1
	19340	When n3 = 500

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11.3.9 Other instructions

Instruction	Processing Time (μsec)	Remarks
WDT	63.7	
WDTP	63.7	
CHK D1 D2	771	When the number of conditional contacts is 1 point.
	3380	When the number of conditional contacts is 50 points.
	6887	When the number of conditional contacts is 100 points.
	10137	When the number of conditional contacts is 150 points.
SLT	8448	When device memory only
	24598	When device memory + R (8K points)
SLTR	29.3	
STRA	30.2	
STRAR	27.7	
STC	28.1	
CLC	30.5	
DUTY n1 n2 D	60.4	
PR S D	3183	
PRC S D	3172	

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IMPORTANT

The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(1) Ground human body and work bench.

(2) Do not touch the conductive areas of the printed circuit board and its electrical parts with any non-grounded tools etc.

Under no circumstances will Mitsubishi Electric be liable or responsible for any consequential damage that may arise as a result of the installation or use of this equipment.

All examples and diagrams shown in this manual are intended only as an aid to understanding the text, not to guarantee operation. Mitsubishi Electric will accept no responsibility for actual use of the product based on these illustrative examples.

Owing to the very great variety in possible applications of this equipment, you must satisfy yourself as to its suitability for your specific application.

Multiplex system type A3VTS

User's Manual

MODEL	A3VTS-USERS-E
MODEL CODE	13J656
IB(NA)66190-A(8905)MEE	

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100-0005 TELEX : J24532 CABLE MELCO TOKYO
NAGOYA WORKS : 1-14 , YADA-MINAMI 5 , HIGASHI-KU, NAGOYA , JAPAN