MITSUBISHI
PROGRAMMABLE CONTROLLER
MELSEC-K

Instruction Manual
Type MELSEC-KOJ1U

83-U/IB(NA) 64479-A

MITSUBISHI ELECTRIC

– CONTENTS –

MEMO

1. FEATURES

1. FEATURES

- **High Performance in a Compact Unit**
  In addition to the standard instruction functions, the Model KOJ1U Series of controllers give you addition, subtration, comparsion and a variety of other practical functions.

- **Full Range of Peripherals**
  For easier planning and maintenance, a full range of peripherals is available.

- **High-speed Processing Capability**
  The executing time is equivalent to K2 CPU.

- **High Speed Excution and Subroutine Call**
  High speed response and subroutine calls are possible by calling high speed processing programs during main program excution.

- **Built-in Timers**
  The built-in timers offer a choice of settings in units of 0.1 second or 0.01 second for high-precision operations.

- **All the Units in the MELSEC K2 Series Can Be Used**
  High-speed counter unit, A/D and D/A converter units etc.
  * For details about the MELSEC K2 series, refer to our separate catalogs.

- **Removable Terminal Block**
  The terminal block can be removed from the main unit with cables connected.

2. CONFIGURATION

2. CONFIGURATION

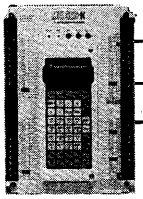
2.1 Overall Configuration

KOJ1U – Economical Model for Small-sized Production	Serviceable Peripherals Available for Further Imporvement of Functions

●Basic unit

Consists of CPU, program memory, power supply, and input/output units.

When extenion unit is used, KOJ1-EX1 is fitted inside.

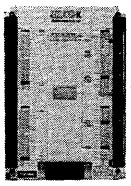


KOJ1U
Inputs : 32
Outputs : 24

●Extension units

Type E56

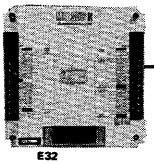
Consists of 32 inputs, 24 outputs, and extension adaptor.
Available in 4 types, DR, AR, AS and AT.



E56
Inputs : 32
Outputs : 24

Type E32

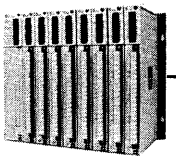
Consists of 16 inputs and 16 outputs.
Available in 4 types, DR, AR, AS and AT.



E32
Inputs : 16
Outputs : 16

●Extension base

This is a base used to mount input/output unit for K2.
A maximum of 128 inputs/outputs can be packaged.



K65B/K68B
Inputs/Outputs : Max. 128

Programer (K7PUE)

●Programming input/output unit

Data cassette interface (K7MTFE)

Data cassette recorder (K7MTE)

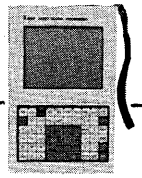
● Industrial-purpose cassette loader and interface

Graphic programming panel interface (K6GPFE)

Graphic programming panel (K8GPPE)

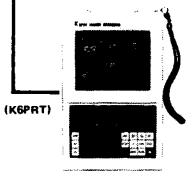
● Graphic programming panel with CRT display and interface

Handy graphic programmer interface (K6HGPFE)



Handy graphic programmer (K6HGPE)

●Handy graphic programming panel with liquid crystal display



(K6PRT)

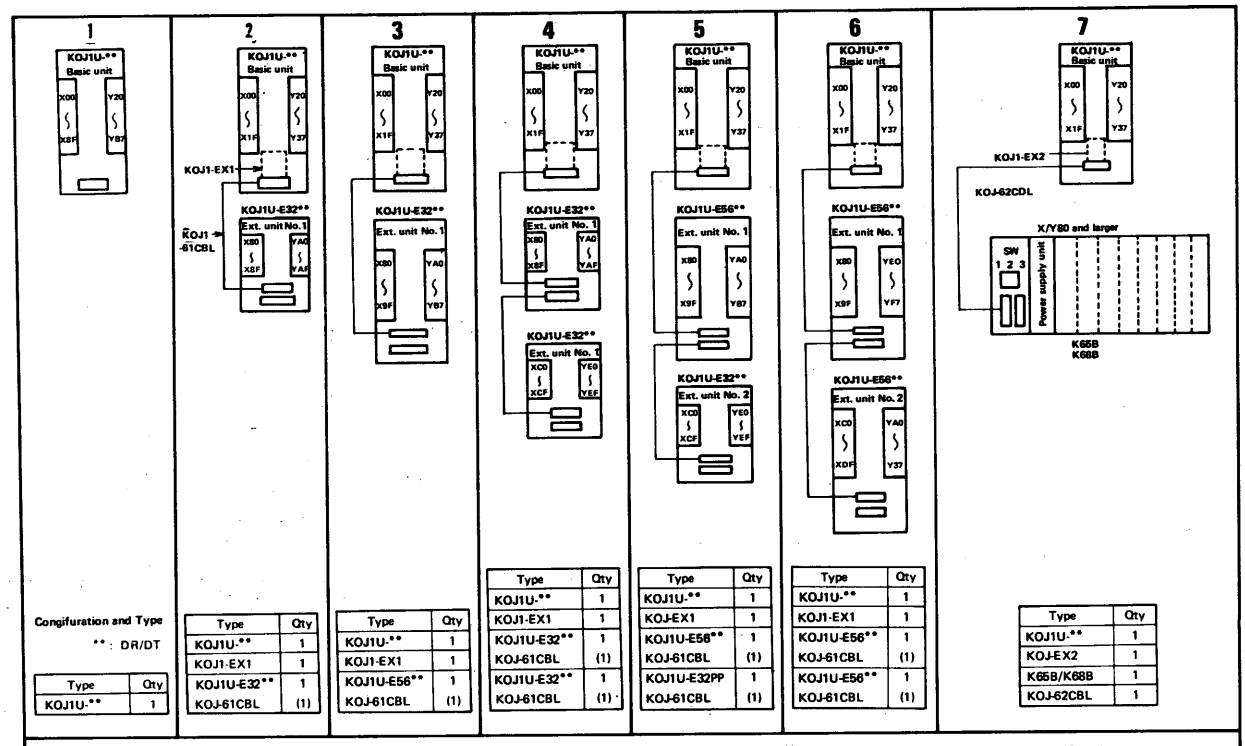
●P-ROM writer (2716, 2732, 2732A, 2764, 27128)

●Audio cassette interface

●Printer interface

2.2 System configuration

Seven types of system configurations are available as shown below.



Congifuration and Type

**: DR/DT

Type	Qty
KOJ1U-**	1

Type	Qty
KOJ1U-**	1
KOJ1-EX1	1
KOJ1U-E32**	1
KOJ-61CBL	(1)

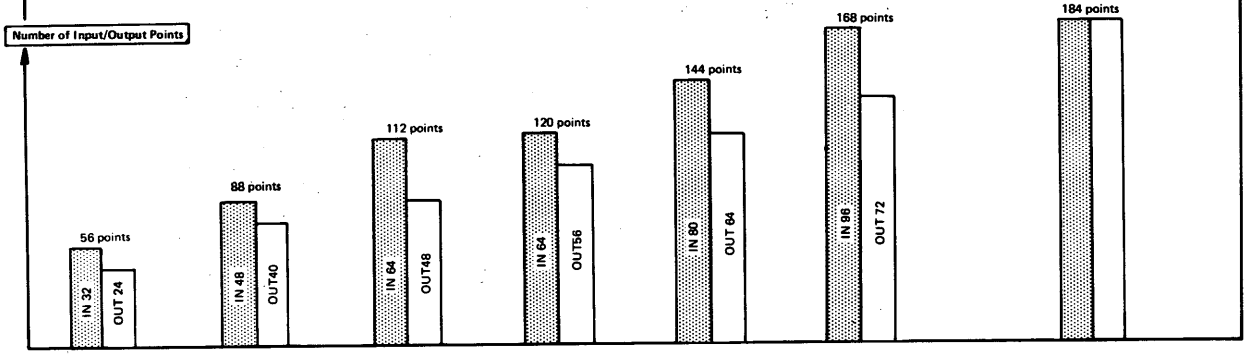
Type	Qty
KOJ1U-**	1
KOJ1-EX1	1
KOJ1U-E56**	1
KOJ-61CBL	(1)

Type	Qty
KOJ1U-**	1
KOJ1-EX1	1
KOJ1U-E32**	1
KOJ-61CBL	(1)
KOJ1U-E32**	1
KOJ-61CBL	(1)

Type	Qty
KOJ1U-**	1
KOJ-EX1	1
KOJ1U-E56**	1
KOJ-61CBL	(1)
KOJ1U-E32PP	1
KOJ-61CBL	(1)

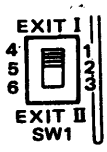
Type	Qty
KOJ1U-**	1
KOJ1-EX1	1
KOJ1U-E56**	1
KOJ-61CBL	(1)
KOJ1U-E56**	1
KOJ-61CBL	(1)

Type	Qty
KOJ1U-**	1
KOJ-EX2	1
K65B/K68B	1
KOJ-62CBL	1



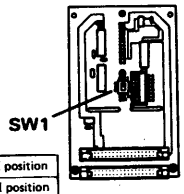
- Switching Procedure between Extension Units No. 1 and No. 2

(1) Type E32 extension unit
When Type E32 extension unit is used, it is necessary to set the internal switch SW1 first.



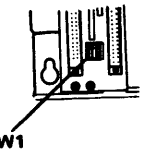
In case of ext. 1	To EXT1 position
In case of ext. 2	To EXT2 position
Systems 2, 4 and 5	

(2) Type E56 extension unit
When Type E56 extension unit is used, it is necessary to set the internal switch SW1 first.

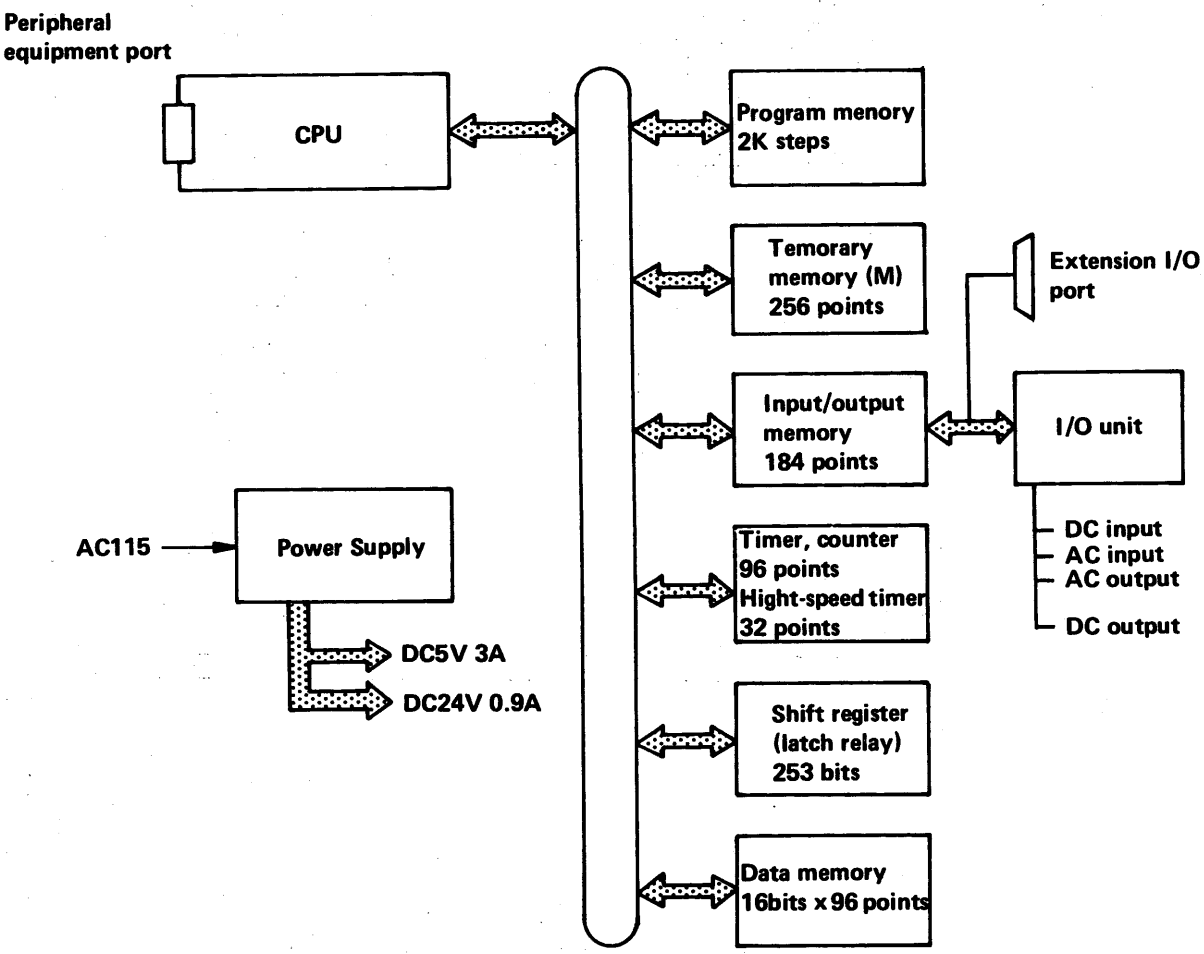


In case of ext. 1	To EXI position
In sase of ext. 2	To EXII position
Systems 3, 5 and 6	

(3) K65B/K68B
When K65B/K68B is used as extension, turn on only one of the internal switches SW1 to SW3. Input/Output No. is initiated from X/Y80.

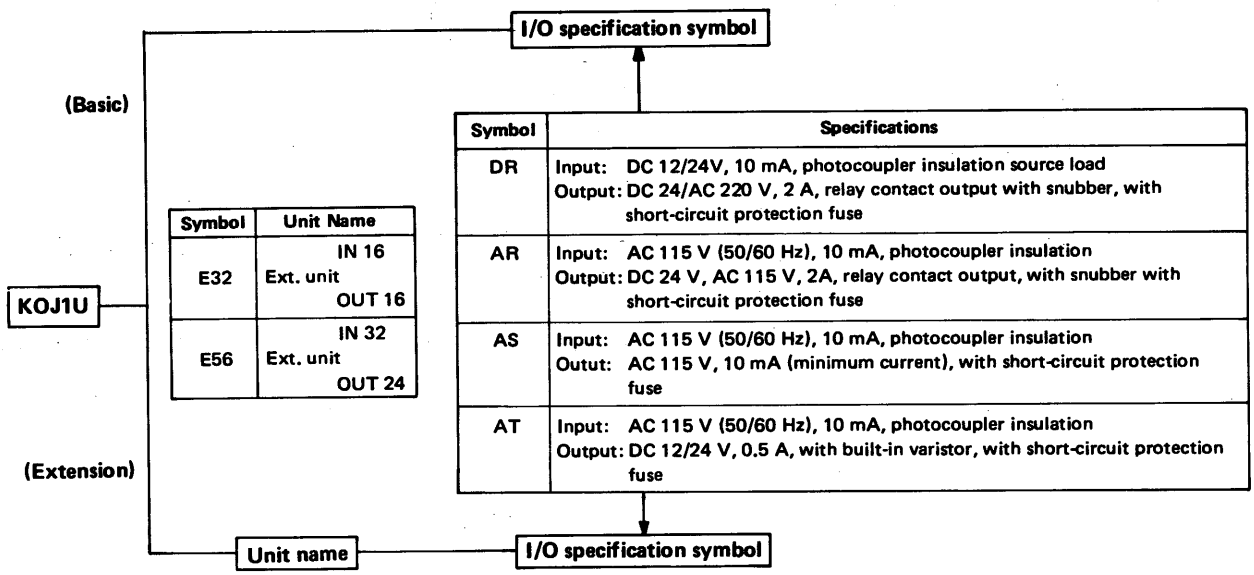


2.3 Overall Block Diagram



2.4 Main Unit Configuration

2.4.1 Equipment configuration



Symbol	Unit Name
E32	IN 16 Ext. unit OUT 16
E56	IN 32 Ext. unit OUT 24

Symbol	Specifications
DR	Input: DC 12/24V, 10 mA, photocoupler insulation source load Output: DC 24/AC 220 V, 2 A, relay contact output with snubber, with short-circuit protection fuse
AR	Input: AC 115 V (50/60 Hz), 10 mA, photocoupler insulation Output: DC 24 V, AC 115 V, 2A, relay contact output, with snubber with short-circuit protection fuse
AS	Input: AC 115 V (50/60 Hz), 10 mA, photocoupler insulation Outut: AC 115 V, 10 mA (minimum current), with short-circuit protection fuse
AT	Input: AC 115 V (50/60 Hz), 10 mA, photocoupler insulation Output: DC 12/24 V, 0.5 A, with built-in varistor, with short-circuit protection fuse

Example of type designation

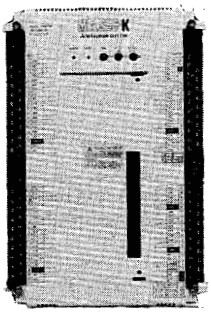
- **Basic unit** KOJ1U-DR
- **Ext. unit** KOJ1U-E56DR

List of Individual Equipment

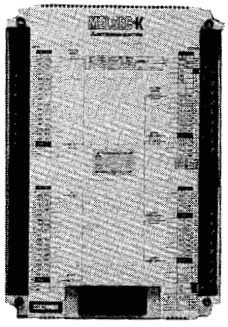
Name	Type	Specifications		Weight (kg)
Extension adaptor	KOJ1-EX1	Adaptor for connecting extension unit (E32, E56) (Fitted to basic unit)		0.1
	KOJ1-EX2	Adaptor for connecting extension base (K65B/K68B) (Fitted to basic unit)		0.1
Power supply unit	KOJ1U-PW	DC 24 V input, DC 24 V 0.9 A output (for E56 extension)		0.5
Extension	KOJ-61CBL KOJ-61CBL2	*1 Cable for connecting across KOJ1U	Length 500 (mm) Length 1000 (mm)	0.075 0.175
	KOJ-62CBL KOJ-62CBL2	Cable for connecting with K65B/K68B extension base	Length 500 (mm) Length 1000 (mm)	0.075 0.175
Extension base	K65B/K68B	Extension base for K2, maximum of 8 I/O units can be fitted.		3.3 (K68B)
Fuse	GGC3 GGL10 GTH-5	Short-circuit protection fuse for power supply and transistor output 3 A Short-circuit protection fuse for relay output 10 A Short-circuit protection fuse for triac output 5 A		
Memory	KORAM 2KORM	1K step ..... built-in 2K step ..... 1 pce. fitted 6116* Equivalent to 2732. For 0 - 2K step.		

*1 Extension unit is equipped with KOJ-61CBL. *2K x 8

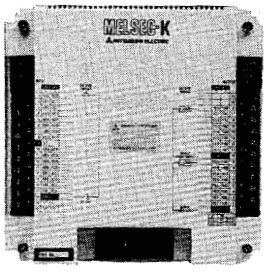
2.4.2 External view of equipment



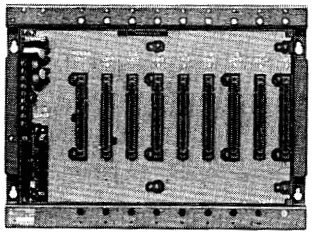
KOJ1U basic unit



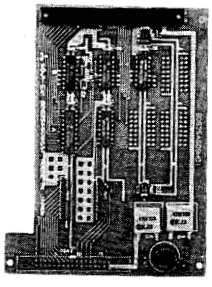
Type 56 extension unit



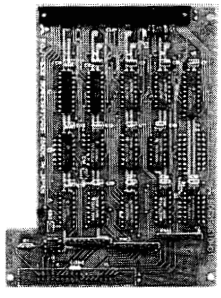
Type 32 extension unit



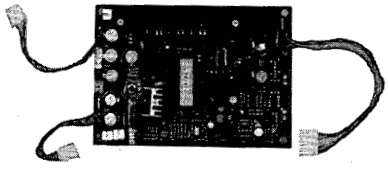
K68B



KOJ1–EX1



KOJ1–EX2



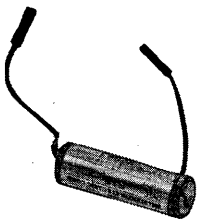
KOJ1U-PW

KORAM

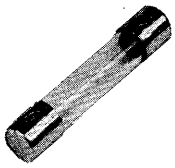
2KROM

KOJ–61CBL

KOJ–62CBL



K6BAT



GGC3
GGL10
GTH-5

2.5 Peripherals

Unit	Description	Type No.	Remarks	Weight (kg)
GPP	Graphic programming panel	K8GPPE	Programming unit with CRT. Used together with K6GPFE and K63CBL.	11.8
	GPP interface unit	K6GPFE	Interface used for connection between main unit CPU and K8GPPE.	0.45
	GPF cable	K63CBL	Cable used for connection between K8GPPE and K6GPFE.	0.7
PU	Programmint unit	K7PUE	Program I/O unit for main unit CPU.	0.5
MT for industrial	Data cassette interface	K7MTFE	Interface used for connection between main unit CPU, K8GPPE and K7MTE.	0.45
	Data cassette	K7MTE	Data cassette for industrial use.	4.5
	Data cassette cable	K63CBL	Cable used for connection between K7MTE and K7MTFE. Same as GPF cable.	0.7
HGP	HGP interface	K6HGPFE	Interface used for connection between main unit CPU and K6HGPE.	0.33
	Handy graphic programmer	K6HGPE	Programming unit with liquid crystal display	1.1
	Interface cable	K70CBL	Cable used for connection between K6HGPFE and K6HGPE.	0.27
PRT	Handy recorder	K6PRT	Cassette loader with liquid crystal display, P-ROM writer, printer interface unit.	0.95
	PRT interface	K6HGPFE	Interface used for connection between main unit and K6PRT.	0.33
	Interface cable	K70CBL	Cable used for connection between K6HGPFE and K6PRT.	0.27

2.6 Selection of Peripherals

Peripheral Equipment Configuration		Applications																																
		Program preparation			Program writing				Program change		Program reading			Program-to-program check	Program storage			Operating condition monitor					Print-out of drawing, etc.				Forced on-off of of output, etc.	Confirmation of ROM erasure
		Circuit	List	Edit, appropriation	Main unit RAM	ROM	Cassette tape	Machine language	Addition	Deletion	Circuit diagram	List	Machine language		ROM	Cassette tape	Data tape	I/O monitor	TCMDF monitor	Abnormal code	Abnormal number	Abnormal condition print-out	Internal circuit	External circuit	List	Hard copy of drawing		
Main unit K7PUE			○						○	○		○						○	○	○							○	
Main unit K7MTFE K7MTE																	○											
Main unit K6GPFE K8GPPE PE1	Not fitted	○	○	○	○			○	○	○	○	○	○	○				○	○	○	○						○	
	K6HGPFE +K6PRT	○	○		○	○	○		○	○	○	○		○	○	○		○	○	○			○	○				
	K7MTFE	○	○	○	○			○	○	○	○	○	○	○			○	○	○	○	○						○	
K6HGPFE Main unit K6HGPE		○	○		○				○	○	○	○						○	○	○								
K6HGPFE Main unit K6PRT					○	○	○							○	○	○							○		○			

MEMO

3. SPECIFICATIONS

3.1 General Specifications

Item		Specifications
Power Sypply	Applied voltage	AC 115V ± 15% 50, 60 Hz
	Power Consumption	85 VA, 62W
Operating ambient temp.		0 ~ 55°C
Storage ambient temp.		–10 ~ 75°C
Operating ambient humidity		10 ~ 90% RH, free of dew condensation
Storing ambient humdity		10 ~ 90% RH, free of dew condensation
Vibration resistance		Shall conform to class 3, IIB, JIS C0911 (16.7 Hz, 3-mm double amplitude, 2 hrs.)
Shock resistance		Shall confrom to JIS C 0912 (10 g x 3 times in X, Y, Z, directions)
Noise resistance		1000 Vpp noise voltage, 1 μs noise width, 25 ~ 60 Hz noise frequency by noise simulator
Dielectric withstand voltage	AC 1500V for 1minute	Across batch of AC terminals and case
		Across batch of external AC terminals and batch of external DC terminals
	AC 500V for 1minute	Across batch of external DC terminals and case
Insulation resistance	5MΩ larger by 500V insulation registance meter	Across batch of external AC terminals and case
		Across batch of external AC terminals and batch of external terminals
		Across external DC terminals and case
Grounding		100 Ω or smaller grounding resistance. When grounding is impossible, connect LG and FG terminals with panel.
Operating ambience		Particularly dust and corrosive gas should be little.
Cooling method		Self-cooling
Applicable cable rating		22 AWG ~ 14 AWG (0.3 mm^2 ~ 2 mm^2)
Reference terminal board tightening torque		11.2 ± 15% kg·f·cm (M3.5 screw used)

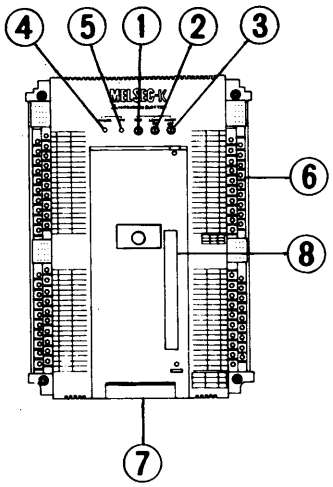
3.2 Performance Specifications

Item		Specifications
Control method		Stored program, repeated operation
I/O control method		Input and output are made each time during repeated operation.
Programming language		Dedicated language to sequence control (relay symbol type, used together with logic symbolic language)
Instruction	No. of instructions	26 types of basic instructions (sequence instruction + data instruction) + 15 types of application instruction
	Word length	16 bits/1 step
Sequence instruction excution time		5.6μS/1 step in average
Program capacity and memory		1024 steps, RAM (Standard equipped) 2048 steps, RAM (KORAM fitted to socket) 2048 steps, ROM (2KROM fitted to socket)
No. of I/O points		Basic unit: 32 inputs, 24 outputs
		E32 extension unit: 16 inputs, 16 outputs
		E56 extension unit: 32 inputs, 24 outputs
		K65B extension base: Up to 5 I/O cards for K2 can be fitted.
		K68B extension base: Up to 8 I/O cards for K2 can be fitted.
No. of temporary storage points		254 points (M0 ~ M253). Turned on when M254 battery is abnormal. Turned on when M255 self-diagonsis result output is run.
Timer, counter (bulit-in)	No. of usable points	128 points (T.C0 ~ 127 incl. timers and counters)
	Timer specifications	T0 ~ T95: 0.1 ~ 99.9 sec. setup time, 0.1 sec. setup increments, on delay. T96 ~ T127: 0.01 ~ 99.99 sec. setup time, 0.01 sec. setup increments, on delay.
	Counter specifications	1 ~ 9999 setting ragnes, max. 10 c/s counting speed (at 1K steps.)
Shift register	No. of usable points	253 bits (M1 ~ 253) excluding those used for temporary storage.
	Specifications	With temporary storang in units of 1 bit combined, up to 253 bits are possible (data shift is also possible).
Data	Data register specifications	96 points (D0 ~ D95), 16 bits for 1 data, max. 4 digits can be handled in units of 4 bits.
	Data input/output	4 I/O points make up 1 digit. Usable jointly with process input/output. Decimal 1 ~ 4 digits from 0 to 9999.
Backup for power failure		Backup for power failure is possible by LATCH ON switch on basic unit. M128 ~ 253, T.C64 ~ 111, D64 ~ 95
Allowable instant stop time		20 ms. Initial start in case if 20 ms or longer period.
Self-diagnostic functions		Arithmetic operation jam monitor, abnormal machine code detection, abnormal power supply detection, RUN signal is output from exterior by program.
Battery functions		Backup for program memory (RAM) and latch function. Lithium battery. Total 300-day backup period. 5-year battery service life.

3.3 Individual Specifications

3.3.1 Basic unit (KOJ1U-**-***)

Item	Specifications
Input voltage	AC 115V ± 15%
Input frequency	50, 60 Hz
Max. apparant input power	85 VA
Max. effective input power	
Rush current	20 A or lower
Output voltage	DC 24 V
Max. output current	0.9 A
Excess current protection	150% ~ 220% of rated value



① **RUN switch**
This switch is used to start and stop the sequencer. Move the switch to "RUN" position and the sequencer is started. Move it to "STOP" position, and program excecution is suspended and the sequencer comes to a stop. When the sequencer is at a stop, all outputs are off.

② **LATCH switch**
This switch is used to select the setting of backup for power failure. "ON" position is for backup for power failure. "OFF" position is for no backup.

③ **RESET switch**
This switch is used to reset abnormal arithmetic operation and to initialize arithmetic operation. Also use this switch to clear all contents of arithmetic operation and restart arithmetic operation. At this time, M, T, C, D, which are not backed up for power failure, and output Y are all cleared.

④ **POWER indicator**
This is a power indicator light for DC 5 V output.

⑤ **RUN indicator light**
This light turns on when normal operation is made. The light turns off when the sequencer comes to a stop or power is cut off. It flickers and turns on when watchdog error or illegal code is detected.

⑥ **CONNECTOR**
This is a connector which connects peripheral unit.

⑦ **CONNECTOR**
This is a connector for extension cable attached to extension adaptor. When adaptor is not provided, blind cap is furnished instead of this connector. The basic unit is standard equipped with blind cap.

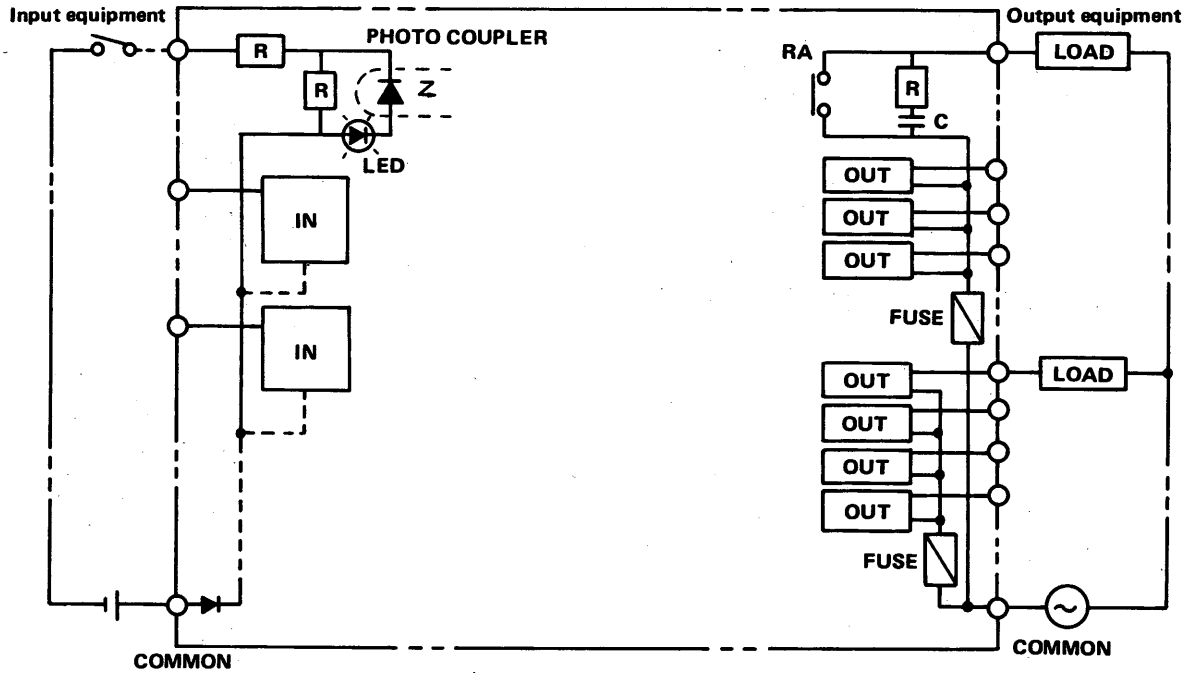
⑧ **TERMINAL BLOCK**
This is a terminal block which connects power supply and I/O signal cable. Equipped with finger protector.

KOJI-DR

3.3.2 Type DR I/O specificatin (DC 24 V input, relay contact output)

Input Specifications		
Insulation method	Photocoupler insulation	
Operation display	All points displayed by LEDs	
Input voltage	DC 12/24 V	
Input current	4/10 mA	
Operation voltage	OFF → ON	10 V min.
	ON → OFF	8 V max.
Response time (at DC 24 V)	OFF → ON	3 ~ 6 mSec
	ON → OFF	
Input system	Sink input (input current efflux system)	
Common connection	16 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	

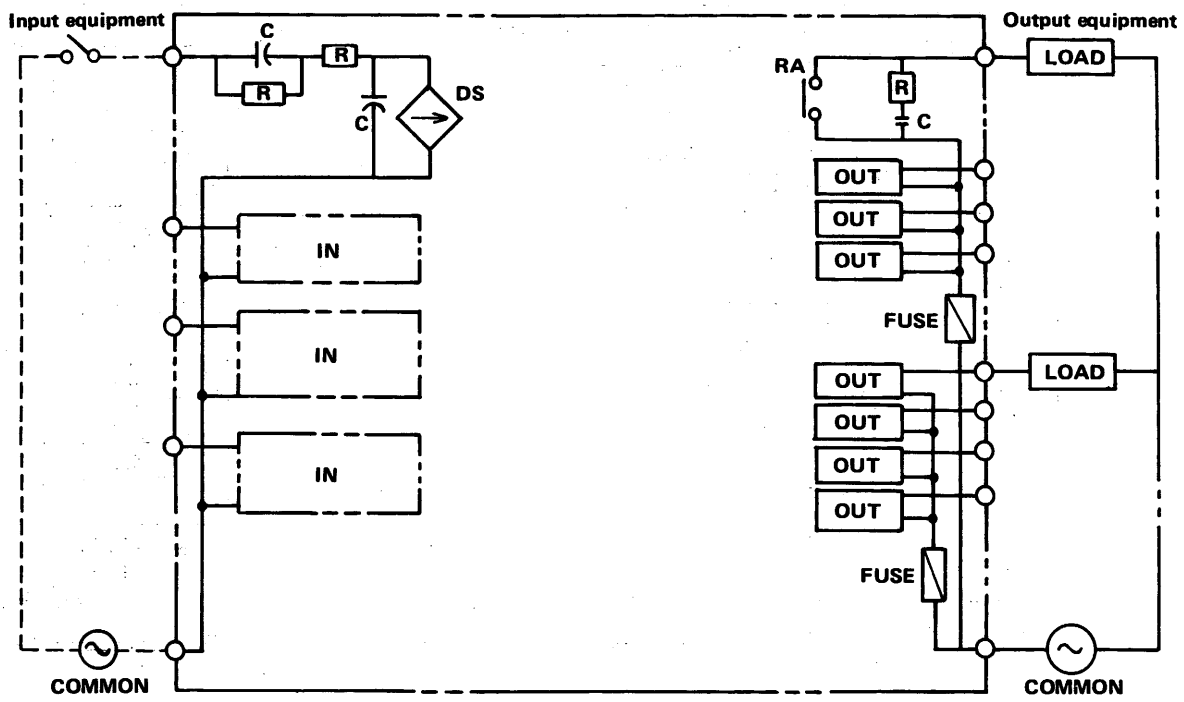
Output Specifications		
Insulation method	Relay insulation	
Operation display	All points displayed by LEDs	
Max. load Voltage	DC 125 V/AC 132 V	
Load current	2 A/1 point	
	8 A/8 points totally	
Min. load	100 mW (mA, 1V min.) 5 mA (AC 100V at AC 200V)	
Response time	OFF → ON	5 mS max.
	ON → OFF	15 mS max.
Life (Mechanical)	20,000,000 times min.	
Leak current	2 mA (AC 220 V, 60 Hz)	
Common connection	8 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	
Current consumption	525 mA (DC 24 V, 25°C when 24 points turn on simultaneously)	
Short-circuit Protection fuse	1 fuse/4 points GGL7 7A AC 250 V	



3.3.3 Type AR I/O specificatin (AC 115 V input, relay contact output)

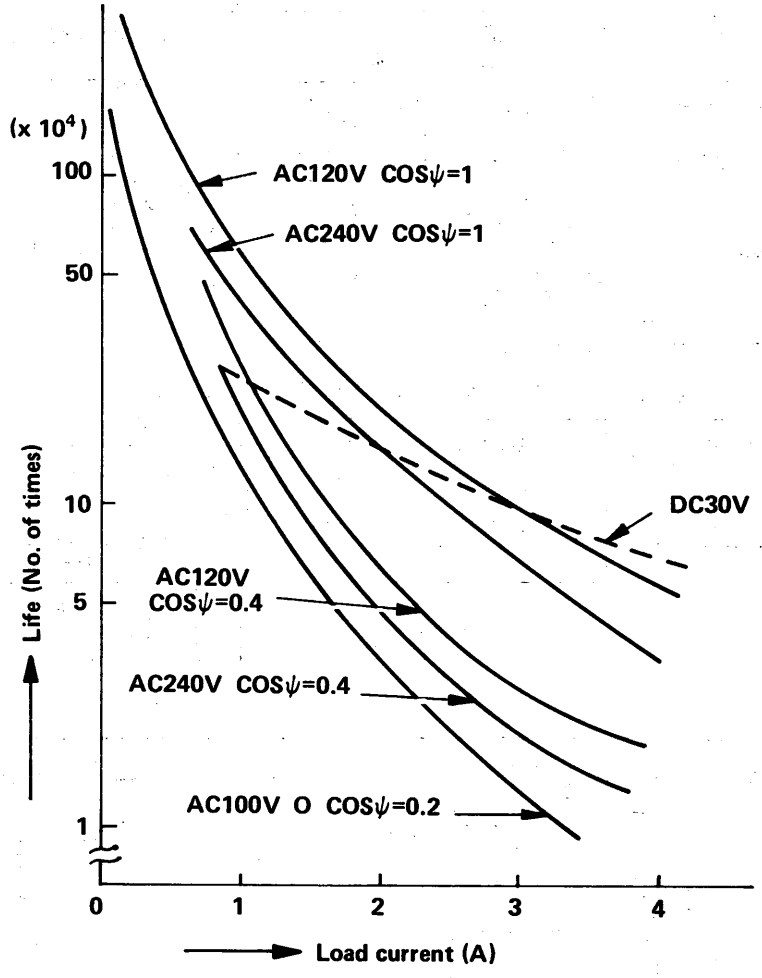
Input Specifications		
Insulation method	Photocoupler insulation	
Operation display	All points displayed by LEDs	
Input voltage	AC 115V ± 15% (AC 85V ~ AC 132V)	
Input current	10 mA ± 1.5 (AC 115V, 50 Hz)	
Operation voltage	ON Voltage 90 V min.	
	OFF Voltage 50 V max.	
Response time (at DC 24 V)	OFF → ON 4 ~ 12 mSec	
	ON → OFF 3 ~ 15 mSec	
Input inrush current	71 mA (90V), 105 mA (132V)	
Input inpedance	12 KΩ (50 Hz), 10 KΩ (60 Hz)	
Common connection	16 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	

Output Specifications		
Insulation method	Relay insulation	
Operation display	All points displayed by LEDs	
Max. load Voltage	DC 125 V/AC 132 V	
Load current	2 A/1 point 8 A/ 8 point totally	
Min. load	100 mW (mA, 1V min.) 5 mA (AC 100V at AC 200V)	
Response time	OFF → ON	8 mS max.
	ON → OFF	15 mS max.
Life (Mechanical)	20,000,000 times min.	
Leak current	2 mA (AC 220 V, 60 Hz)	
Common connection	8 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	
Current consumption	525 mA (DC 24 V, 25°C when 24 points turn on simultaneously)	
Short-circuit Protection fuse	1 fuse/4 points, GGL7, 7A, AC 250V	



- Contact Life of Contact Output

Relation between the load current and the contact life (expressed by number of times) of contact output used for Type AR and DR is as shown in the chart below.



Contact life curve

Note: When DC 100V load is opened and closed at the contact, set load current at 0.1 A or lower. When frequency is too high even at 0.1 A load, be sure to connect C-R surge killer or flywheel diode in parallel with the load.

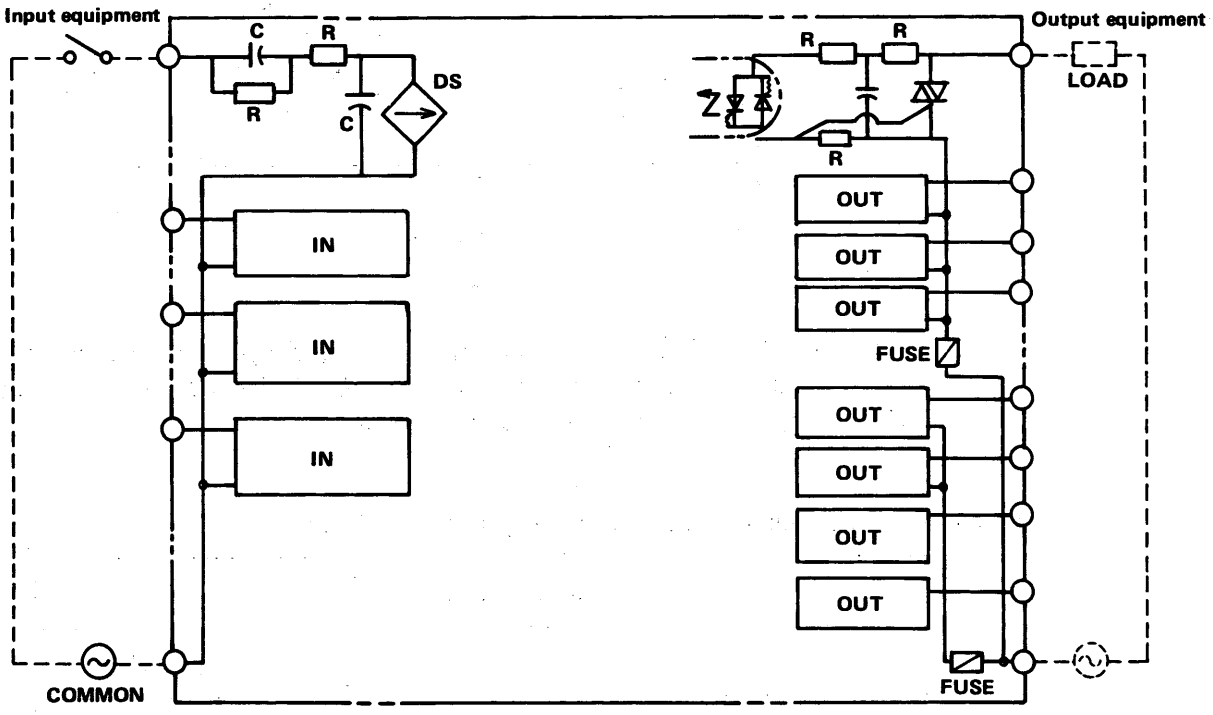
Example of drivable magnetic contactor (Mitsubishi Electric make)

Type of magnetic contactor		
Direct drive possible		Direct drive impossible
S-A10RM ~ S-A12RM	1,000,000 times	S-A600
S-K20 ~ S-K400	1,000,000 times	

3.3.4 Type AS I/O specificatin (AC 115 V input, triac output)

Input Specifications		
Insulation method	Photocoupler insulation	
Operation display	All points displayed by LEDs	
Input voltage	AC 115V ± 15% (95 ~ 132%)	
Input current	10 mA ± 1.5 (AC 115V, 50 Hz)	
Operation voltage	ON Voltage	85 V min.
	OFF Voltage	40 V max.
Response time (at DC 24 V)	OFF → ON	5 ~ 15 mSec
	ON → OFF	
Input inrush current	71 mA (90V), 105 mA (132V)	
Input inpedance	12 KΩ (50 Hz), 10 KΩ (60 Hz)	
Common connection	16 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	

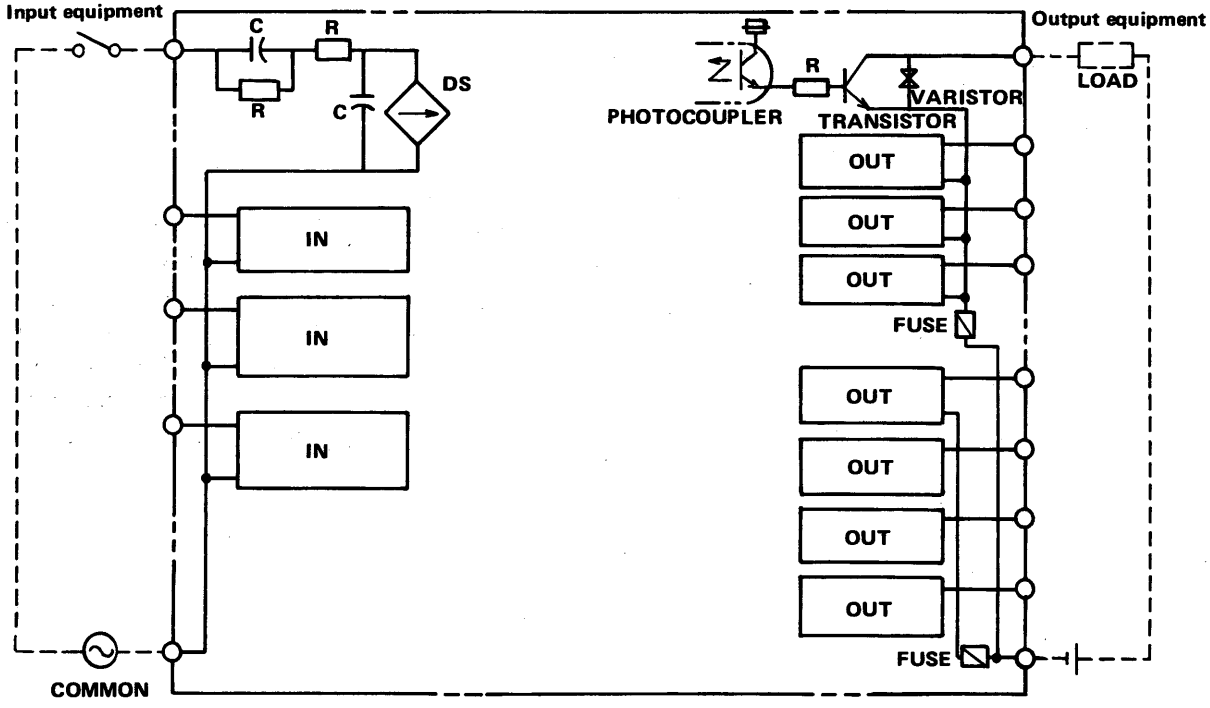
Output Specifications		
Insulation method	Photocoupler insulation	
Operation display	All points displayed by LEDs	
Max. load Voltage	AC 132 V	
Load current	1 A/1 point	
	5 A/8 point totally	
Max. rush load power supply	30 A, 1 sycle	
Output voltage drop	1.5 V max. (at 1A)	
Response time	OFF → ON	1 mS max.
	ON → OFF	(AC 1/2 cycle + 1 mS max.)
Leak current	1 mA (AC 120 V, 60 Hz)	
Common connection	8 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	
Short-circuit Protection fuse	GTH-5 (5 A)	



3.3.5 Type AT I/O specificatin (AC 115 V input, transistor output)

Input Specifications		
Insulation method	Photocoupler insulation	
Operation display	All points displayed by LEDs	
Input voltage	AC 115V ± 15% (AC 85V ~ AC 132V)	
Input current	10 mA ± 1.5 (AC 115V, 50 Hz)	
Operation voltage	ON Voltage	90 V min.
	OFF Voltage	50 V max.
Response time (at DC 24 V)	OFF → ON	4 ~ 12 mSec
	ON → OFF	3 ~ 15 mSec
Input inrush current	71 mA (90V), 105 mA (132V)	
Input inpedance	12 KΩ (50 Hz), 10 KΩ (60 Hz)	
Common connection	16 points connected with 1 common	
Terminal block specifications	2-piece type, with finger protector	

Output Specifications		
Insulation method	Photocupler insulation	
Operation display	All points displayed by LEDs	
Rated Voltage	DC 12/24 V	
Max. output voltage	DC 50V (DC 24V + 20%, single phase full-wave rectification usable)	
Rush current	10 A, 10 mS	
Max. output current	0.5 A/1 point, 4 A/8 points, all points ON	
Output voltage drop	0.8 V (TYP), 1.2 V (MAX)	
Response time	OFF → ON	0.1 mS max.
	ON → OFF	1 mS max.
Leak current	1 mA max.	
Built-in 24 V current consumption	50 mA (32 TYP), 75 mA (56 TYP)	
Common connection	8 points connected /1 common	
Protection	Excess voltage protection: varistor Short-circuit protection: fuse	
Terminal block specifications	2-piece type, with finger protector	



3.3.6 Power capacity calculation

DC 24 V of power supply (KOJ1U-PW) is supplied to the basic unit, the DC input circuits of E32 and E56 extension units, the relay power supply of contact output, etc. When the capacity of DC 24 V power supply within the basic unit is insufficient, it is possible to incorporate KOJ1U-PW into the E56 extension unit.
Calculate capacity as described below.

(1) Rated current of DC 24 V power supply (KOJ1U-PW)

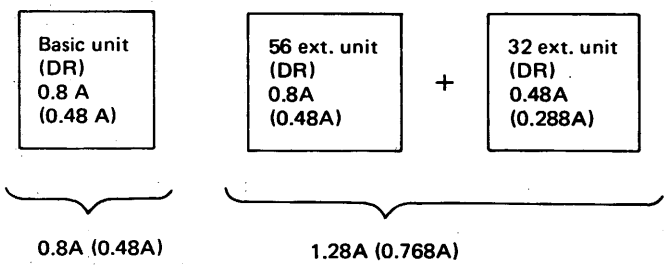
Ambinent temp.	Current capacity
~ 45°C	1.1 A
55°C	0.9 A

(1) Current consumption of DC 24 V of each unit

I/O symbol	24V current consumption per point		Current consumption of basic unit	Current consumption of E32 ext. unit	Current consumption of E56 ex
DR	~ 45°C	Input circuit 10mA Output circuit 21.6mA	10mA x 32 + 21.6mA x 24 = 0.84A	10mA x 16 + 21.6mA x 16 = 0.51A	10mA x 32 + 21.6mA x 24 = 0.84A
	55°C	Input circuit 10mA Output circuit 20mA	10mA x 32 + 20 x 24 = 0.8A	10mA x 16 + 20 x 16 = 0.48A	10mA x 32 + 20 x 24 = 0.8A

* Current consumption in above table is based on values obtained when all points are turned on at the same time.

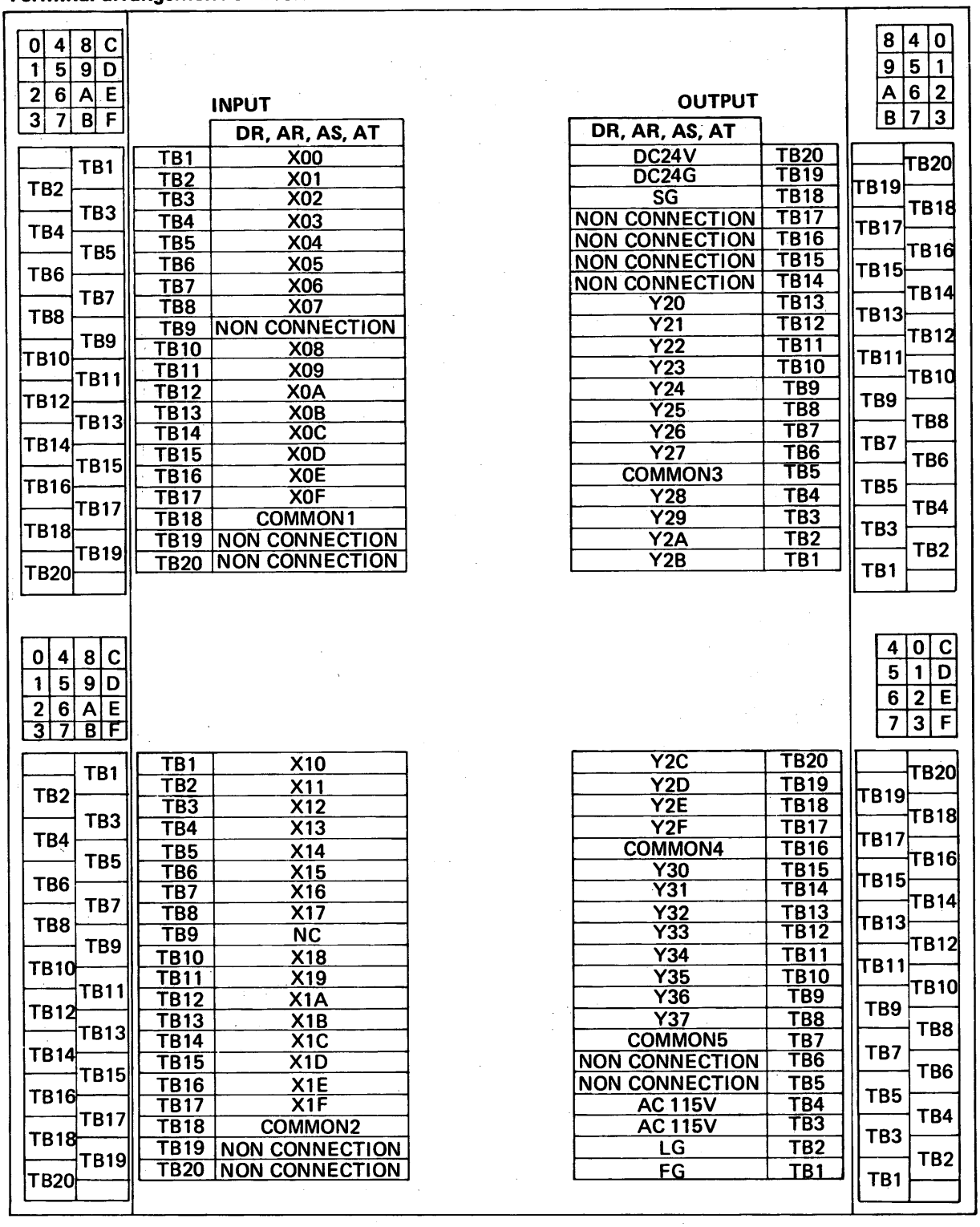
(2) Example of capacity calculation (55°C)
Unit configuration



When capacity is calculated on the assumption that each unit has simultaneous 60% "ON" ratio, values in parentheses are obtained. In this case, power supply unit is added to the E56 extension unit in order to supply power also to the E32 extension unit.

3.4 Terminal Arrangement

3.4.1 Terminal arrangement of basic unit



0	4	8	C
1	5	9	D
2	6	A	E
3	7	B	F

TB2	TB1
TB4	TB3
TB6	TB5
TB8	TB7
TB10	TB9
TB12	TB11
TB14	TB13
TB16	TB15
TB18	TB17
TB20	TB19

INPUT

	DR, AR, AS, AT
TB1	X00
TB2	X01
TB3	X02
TB4	X03
TB5	X04
TB6	X05
TB7	X06
TB8	X07
TB9	NON CONNECTION
TB10	X08
TB11	X09
TB12	X0A
TB13	X0B
TB14	X0C
TB15	X0D
TB16	X0E
TB17	X0F
TB18	COMMON1
TB19	NON CONNECTION
TB20	NON CONNECTION

OUTPUT

DR, AR, AS, AT	
DC24V	TB20
DC24G	TB19
SG	TB18
NON CONNECTION	TB17
NON CONNECTION	TB16
NON CONNECTION	TB15
NON CONNECTION	TB14
Y20	TB13
Y21	TB12
Y22	TB11
Y23	TB10
Y24	TB9
Y25	TB8
Y26	TB7
Y27	TB6
COMMON3	TB5
Y28	TB4
Y29	TB3
Y2A	TB2
Y2B	TB1

8	4	0
9	5	1
A	6	2
B	7	3

TB19	TB20
TB17	TB18
TB15	TB16
TB13	TB14
TB11	TB12
TB9	TB10
TB7	TB8
TB5	TB6
TB3	TB4
TB1	TB2

0	4	8	C
1	5	9	D
2	6	A	E
3	7	B	F

TB2	TB1
TB4	TB3
TB6	TB5
TB8	TB7
TB10	TB9
TB12	TB11
TB14	TB13
TB16	TB15
TB18	TB17
TB20	TB19

TB1	X10
TB2	X11
TB3	X12
TB4	X13
TB5	X14
TB6	X15
TB7	X16
TB8	X17
TB9	NC
TB10	X18
TB11	X19
TB12	X1A
TB13	X1B
TB14	X1C
TB15	X1D
TB16	X1E
TB17	X1F
TB18	COMMON2
TB19	NON CONNECTION
TB20	NON CONNECTION

Y2C	TB20
Y2D	TB19
Y2E	TB18
Y2F	TB17
COMMON4	TB16
Y30	TB15
Y31	TB14
Y32	TB13
Y33	TB12
Y34	TB11
Y35	TB10
Y36	TB9
Y37	TB8
COMMON5	TB7
NON CONNECTION	TB6
NON CONNECTION	TB5
AC 115V	TB4
AC 115V	TB3
LG	TB2
FG	TB1

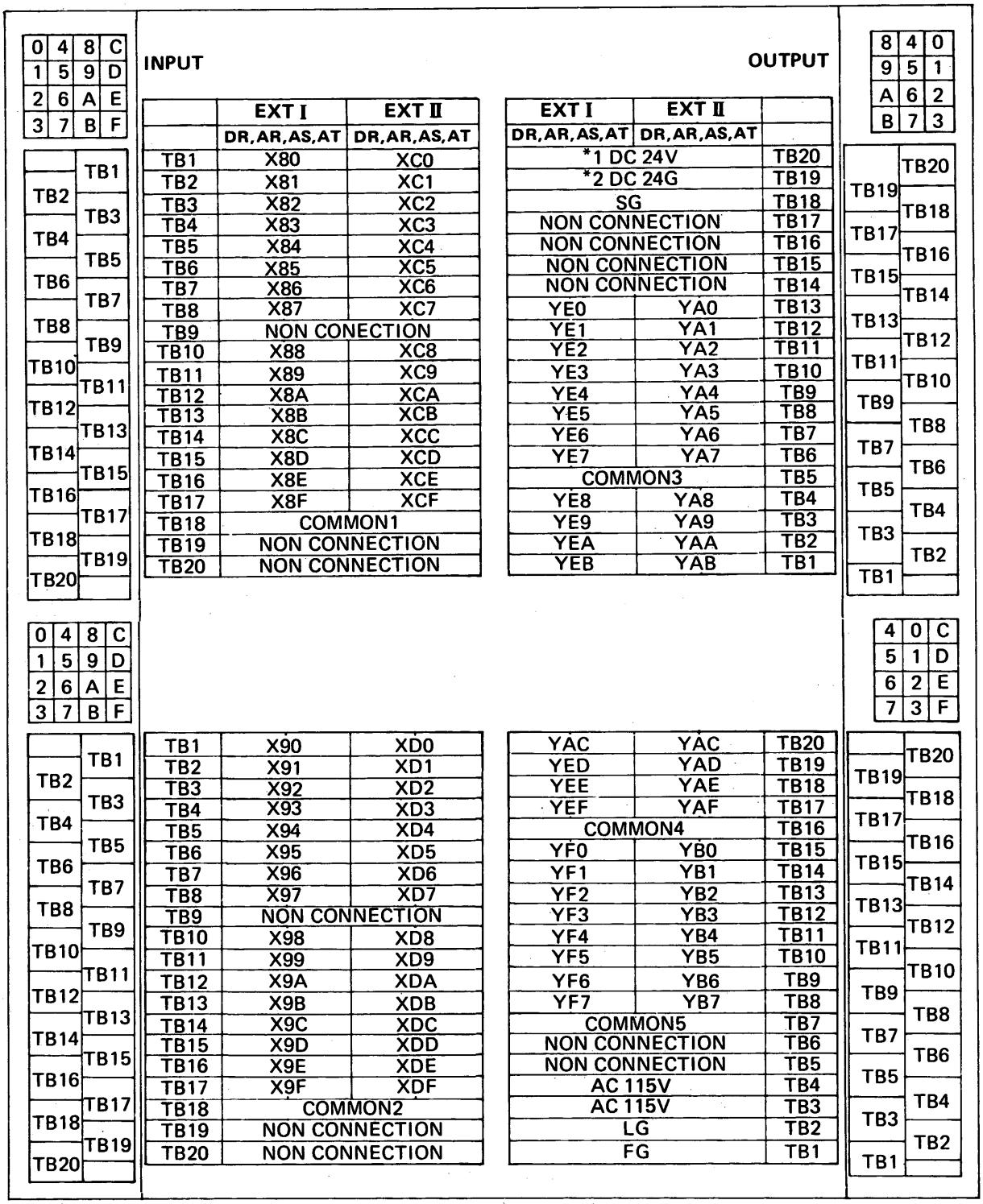
4	0	C
5	1	D
6	2	E
7	3	F

TB19	TB20
TB17	TB18
TB15	TB16
TB13	TB14
TB11	TB12
TB9	TB10
TB7	TB8
TB5	TB6
TB3	TB4
TB1	TB2

I/O No. allocation

IN	X00 ~ X0F	(16 points)
X	X10 ~ X1F	(16 points)
OUT	Y20 ~ Y2F	(16 points)
Y	Y30 ~ Y37	(8 points)

3.4.2 Terminal arrangement of Type E56 extension unit



0	4	8	C
1	5	9	D
2	6	A	E
3	7	B	F

INPUT

	EXT I	EXT II
	DR,AR,AS,AT	DR,AR,AS,AT
TB1	X80	XC0
TB2	X81	XC1
TB3	X82	XC2
TB4	X83	XC3
TB5	X84	XC4
TB6	X85	XC5
TB7	X86	XC6
TB8	X87	XC7
TB9	NON CONECTION	
TB10	X88	XC8
TB11	X89	XC9
TB12	X8A	XCA
TB13	X8B	XCB
TB14	X8C	XCC
TB15	X8D	XCD
TB16	X8E	XCE
TB17	X8F	XCF
TB18	COMMON1	
TB19	NON CONNECTION	
TB20	NON CONNECTION	

OUTPUT

EXT I	EXT II	
DR,AR,AS,AT	DR,AR,AS,AT	
*1 DC 24V		TB20
*2 DC 24G		TB19
SG		TB18
NON CONNECTION		TB17
NON CONNECTION		TB16
NON CONNECTION		TB15
NON CONNECTION		TB14
YE0	YA0	TB13
YE1	YA1	TB12
YE2	YA2	TB11
YE3	YA3	TB10
YE4	YA4	TB9
YE5	YA5	TB8
YE6	YA6	TB7
YE7	YA7	TB6
COMMON3		TB5
YE8	YA8	TB4
YE9	YA9	TB3
YEA	YAA	TB2
YEB	YAB	TB1

8	4	0
9	5	1
A	6	2
B	7	3

0	4	8	C
1	5	9	D
2	6	A	E
3	7	B	F

TB1	X90	XD0
TB2	X91	XD1
TB3	X92	XD2
TB4	X93	XD3
TB5	X94	XD4
TB6	X95	XD5
TB7	X96	XD6
TB8	X97	XD7
TB9	NON CONNECTION	
TB10	X98	XD8
TB11	X99	XD9
TB12	X9A	XDA
TB13	X9B	XDB
TB14	X9C	XDC
TB15	X9D	XDD
TB16	X9E	XDE
TB17	X9F	XDF
TB18	COMMON2	
TB19	NON CONNECTION	
TB20	NON CONNECTION	

YAC	YAC	TB20
YED	YAD	TB19
YEE	YAE	TB18
YEF	YAF	TB17
COMMON4		TB16
YF0	YB0	TB15
YF1	YB1	TB14
YF2	YB2	TB13
YF3	YB3	TB12
YF4	YB4	TB11
YF5	YB5	TB10
YF6	YB6	TB9
YF7	YB7	TB8
COMMON5		TB7
NON CONNECTION		TB6
NON CONNECTION		TB5
AC 115V		TB4
AC 115V		TB3
LG		TB2
FG		TB1

4	0	C
5	1	D
6	2	E
7	3	F

I/O No. allocation

	EXTENSION I		EXTENSION II	
IN X	X80 ~ X8F	(16 points)	XC0 ~ XCF	(16 points)
	X90 ~ X9F	(16 points)	XD0 ~ XDF	(16 points)
OUT Y	XA0 ~ XAF	(16 points)	YE0 ~ YEF	(16 points)
	XB0 ~ XBF	(8 points)	YF0 ~ YF7	(8 points)

*1, *2 To be unilized only when extension power supply is used with E56AS.

3.4.3 Terminal arrangement of Type E32 extension unit

EXTENSION I

0	4	8	C
1	5	9	D
2	6	A	E
3	7	B	F

	TB1
TB2	
	TB3
TB4	
	TB5
TB6	
	TB7
TB8	
	TB9
TB10	
	TB11
TB12	
	TB13
TB14	
	TB15
TB16	
	TB17
TB18	
	TB19
TB20	

	DR, AR, AS, AT
TB1	X80
TB2	X81
TB3	X82
TB4	X83
TB5	X84
TB6	X85
TB7	X86
TB8	X87
TB9	NON CONNECTION
TB10	X88
TB11	X89
TB12	X8A
TB13	X8B
TB14	X8C
TB15	X8D
TB16	X8E
TB17	X8F
TB18	COMMON1
TB19	NON CONNECTION
TB20	FG

DR, AR, AT	AS	
DC 24V	NC	TB20
DC 24G	NC	TB19
YA0		TB18
YA1		TB17
YA2		TB16
YA3		TB15
YA4		TB14
YA5		TB13
YA6		TB12
YA7		TB11
COMMON2		TB10
YA8		TB9
YA9		TB8
YAA		TB7
YAB		TB6
YAC		TB5
YAD		TB4
YAE		TB3
YAF		TB2
COMMON3		TB1

C	8	4	0
D	9	5	1
E	A	6	2
F	B	7	3

	TB20
TB19	
	TB18
TB17	
	TB16
TB15	
	TB14
TB13	
	TB12
TB11	
	TB10
TB9	
	TB8
TB7	
	TB6
TB5	
	TB4
TB3	
	TB2
TB1	

IN X	X80 ~ X8F (16 points)
OUT Y	XA0 ~ XAF (16 points)

EXTENSION II

0	4	8	C
1	5	9	D
2	6	A	E
3	7	B	F

	TB1
TB2	
	TB3
TB4	
	TB5
TB6	
	TB7
TB8	
	TB9
TB10	
	TB11
TB12	
	TB13
TB14	
	TB15
TB16	
	TB17
TB18	
	TB19
TB20	

	DR, AR, AS, AT
TB1	XC0
TB2	XC1
TB3	XC2
TB4	XC3
TB5	XC4
TB6	XC5
TB7	XC6
TB8	XC7
TB9	NON CONNECTION
TB10	XC8
TB11	XC9
TB12	XCA
TB13	XCB
TB14	XCC
TB15	XCD
TB16	XCE
TB17	XCF
TB18	COMMON 1
TB19	NON CONNECTION
TB20	FG

DR, AR, AT	AS	
DC 24V	NC	TB20
DC 24G	NC	TB19
YE0		TB18
YE1		TB17
YE2		TB15
YE3		TB15
YE4		TB14
YE5		TB13
YE6		TB12
YE7		TB11
COMMON 2		TB10
YE8		TB9
YE9		TB8
YEA		TB7
YEB		TB6
YEC		TB5
YED		TB4
YEE		TB3
YEF		TB2
COMMON 3		TB1

C	8	4	0
D	9	5	1
E	A	6	2
F	B	7	3

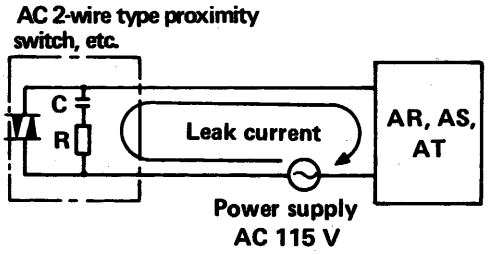
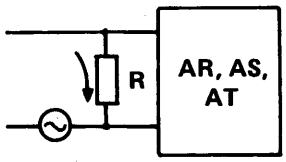
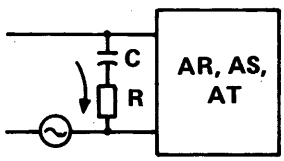
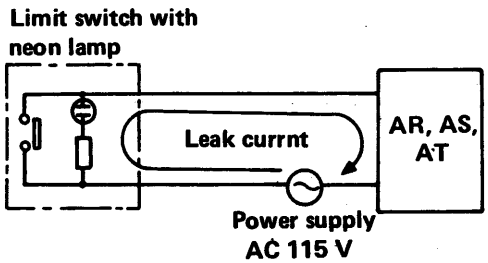
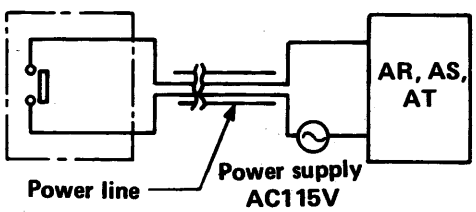
	TB20
TB19	
	TB18
TB17	
	TB16
TB15	
	TB14
TB13	
	TB12
TB11	
	TB10
TB9	
	TB8
TB7	
	TB6
TB5	
	TB4
TB3	
	TB2
TB1	

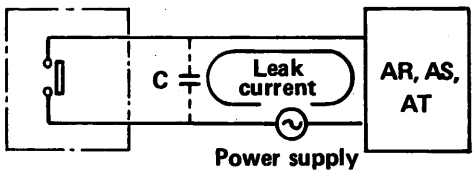
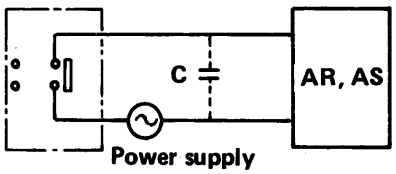
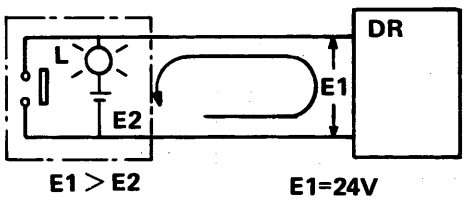
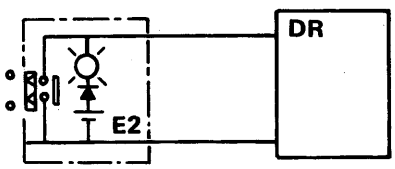
IN X	XC0 ~ XCF (16 points)
OUT Y	YE0 ~ YEF (16 points)

3.5 Cautions and Corrective Actions for Input and Output Circuits

3.5.1 Cautions and corrective actions for input circuits

Table 3.5.1

Ex.	Condition	Cause	Corrective Action
1	Though triac is not on, input turns on. Though triac is turned off, input fails to turn off.	Input is turned on by leak current from the CR absorber used to protect triac from surge.  This occurs in AR, AS, or AT when leak current excedds 4 mA.	Connect resistor or series co-mbination of resistor and capacitor as shown below in order to reduce input impedance so that voltage across input terminals of input unit is lower than input operation "off" voltage.  Example: 15KΩ 2W  Example: CR: 0.5μF + 50Ω
2	Though limit switch is not on, turns on. Though limit switch is turned off, input fails to turn off.	When limit switch is provided with neon lamp, input is turned on by leak current caused by neon lamp. 	
3	Same as example 2.	In case input signal line is wired long distance in parallel to other power line, etc., input turns on because voltage is induced by induced voltage from power line. 	*Note: Determine R and CR values depending on leak current values.* *When only resistors is used, more heat is generated.* *If possible, use the combination of resistor and capacitor.* *This combination produces an effect also on large surge.*

Ex.	Condition	Cause	Corrective Action
4	Same as example 2.	Input is turned on by leak current caused by line-to-line capacity across wired cable. 	(a) Same as examples 1, 2, and 3. (b) As shown below, provide power supply on limit switch side. 
5	Same as example 2. Though limit switch is not on, lamp turn on.	With 2 power supplies used, since E1 voltage is larger than E2 voltage, unidentified flowing current flows as show below. 	(a) Use 1 power supply. (b) Take action so that E1 ≦ E2 is established. (c) Connect snake path prevention diode as shown below. 

Input cable wiring

Input has many problems of wrong input and noise. These problems can be reduced by the aforementioned corrective actions and the following wiring method.

(1) Input signal cable shall not be bundled or provided close to high-voltage and large-current power lines and main circuit line. If possible, keep it more than 100 mm away from the aforementioned lines.

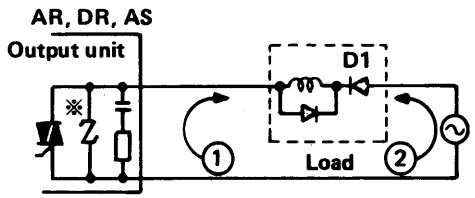
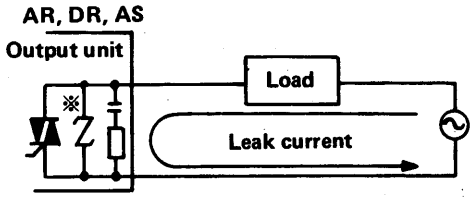
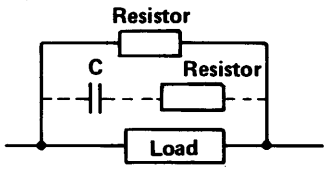
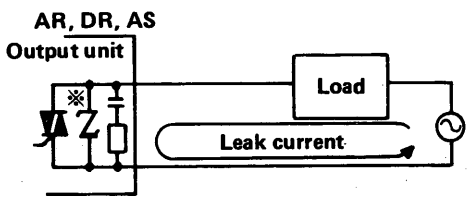
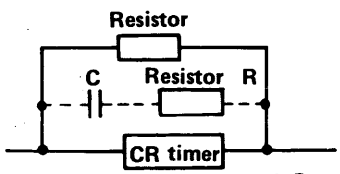
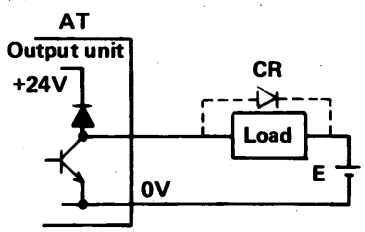
(2) When wiring is made at 200 mm or longer distance with AR, AS or AT, prblem indicated in example 4 of Table 3.5.1 arises with only the use of 2 cables connected with input device. In this case, take corrective cation described in examples 1 and 2 or provide an intermediary relay.

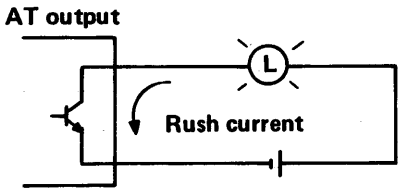
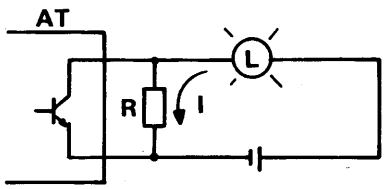
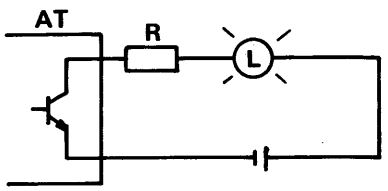
(3) When shielded cable is used, shield coating shall be ground in a bundle at 1 point on the sequencer side. If both ends are ground, current will flow through the shield coating and therefore shielding effect is not produced at all.

(4) When conduit wiring is made by means of metal pipe, ground the pipe securely.

3.5.2 Cautions and corrective actions for output circuits

Table 3.5.2

Condition	Cause	Corrective Action
–Example 1– When output off, ecess voltage is applied to load.	○ Load is half-wave rectified internally (seen in some solenoids)  ○ When power supply polarity is as shown by ①, C is charged. When polarity is as shown by ②, voltage charged in C plus line voltage are applied across D1. Max. voltage is approx. 2√2E.	○ Connect resistor of several ten K across load. *Note: When resistor is used in this way, it does not offer problem to output elemnt, be may sometimes cause the diode, which is built in the load, to deteriorate or burn.*
–Example 2– Load does not turn off.	○ Leak current caused by built-in snubber. This is especially liable to occur in the case of small-capacity load. 	○ Connect resistor of approx. several ten K across load. *Note: In case wiring distance from output card to load is long, take care because there may exist leak current due to line-to-line capacity.* ○ Connect C and R across load.  CR: 0.1 ~ 0.47μF + 47 ~ 120 Ω
–Example 3– When motor type or C, R type timer is used as load, time limit fluctuates.		○ After driving relay, drive timer at the same contact. ○ Connect C and R across CR timer.  CR: 0.1 ~ 0.47μF + 47 ~ 120 Ω
–Example 4– Load fails (for direct current).	○ Circulation occurs because 2 power supplies are used.  ○ If +24V < E, circulation occurs.	○ Use load power supply of DC 24 V. ○ Connect circulation preventive diode. (See note.) *Note: In case relay or the like is used as load, it is necessary to connect reverse voltage absorbing diode (shown in dotted line in figure at left) with load.*

Condition	Cause	Corrective Action
—Example 5— Output transistor is destroyed.	In case transistor is used for output and lamp is used as load, since inrush current flows through lamp when transistor turn on, output transistor is destroyed.  Since AT has max. withstand rush current or 10A (10 msec), rush current for lamp should be below this value.	(a) Provide resistor as shown below so that small current, which will not turn on the flows at all times, in order to prevent rush current from generating. Example I : rush current x 1/3 ~ 1/4  (b) Provide resistor as shown below to restrict rush current. 

Output cable wiring

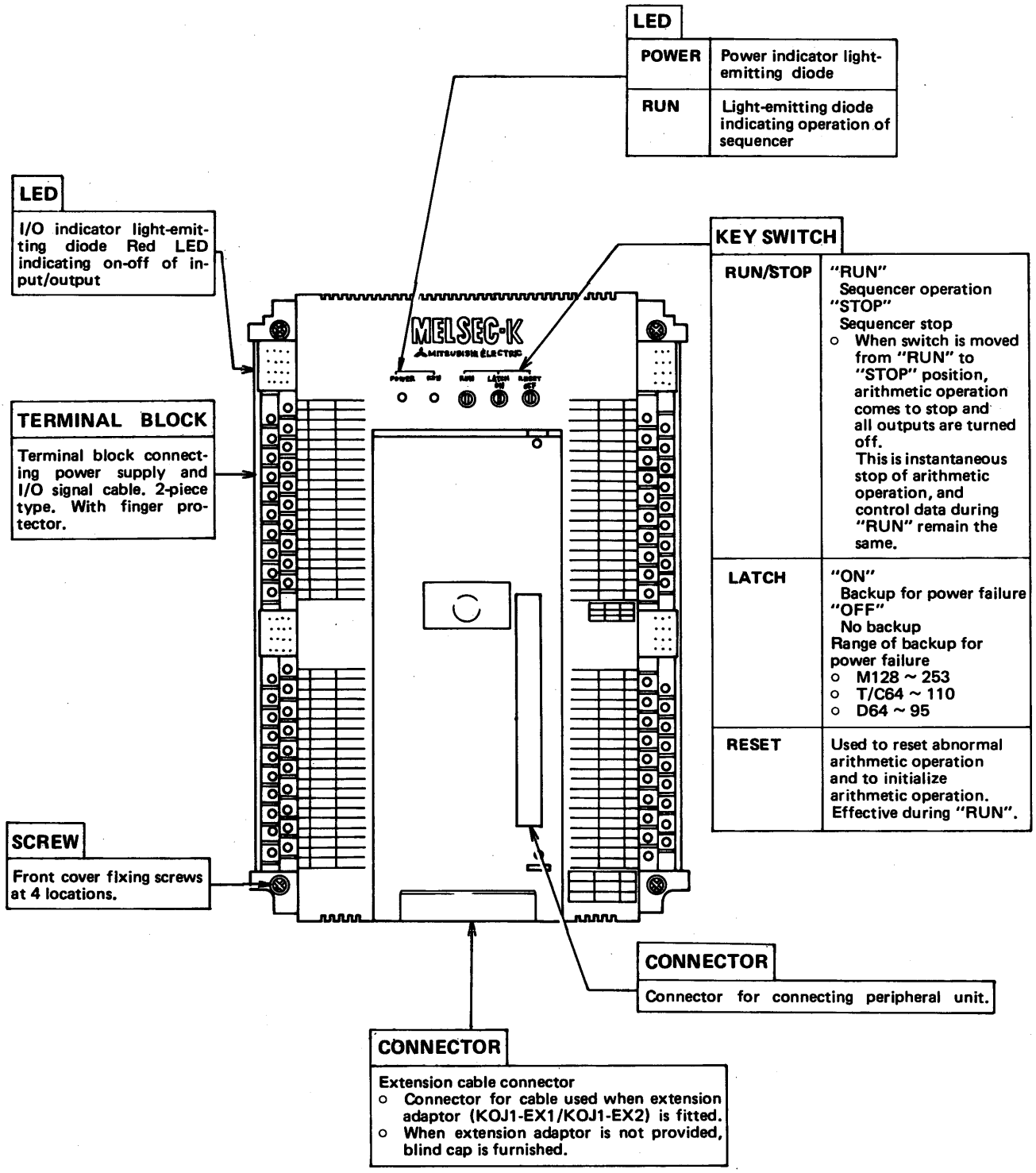
(1) Keep output cable as far away as possible from input cable.
(2) Since leak current due to line-to-line capacity is generated in addition to the leak current of output in the case of wiring at 200 m or longer distance, it is necessary to take action mentioned in Example 2 of Table 3.5.2.
(3) Take care to prevent contact with cable at different potential and to prevent grounding.
(4) Keep DC output line as far away as possible from AC line.

MEMO

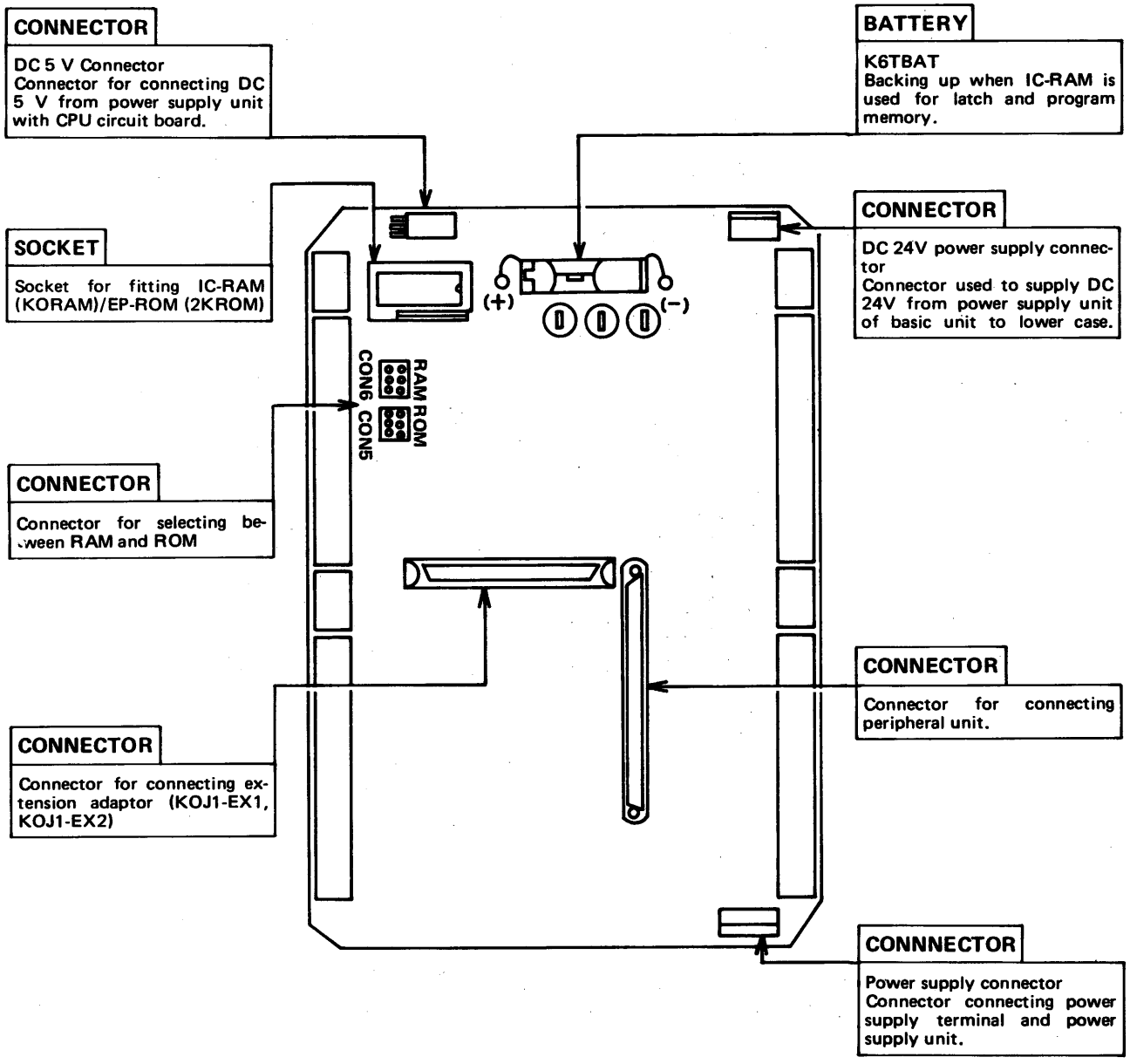
4. NOMENCLATURE AND CONFIGURATION

4. NOMENCLATURE AND CONFIGURATION

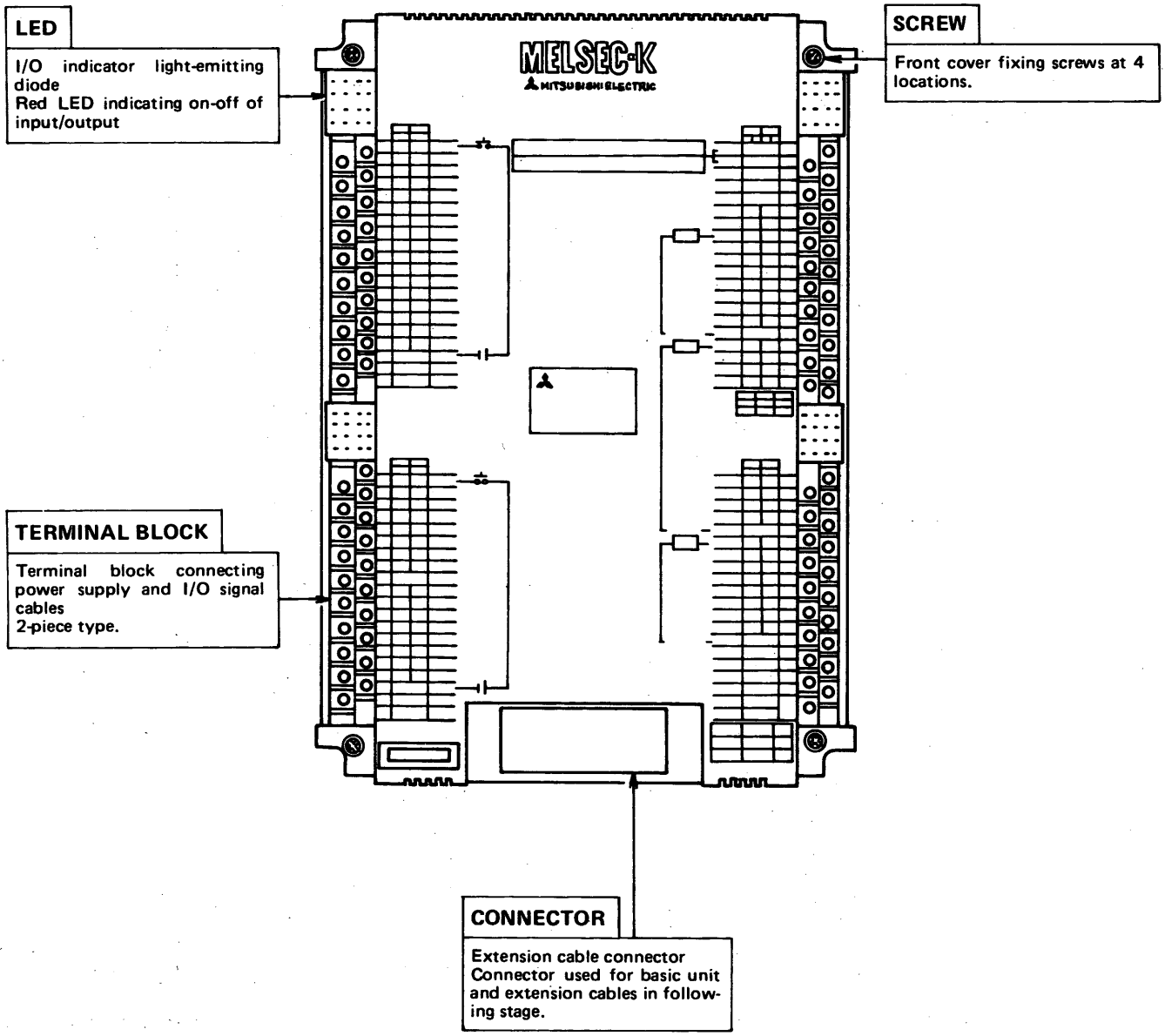
4.1 External View of Basic Unit



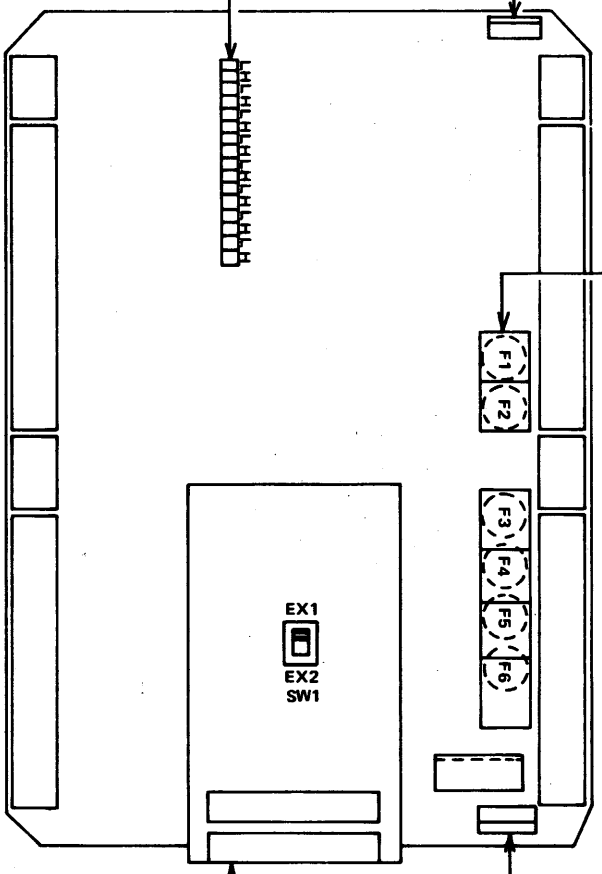
Internal Configuration of Basic Unit



4.2 External View of Type 56 Extension Unit



Internal Configuration of Type 56 Extension Unit



SWITCH

Switch for selecting high-speed input. First 8 points (X0 to X7) are provided with high-speed select switches. Basic unit is also provided with these switches. At shipment, the switch is in L position.

	Response speed
H L	5 mS
H L	0.5 mS

Note: High-speed input selection switchis incorporated only in DR.

CONNECTOR

DD 24 V power supply connector
Connector used to supply DC 24 V from power supply of unit to lower case when extension power supply is used.

FUSE

Fuse for protection of output short circuit
GLL7 for relay output
GGC3 for transistor output
GTH-5 for triac output

	Basic	Ext. I	Ext. II
F1:	Y20 /	YA0 /	E0 ~
	Y23 /	YA3 /	YE3
F2:	Y24 /	YA4 /	E4 ~
	Y27 /	YA7 /	YE7
F3:	Y28 /	YA8 /	YE8 ~
	Y2B /	YAB /	YEB
F4:	Y2C /	YAC /	YEC ~
	Y2F /	YAF /	YEF
F5:	Y30 /	YB0 /	YF0 ~
	Y33 /	YB3 /	YF3
F6:	Y34 /	YB4 /	YF4 ~
	Y37 /	YB7 /	YF7

F7: Power supply fuse GGC3 (3A)

CONNECTOR

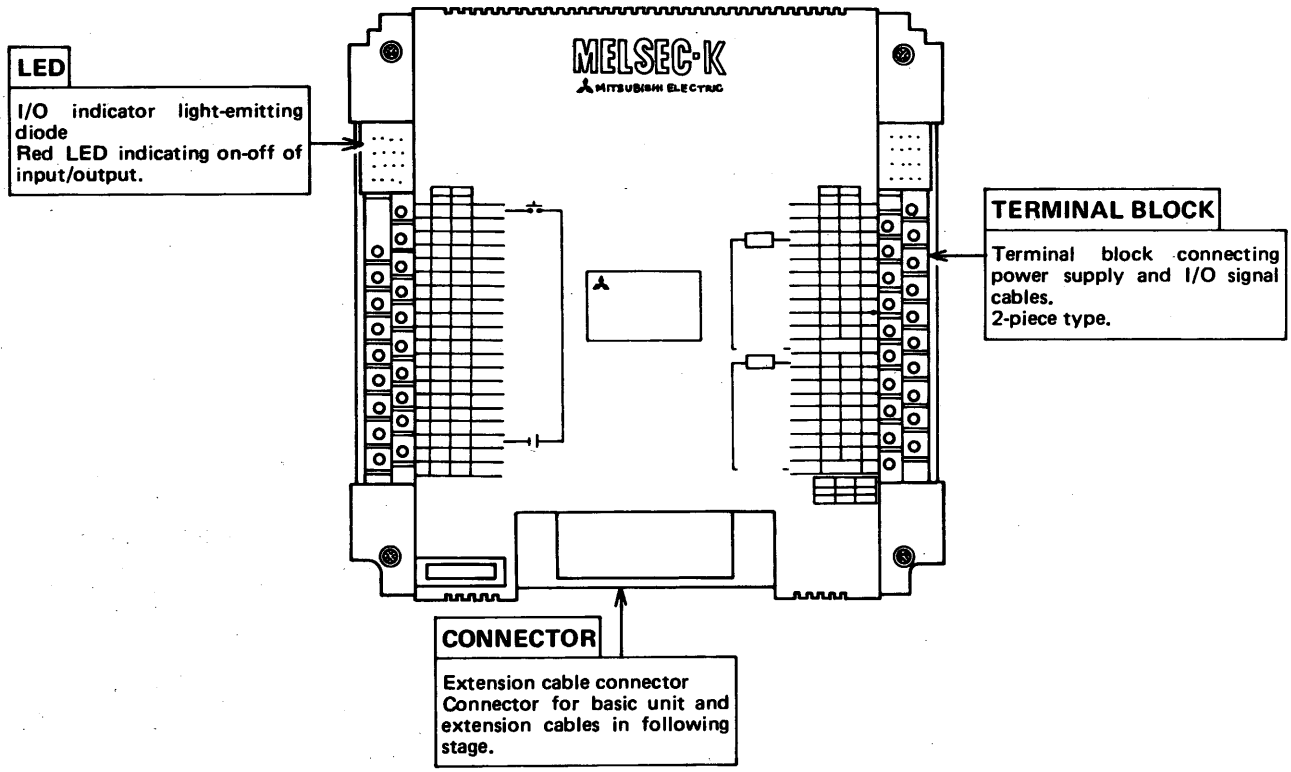
Power supply connector
Connector connecting power supply terminal block and power supply unit when extension power supply is used.

ADAPTOR

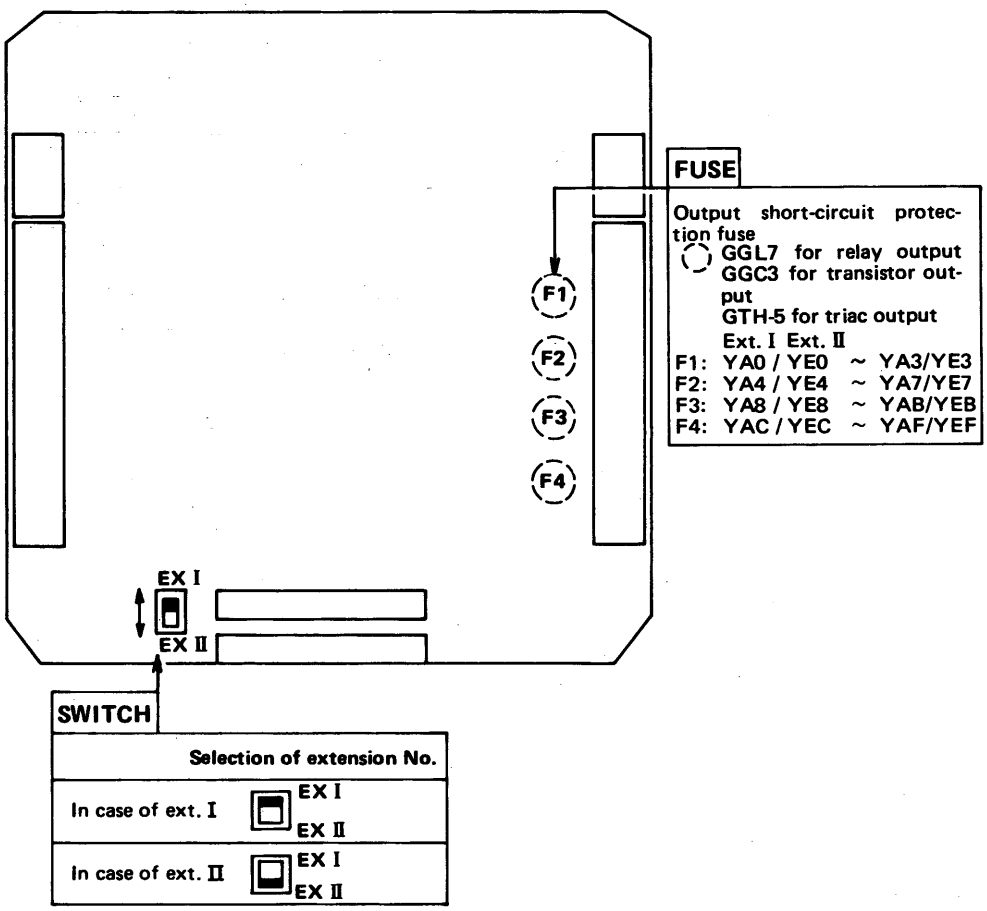
Extension adaptor

Selection of SW1 In case of ext. I	EX I / EX II
In case of ext. II	EX I / EX II

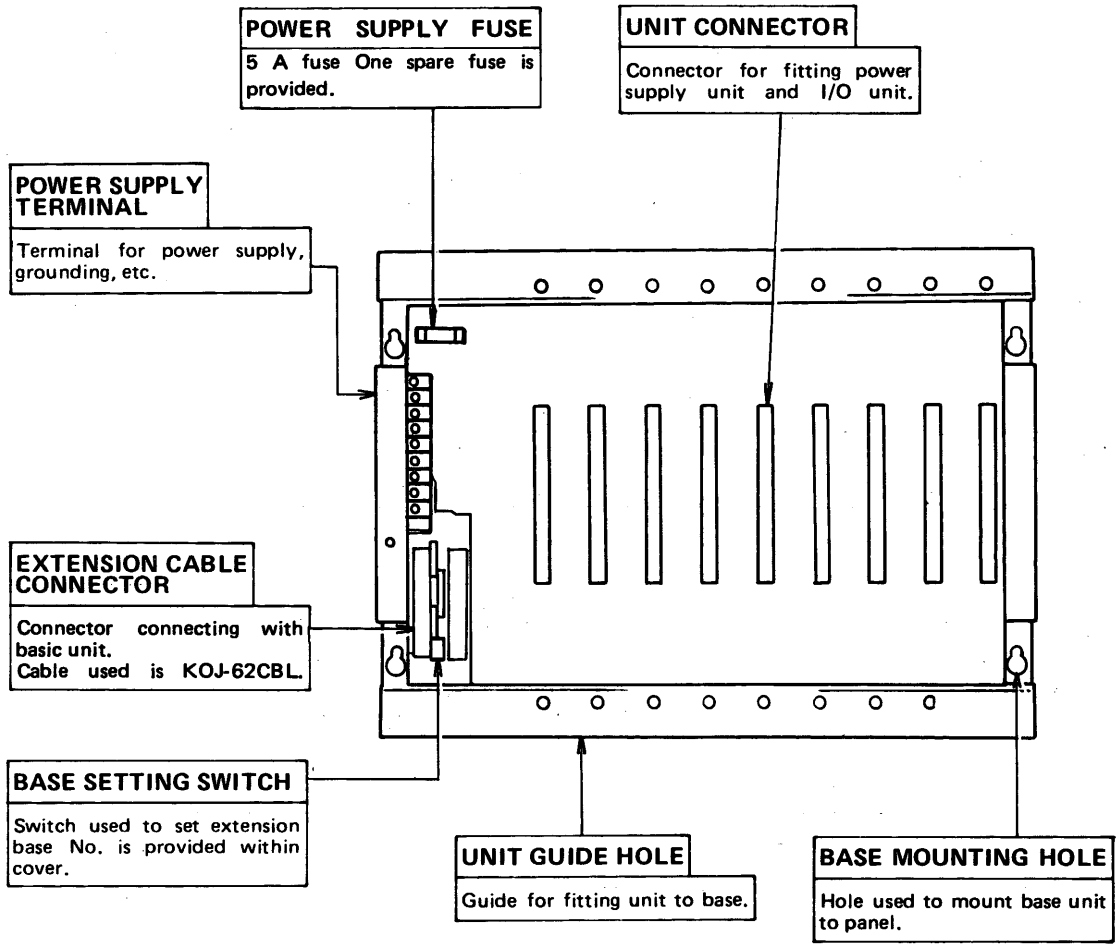
4.3 External View of Type 32 Extension Unit



Internal Configuration of Type 32 Extension Unit



4.4 External View of K68B Extension Base Unit



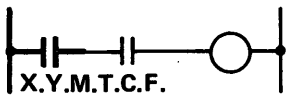
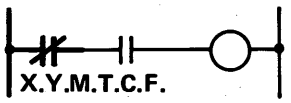
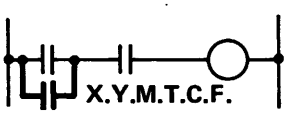
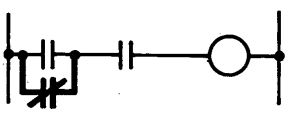
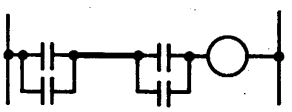
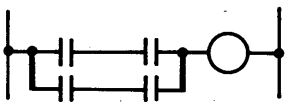
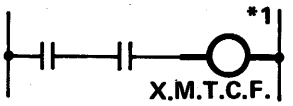
MEMO

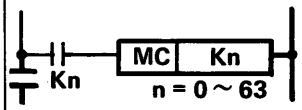
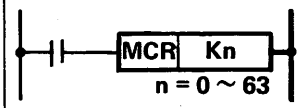
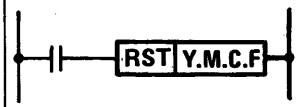
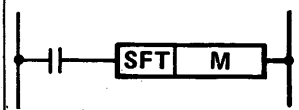
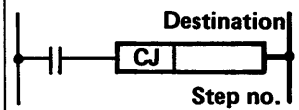
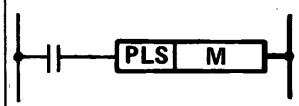
5. EXPLANATION OF PROGRAM

5.1 INSTRUCTION

- Sequence Instructions

Table 5.1.1

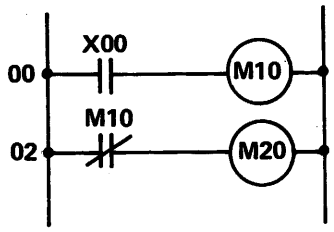
No.	Ins. code	Instruction	Symbol
1	LD	Load	
2	LDI	Load inverse	
3	AND	And	
4	ANI	And inverse	
5	OR	OR	
6	ORI	OR inverse	
7	ANB	And block	
8	ORB	OR block	
9	OUT	Out	

No.	Ins. code	Instruction	Symbol
10	MC	Master control	
11	MCR	Master control reset	
12	SET	Set memory	
13	RST	Reset memory & counter	
14	SFT	Shift memory	
15	CJ	Conditional jump	
16	PLS	Pulse generate	
17	NOP	No operation	Use for program delete or space
18	END	End	Return to step 0. END definitely entered at end of program

Note: Instructions for timer and counter-values can be entered using constant K or data register D.
Out T.C and CJ are 2-word instructions and all others are 1-step instructions.

5.2 Explanation of Instruction

5.2.1 Load (LD)/load inverse (LDI)/out (OUT)



Coding

Step	Instruction
0000	LD X00
0001	OUT M10
0002	LDI M10
0003	OUT M20

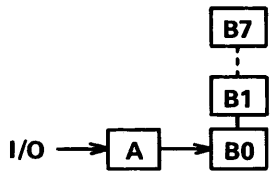
Register content

A	B0
X00	X00
X00	X00
M10	M10
M10	M10

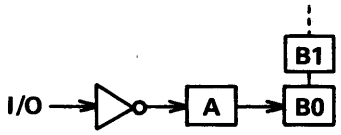
LD	Contact "a" arithmetic operation start instruction
LDI	Contact "b" arithmetic operation start instruction
OUT	Output instruction

● Arithmetic operation principle

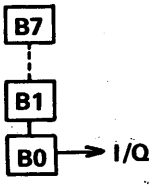
LD Specific I/O No. content (on or off) is stored into answer register A and the result is transferred to the lowest order B0 of auxiliary registers (B0 ~ B7).



LDI Specific relay No. content is inversed and stored into register A.

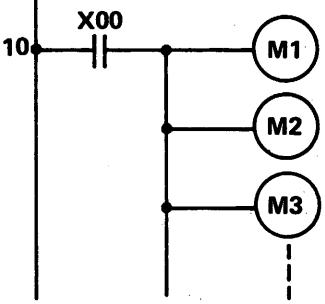


OUT Content in register B is output to specific relay No.



At this time, content in register B does not change.

● Consecutive OUT instructions

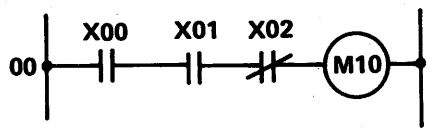


Step	Instruction
0010	LD X00
0011	OUT M1
0012	OUT M2
0013	OUT M3

OUT instruction can be consecutively used for program.

Note: The number of consecutive OUT instructions is up to 22 in the case of GPP and HGP.

5.2.2 And (AND)/and inverse (ANI)



Coding

Step	Instruction
0000	LD X00
0001	AND X01
0002	ANI X02
0003	OUT M10

Register content

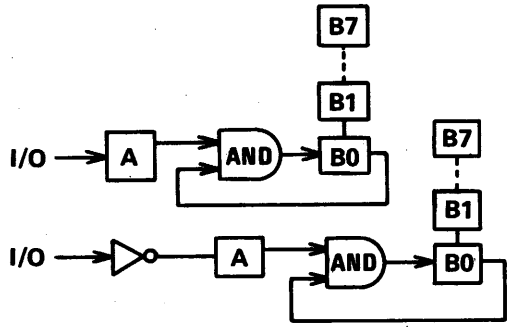
A	B
X00	X00
X00 X01	X00 X01
X00 X01 X02	X00 X01 X02
X00 X01 X02	X00 X01 X02

AND Contact "a" series connection

ANI Contact "b" series connection

- Arithmetic operation principle

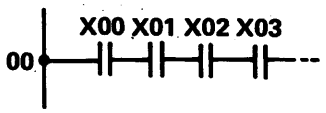
  AND . . AND or ANI operation of specific relay No. content is performed with register B0
  ANI and the result is stored into register B0.



- Number of contacts

  The number of contacts is limitless. AND or ANI can be used consecutively for any number of contacts.

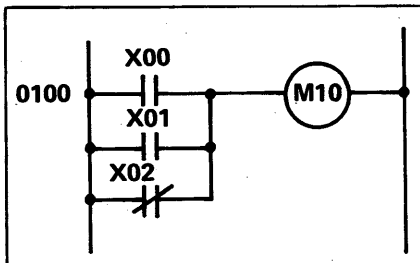
Note: Consecutive contact writing by GPP and HGP with circuit mode is allowed up to 161 contacts.



Step	Instruction
0000	LD X00
0001	AND X01
0002	AND X02
0003	AND X03
⋮	⋮

In this case, since the contact for the 1st relay No. X00 is logic start, it is programmed as "LD X00".

5.2.3 Or (OR)/or inverse (ORI)



Coding

Step	Instruction
0100	LD X00
0101	OR X01
0102	ORI X02
0103	OUT M10

Register content

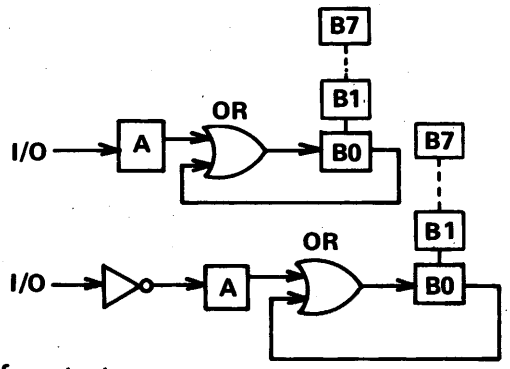
A	B0
X00	X00
X00 X01	X00 X01
X00 X01 X02	X00 X01 X02
X00 X01 X02	X00 X01 X02

OR ..... Contact "a" parallel connection

ORI ..... Contact "b" parallel connection

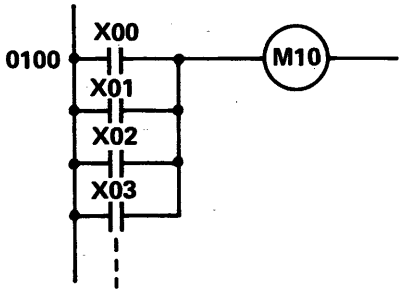
- Arithmetic operation principle

  OR ... OR or ORI operation of specific relay No. Content is performed with register B0
  ORI and the result is stored into B0.



- Number of contacts

  The number of contacts is limitless. OR or ORI can be used consecutively for any number of contacts.

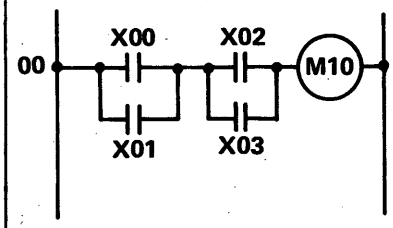


Step	Instruction
0100	LD X00
0101	OR X01
0102	OR X02
0103	OR X03
⋮	⋮
⋮	OUT M10

Note: The number of consecutive parallel contacts by GPP and HGP is to 22.

In this case, since the first X00 is logical start, it is programmed as "LDX00".

5.2.4 And block (ANB)



Coding

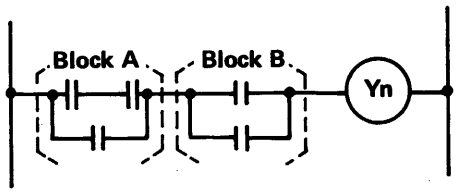
Step	Instruction
0000	LD X00
0001	OR X01
0002	LD X02
0003	OR X03
0004	ANB
0005	OUT M10

Register content

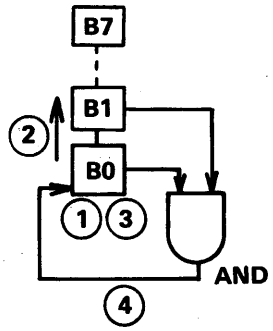
A	B0	B1
⊣⊢	⊣⊢	—
⊓⊔	⊓⊔	—
⊣⊢	⊣⊢	⊓⊔
⊓⊔	⊓⊔	⊓⊔
⊓⊔⊓⊔	⊓⊔⊓⊔	—
⊓⊔⊓⊔	⊓⊔⊓⊔	—

ANB Block-to-block series connection arithmetic operation

- Arithmetic operation principle

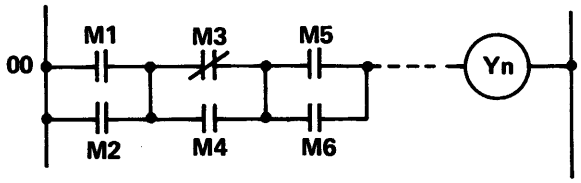


① First, the arithmetic operation result of block A is stored in register B0.
② When the arithmetic operation of block B is initiated, content in B0 is transferred to B1.
③ The arithmetic operation result of block B is stored in B0.
④ AND operation of B0 content and B1 content is performed by "ANB" instruction, and the result is stored in B0 again.



- Number of blocks

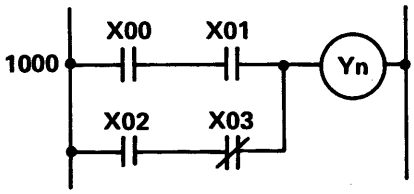
*1 The number of AND bolcks (ANBs) is limitless.



Step	
0000	LD M1
0001	OR M2
0002	LDI M3
0003	OR M4
0004	ANB
0005	LD M5
0006	OR M6
0007	ANB
⋮	⋮
⋮	OUT Yn

*1 When ANB is utilized consecutively, use programming of ANB instruction per block.

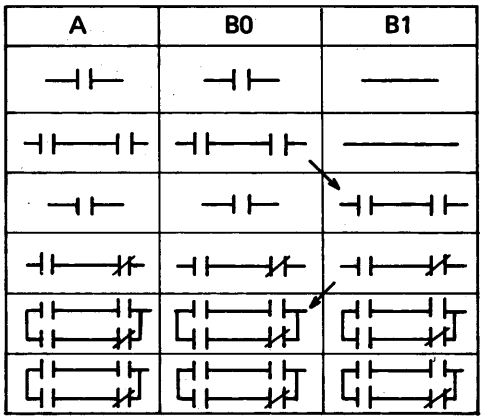
5.2.5 Or block (ORB)



Coding

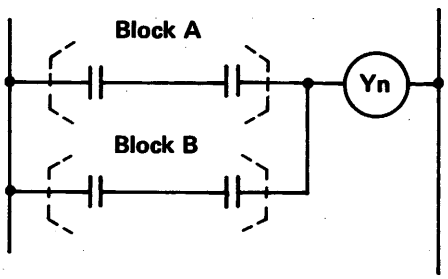
Step	Instruction
1000	LD X00
1001	AND X01
1002	LD X02
1003	ANI X03
1004	ORB
1005	OUT Yn

Register content

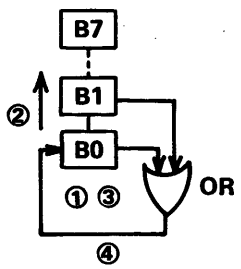


ORB Block-to-block parallel connection

- Arithmetic operation principle

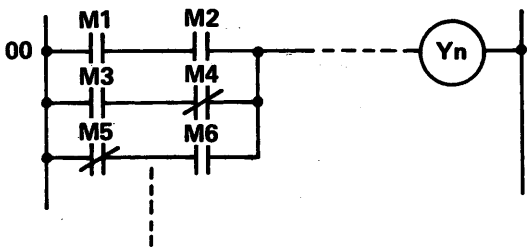


① First, the arithmetic operation result of block A is stored in register B0.
② When the arithmetic operation of block B is initiated, content in B0 is transferred to B1.
③ The arithmetic operation result of block B is stored in B0.
④ OR operation of B0 content and B1 content is performed by "ORB" instruction, and the result is stored in B0 again.



- Number of blocks

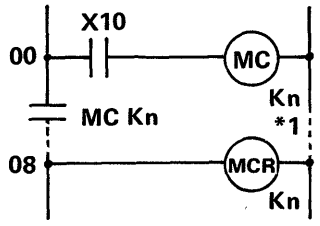
*1 The number of OR blocks (ORBs) is limitless.



Step	Instruction
0000	LD M1
0001	AND M2
0002	LD M3
0003	ANI M4
0004	ORB
0005	LDI M5
0006	AND M6
0007	ORB
⋮	⋮
⋮	OUT Yn

*1 When ORB is utilized consecutively, use programming of ORB instruction per block.

5.2.6 Master control (MC)



Coding

Step	Instruction
0000	LD X10
0001	MC Kn
⋮	⋮
0008	MCR Kn

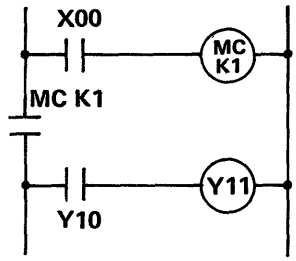
*1 n = 0 ~ 63

MC	Master control start
MCR	Master control reset

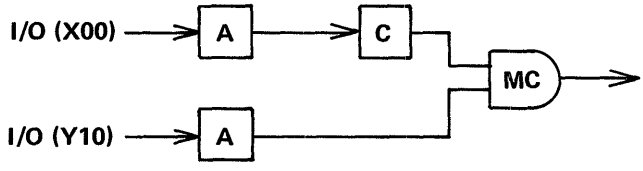
By opening and closing the common line of control circuit for either instruction, effective circuit can be made up.

5

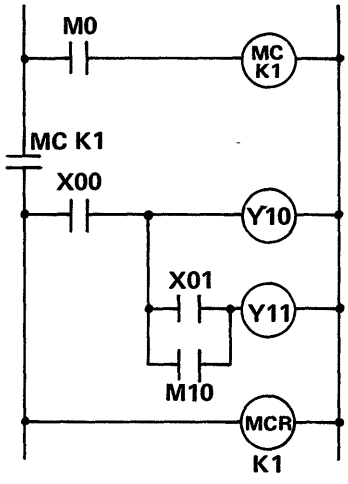
- Arithmetic operation principle



(1) I/O data (X00) is placed in register A and then the content in register A is transferred to register C.
(2) AND operation of I/O data (Y10) and register C content is performed, and OUT Y11 is executed.

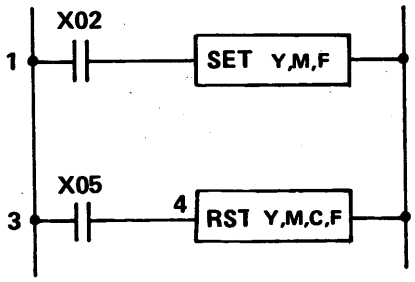


MC and MCR require index No. "Kn". Be sure to provide MCR Kn for MC Kn.



Step	Instruction
0000	LD M0
0001	MC K1
0002	LD X00
0003	OUT Y10
0004	LD X01
0005	OR M10
0006	ANB
0007	OUT Y11
0008	MCR K1

5.2.7 Set, reset (SET, RST)



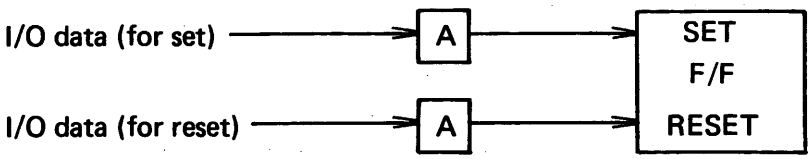
SET Flip-flop set
RST Flip-flop reset

Coding

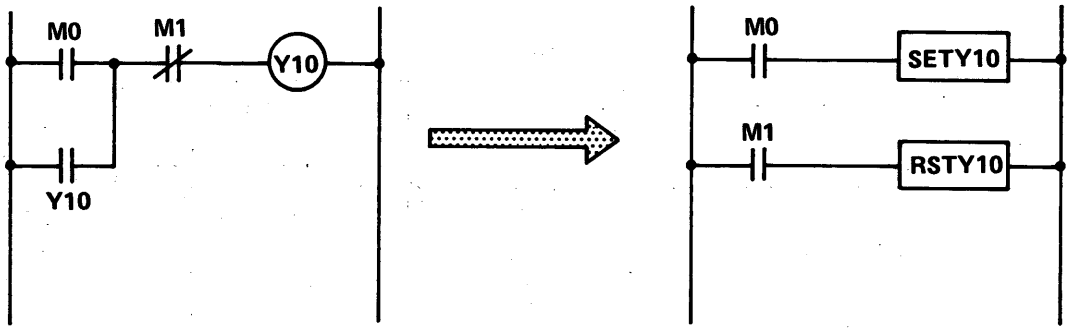
● Set, reset of Y · Set, reset of M · Set, reset of F

Step	Instruction	Instruction	Instruction
0001	LDX 02	LDX 02	LDX 02
0002	SET Y10	SET M00	SET F00
0003	LDX 05	LDX 05	LDX 05
0004	RST Y10	RST M00	RST F00

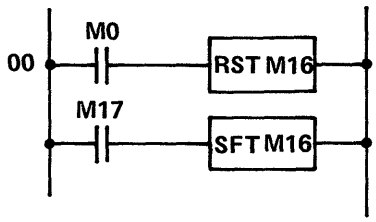
● Arithmetic operation principle



When I/O data for set are input, internal flip-flop is set. When I/O data for reset are input, flip-flop is reset.



5.2.8 Shift instruction (SFT)

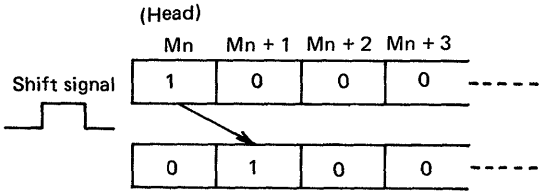


Coding

Step	Instruction
0000	LD M0
0001	RST M16
0002	LD M17
0003	SFT M16

SFT Temporary memory shift

- Arithmetic operation principle

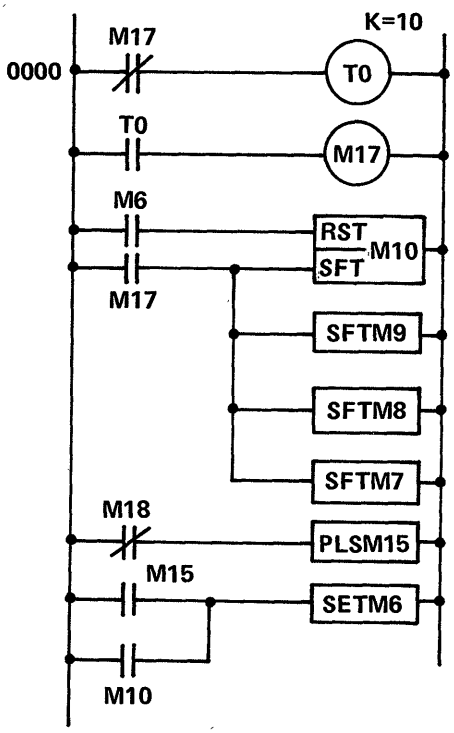


By giving SFT instruction to temporary memory (M), 1-bit shift register can be constituted.

If Mn-1 = 1 → Mn = 1
If Mn-1 = 0 → Mn = 0
} Establish Mn = 0 after SFT instruction.

It is necessary to set Mn, which is the head of shift register, at "1" by SET instruction.

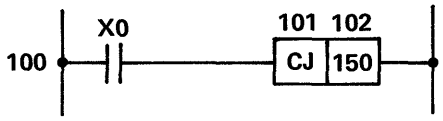
Note: Do not give SFT instruction to M0 because M255 may possibly shift to M0. For the same reason, do not give SFT instruction to M254.



Step	Instruction
0000	LDI M17
0001	OUT T0
0002	K10
0003	LD T0
0004	OUT M17
0005	LD M6
0006	RST M10
0007	LD M17
0008	SFT M10
0009	SFT M9
0010	SFT M8
0011	SFT M7
0012	LDI M18

Step	Instruction
0013	PLS M15
0014	LD M15
0015	OR M10
0016	SET M6

5.2.9 Conditional jump instruction (CJ)



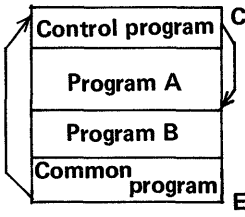
Coding

Step	Instruction
0100	LD X0
0101	CJ
0102	K150

CJ Conditional jump

*1 Unnecessary circuit is jumped temporarily.
Process circuit is separated depending on conditions in order to perform high-speed arithmetic operation processing.

- Arithmetic operation principle
  By conditional jump instruction, program seuqence skips to jump destination and the programs from the jump destination on are executed.



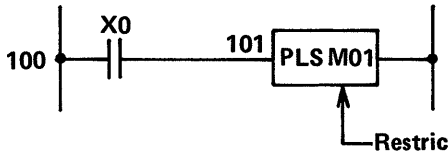
By using CJ instruction, it is possible to force the program sequence to jump the program which is normally not required (program A) and to execute on necessary programs. Therefore, scan time can be economized, and at the same time, program can be separated.

Differences between Master Control (MC) and Conditional Jump (CJ)

Item	MC	CJ
Operation time	Unchanged	Reduced
Program	Complicated	Simplified
Step control	Not required	Required*1

*1 It is necessary to specify the jump destination. Therefore, it is required to control the step No. Especially when instruction is inserted or deleted in debugging of program, the step No. of jump destination changes. However, the step No. is automatically altered in the case of PU, GPP and HGP.

5.2.10 Pulse instruction (PLS)



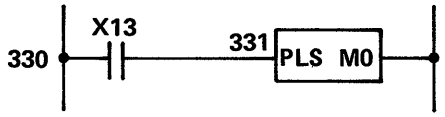
Coding

Step	Instruction
0100	LD X0
0101	PLS M01

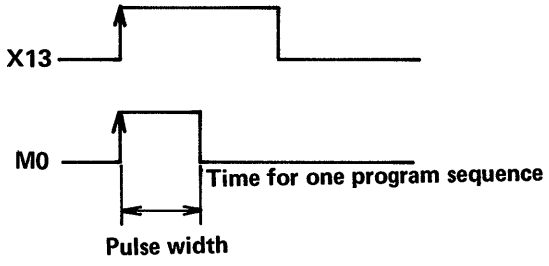
PLS Pulse generation

Pulse signals for one program sequence are generated.

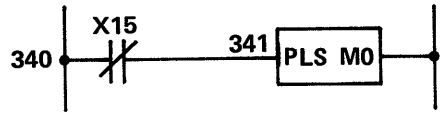
Leading edge detection pulse



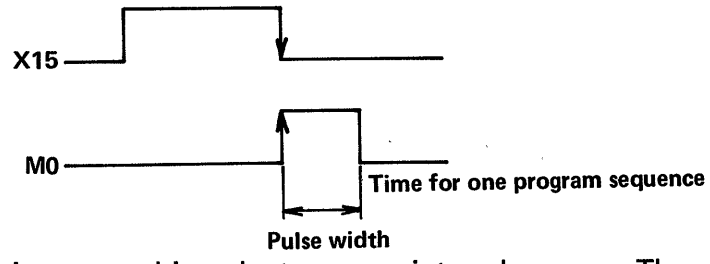
Step	Instruction
0330	LD X13
0331	PLS M0



Trailing edge detection pulse



Step	Instruction
0340	LDI X15
0341	PLS M0



- This pulse is generated in order to process internal program. Therefore, it cannot be used as a pulse signal by drawing it to the exterior.

5.2.11 No operation (NOP) ..... instruction used to progress the program unique to sequencer.

NOP	No operation

NOP is a no operation instruction and has no influence on the results of preceding arithmetic operation. An effective use of this instruction is to write NOP per desired step when preparing a program and to delete it when the program is completeld.

* Although NOP is a no operation instruction, the use of this instruction results in loss of scan time because the step with NOP is not skipped but scanned.

5.2.12 END instruction (END)

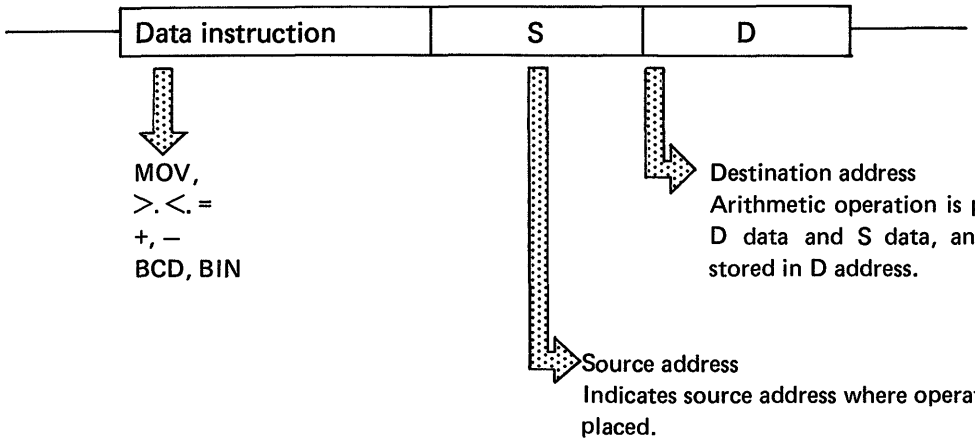
END	Program end
	Write this at the end of program.

END is entered at the end of a required program step to declare the end of the program. The CPU returns the program counter to "0" and initiates scanning again from the step No. "0".

The END Instruction can also be utilized temporarily at the time of program debugging or test and also when program is executed halfway.

5.3 Data Instructions

Data instructions such as addition, subtraction, comparison, BCD, BIN, and conversion are provided in addition to the sequence instructions which use relay and logic symbols.
The tada instruction consists of 3 steps and is expressed as shown below.



5.3.1 Instructions

- Data-Handling Instructions

Table 5.3.1

No.	Ins. code	Instruction	Symbol
1	MOV	Move Data S➡D	*1 MOV S D *2 *3
2	>	Comp. more than S > D	*4 > S D Y.M.T.C.F
3	<	Comp. less than S < D	*4 < S D Y.M.T.C.F
4	=	Equal S = D	*4 = S D Y.M.T.C.F
5	+	*5 Add S + U➡D	+ S D
6	−	*5 Sub. D − S➡D	− S D
7	BCD	BIN➡BCD conv. S➡BCD conv.➡D	BCD S D
8	BIN	BCD➡BIN conv. S➡BIN conv.➡D	BIN S D

** 1. This instruction is executed using input signal ON.*
2. S means source; data initiation.
3. D means destination; data results.
4. These are a contact instructions; other instructions are coil-contact instructions.
5. Cannot handle negative value.
6. All data instructions are 3-word instructions.

MOV

S \ D	K	D	T	C	X	Y	M
K		○					
D		○	○	○		○	○
T		○					
C		○					
X		○					
Y							
M		○					

MOV	Km	Dn	Store constant m in Dn: constant set.
MOV	Dm	Dn	Transmit Dm data to Dn: number shift.
MOV	Dm	T, Cn	Transmit Dm data to T, Cn: temporary value change of T or C.
MOV	Dm	KnY, M	Output Dm data to Y or M: n is decimal unit No. 1 ~ 4, 1 unit consists of 4 digits.
MOV	T,Cm	Dn	Transmit temporary value of T or Cm to Dn.
MOV	KmX,M	Dn	Transmit X or M of m decimals (1m unit = 4 digits) to Dn: input instruction.

>, <, =, +, −

S \ D	K	D	T	C	X	Y	M
K		○					
D		○					
T							
C							
X							
Y							
M							

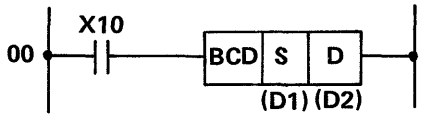
>	Km	Dn	Compare whether constant m > Dn data.
<	Km	Dn	Compare whether constant m K Dn data.
=	Dm	Dn	Compare whether data of Dm = data of Dn.
+	Km	Dn	Add constant m to Dn data, and store the result in Dn.
+	Dm	Dn	Add Dm data to Dn data, and store the result in Dn.
−	Km	Dn	Subtract constant m from Dn data, and store the result in Dn.
−	Dm	Dn	Subtract Dm data from Dn data, and store the result in Dn.

BCD(○)
BIN(●)

S \ D	K	D	T	C	X	Y	M
K							
D		●○					
T		○					
C		○					
X		●					
Y							
M							

BCD	Dm	Dn	Convert Dm data (BIN) to BCD, and store the result in Dn.
BCD	T,Cm	Dn	Convert T or C data to BCD, and store the result in Dn.
BIN	Dm	Dn	Convert Dm data (BCD) to BIN, and store the result in Dn.
BIN	KmX	Dn	Convert input of 4-decimal units (1 unit = 4 digits) to BIN, and store the result in Dn.

5.3.2 BCD convert instruction (BCD)



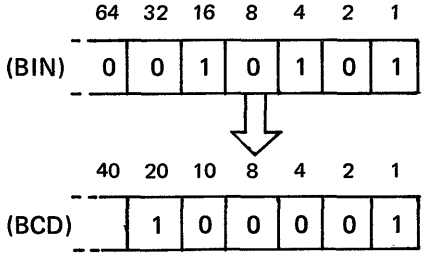
Coding

Step	Instruction
0000	LD X10
0001	BCD
0002	D1
0003	D2

BCD — BCD convert instruction (Binary coded decimal)

Instruction which is used to convert BIN (binary code) into BCD (binary coded decimal).

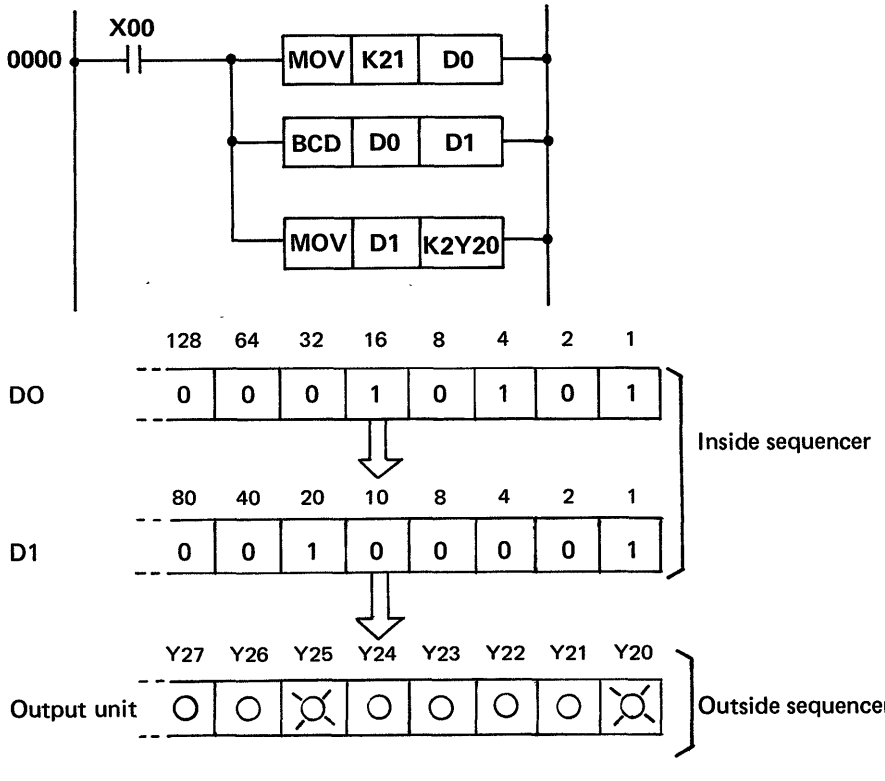
- Arithmetic operation principle



○ mark shows convertible combination.

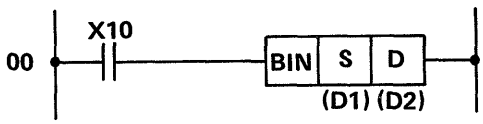
S \ D	K	D	T	C	X	Y	M
K							
D		○					
T		○					
C		○					
X							
Y							
M							

"21" is expressed in BIN and BCD as shown above. BCD instruction performs BIN to BCD conversion as shown by the arrow, and is utilized to output the content of register to the exterior, as a decimal number, through output unit.



Step	Instruction
0000	LD X00
0001	MOV
0002	K21
0003	D0
0004	BCD
0005	D0
0006	D1
0007	MOV
0008	D1
0009	K2Y20

5.3.3 BIN covert instruction (BIN)



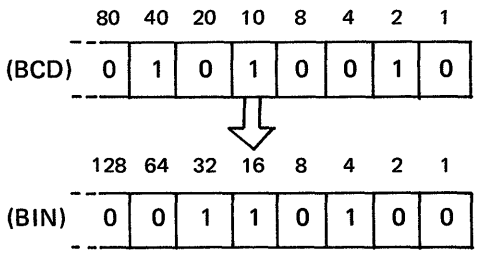
Coding

Step	Instruction
0000	LD X10
0001	BIN
0002	D1
0003	D2

BIN Binary convert instruction

Since input data generally has many decimal numbers, this BIN instruction is provided. The input data of BCD is converted and input, and then internally processed in binary code.

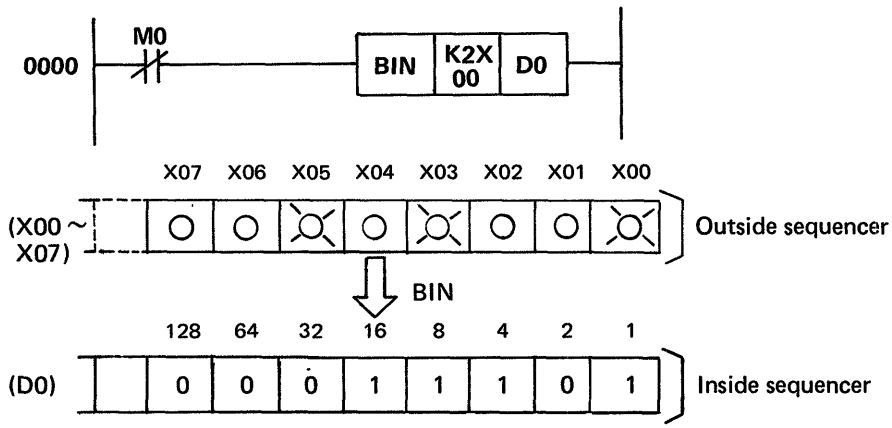
- Arithmetic operation principle



○ mark shows convertible combination.

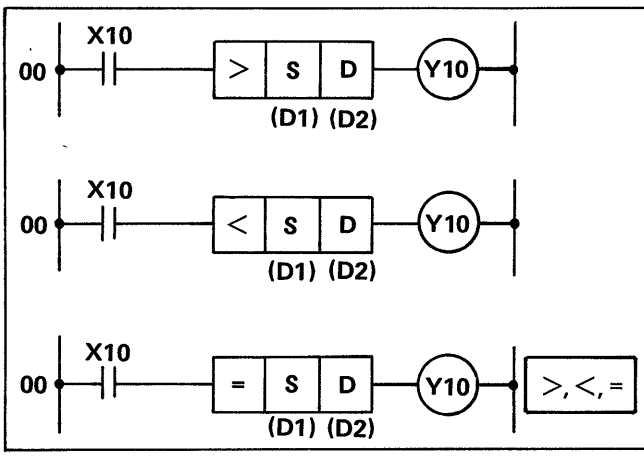
S \ D	K	D	T	C	X	Y	M
K							
D		○					
T							
C							
X		○					
Y							
M							

"52" is expressed in BCD or BIN as shown above. BIN instruction performs BCD to BIN conversion as indicated by the arrow and is utilized, for example, to read BCD data of digital switch, N/C, computer, etc. into the sequencer.



Step	Instruction
0000	LDI M0
0001	BIN
0002	K2X00
0003	D0

5.3.4 Data compare instruction (>, =, <)



Coding

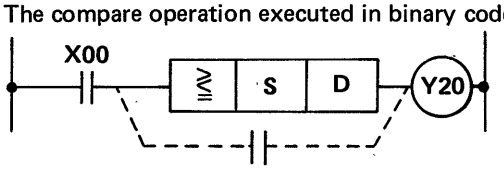
Step	Instruction
0000	LD X10
0001	> (<) (=)
0002	D1
0003	D2
0004	OUT Y10

Data compare instruction

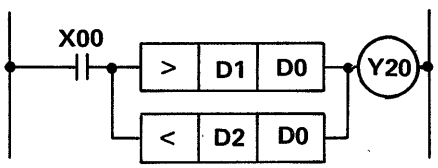
○mark shows operable S/D combination.

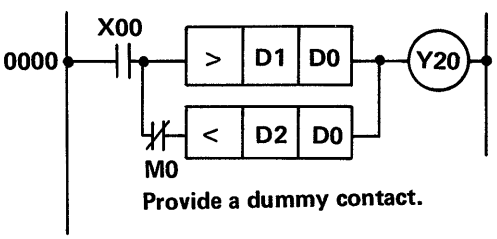
S \ D	K	D	T	C	X	Y	M
K		○					
D		○					
T							
C							
X							
Y							
M							

The compare operation executed in binary code.



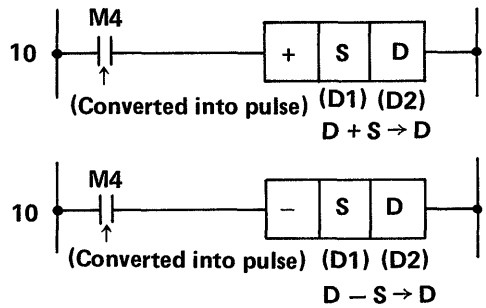
The compare instruction is equivalent to contact in handling. However, since OR instruction cannot be performed, do as shown below.





Step	Instruction
0000	LD X00
0001	>
0002	D1
0003	D0
0004	LDI M0
0005	<
0006	D2
0007	D0
0008	ORB
0009	OUT Y20

5.3.5 Add instruction (+), subtract instruction (–)



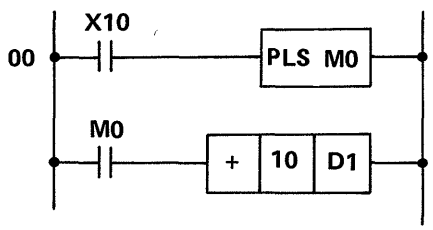
+ Add instruction

– Subtract instruction

Coding

Step	Instruction
0010	LD M4
0011	+ (–)
0012	D1
0013	D2

*Be sure to use pulse instruction and also use M, which has been converted into pulse signal, prior to this add or subtract instruction.

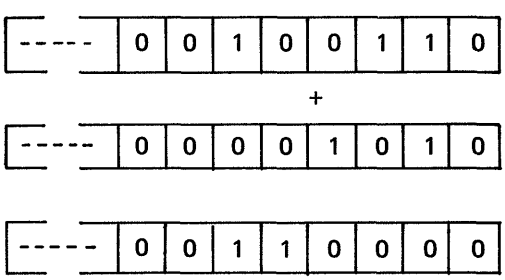


When M0 turns on, D1 is added to 10 and the value is entered into D1.

Step	Instruction
0000	LD X10
0001	PLS M0
0002	LD M0
0003	+
0004	10
0005	D1

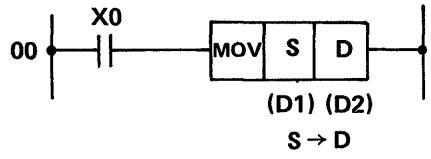
○ mark shows operable combination.

S \ D	K	D	T	C	X	Y	M
K		○					
D		○					
T							
C							
X							
Y							
M							



* Take care of subtract instruction because it is reverse in position to a normal arithmetic equation, i.e. the subtracted value is located in D and the subtracting value in S.
Also take care not to make the result of arithmetic operation negative because only positive integers are handled. When there is a possibility that arithmetic result may become negative, compare whether S or D is larger. When S is larger than D, subtract D from S and store into M the fact that the result is negative.

5.3.6 Move instruction (MOV)



MOV Transmit instruction

Coding

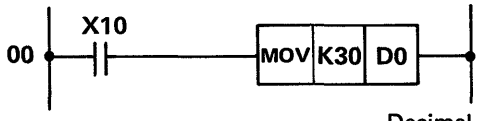
Step	Instruction
0000	LD X0
0001	MOV
0002	D1
0003	D2

- After arithmetic operation, S and D contents are the same.
- After execution of instruction, S content does not change.
- K, D, T, and C are transmitted in 16 bits.

○ mark shows operable S/D combination.

S \ D	K	D	T	C	X	Y	M
K		○					
D		○	○	○		○	○
T		○					
C		○					
X		○					
Y							
M		○					

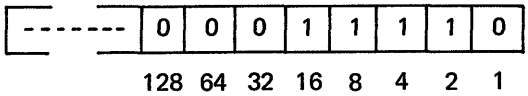
- Constant set



Step	Instruction
0000	LD X10
0001	MOV
0002	K30
0003	D0

Decimal "30" is converted into binary code, and is entered into D0.

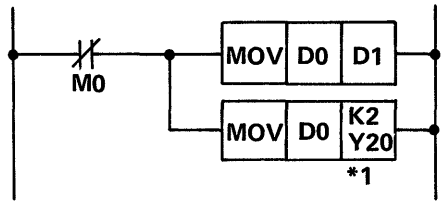
* The constants handled by PU or GPP become binary numbers inside the sequencer.



Content of D0
(Data registration consists of 16 bits)

- Data transfer

16 + 8 + 4 + 2 = 30



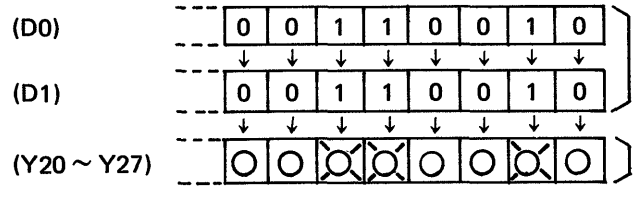
*1, Km Y20 specifying method

4 bit x m (1 ~ 4) Leading bit = Y20 ~ Y27

(Exampla)

K4 x X00 = 4 bits x 4 X00 (leading bit)

= X00 ~ X0F



5.4 Application Instructions

5.4.1 Application Instruction

No.	Name of function	Function No.	Instruction	Data register used and purposes					
				D110	*	D111	*	D112	*
1	8-Bit data association	F110	OUT F110	Lower 8-bit D No. Associated D No.	I	Upper 8-bit D No.	I		
2	16-bit data dissociation	F111	OUT F111	D No. before dissociation Lower 8-bit D No.	I	Upper 8-bit D No.	I		
3	16-bit dataAND	F112	OUT F112	D No. Operated result D No.	I	D No.			
4	16-bit data OR	F113	OUT F113	D No. Operated result D No.	I	D No.			
5	Batch shift of M	F114	OUT F114	Head No. of M	I	Number of bits	I	Shift direction	I
6	Batch shift of D	F115	OUT F115	Head No. of D	I	Number of registers	I	Shift direction	I
7	Batch reset of D	F116	OUT F116	Head No. of D	I	Number of registers	I		
8	Indirect reading of T,C,D	F117	OUT F117	T, C, D No.	I	Contents read	O		
9	Indirect writing of T, C, D	F118	OUT F118	T, C, D No.	I	Data written	I		
10	Y → D Data transfer	F119	OUT F119	Y No. and number of digits	I	D No. transferred	I		
11	4 ↔ 16 Decode/encode	F108	OUT F108	Data	I	Decode or encode	I	Result of decode/ encode	O
12	16-bit check	F109	OUT F109	Check data	I	Cumulated bits	O		
13	Data inversion	F100	OUT F100	D No.	I				
14	High-speed processing program call instruction	F126	SET F126	D123		D126			
	High-speed processing program return instruction		RST F126	High-speed program head step No.	I	High-speed program head step No.			

* { "I" shows the data to be prepared before execution of application instruction.
"O" shows the resultant data after execution of application instruction.

Note: D No. shown in the above list is data register No. (0 ~ 95) for operand. Arithmetic operation is actually performed with the specified data register.

5.4.2 Functions and practical use of application instructions

8-bit data association

When AND or OR operation is performed with 16-bit data in the standard K series CPU, only plus integer ranging from 0 to 9999 can be specified. When the additional function is used, however, 16-bit data can be formed as follows:

5.4.2.1 Functions

Function No. F110

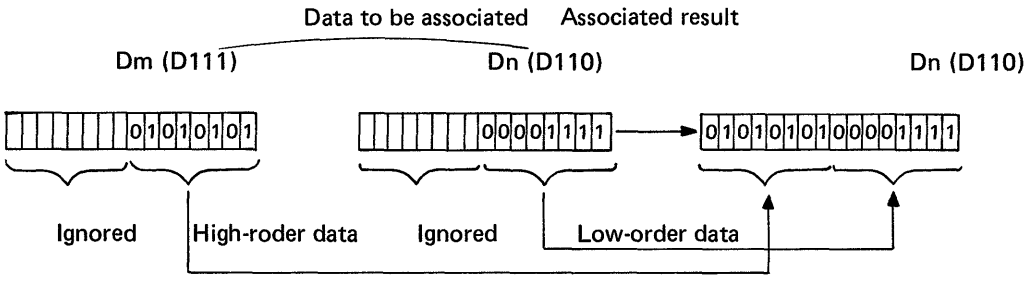
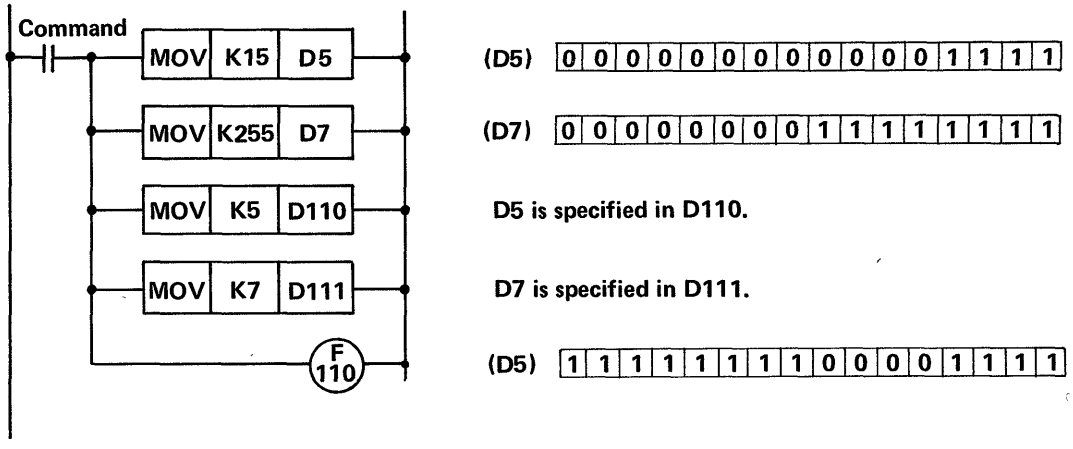


Fig. 5.4.2.1 Data association

Note: D (D110) indicates the contents of the data register specified by D110.

(1) When D No. storing lower (low-order) 8-bit data to be added with counterpart and other D No. storing higher 8-bit data are set in D110 and D111 respectively, and F111 is executed, the resultant 16-bit data is placed in Dn (D110).
(2) The content in Dm (D111) do not change. The resultant data is placed in Dn.
(3) The data to which another data is associated, may be either BCD 2-digit data, or binary 8-bit data.
(4) When the newly formed binary 16-bit data is larger than 9999 and BCD instruction is executed, "RUN" display flickers. No substantial problem is caused by data exceeding 9999 as far as BCD instruction is not executed. However, monitor data by PU or GPP cannot be normally displayed.

(Circuit application)



5.4.3 16-bit data dissociation

The result from AND or Or with 16-bit data is divided into one pair of 8-bit data when this function is used.

5.4.3.1 Functions

Function No.: F111

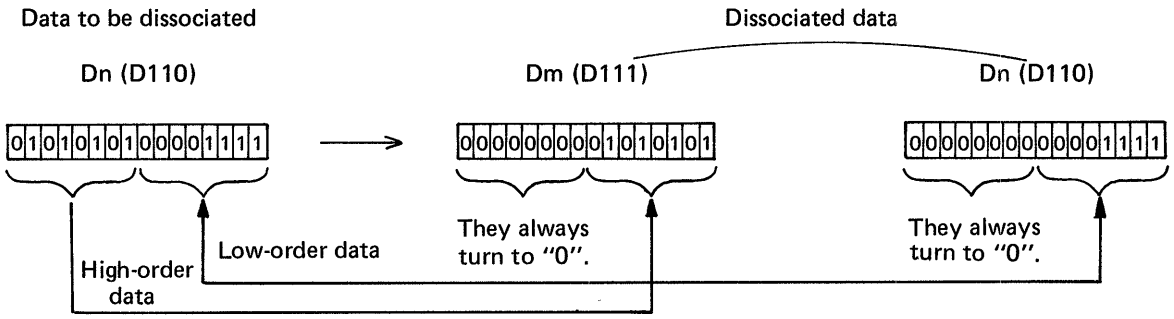


Fig. 5.4.3.1 Data dissociation

(1) When D No. (Dn) storing 16-bit data to be dissociated is entered in D110 and D No. in which upper 8-bit data is placed after the dissociation is entered in D111, and F111 is executed, the dissociated two data are placed in Dm (D111) and Dn (D110).
(2) The data to be dissociated may be binary 16-bit data or BCD 4-digit data.

5.4.3.2 Circuit applications

Ex.: Content (BCD 4-digit data) of D5 are divided into two-digit BCD data, and placed in D5 and D20 separately.

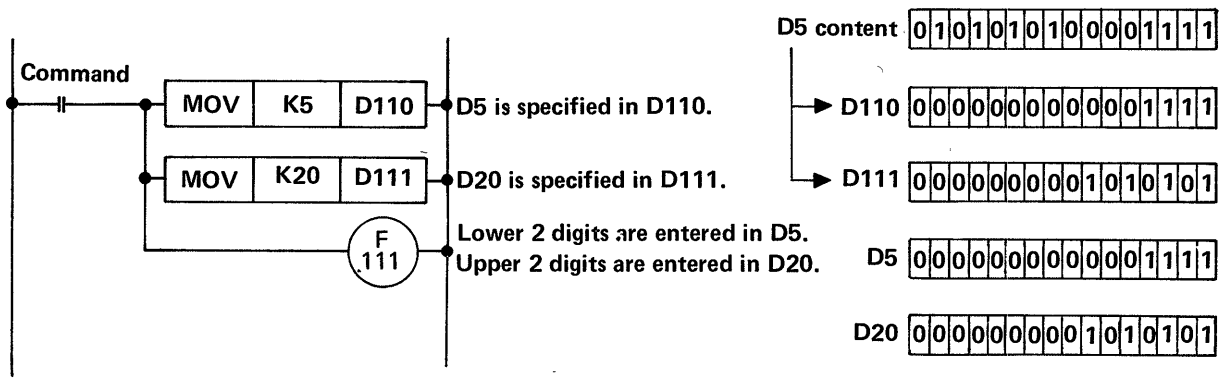


Fig. 5.4.3.2 Data Dissociation Circuit

5.4.4 16-bit data AND operation

Each bit-to-bit AND operation is performed between two data registers.

5.4.4.1 Functions

Function No.: F112

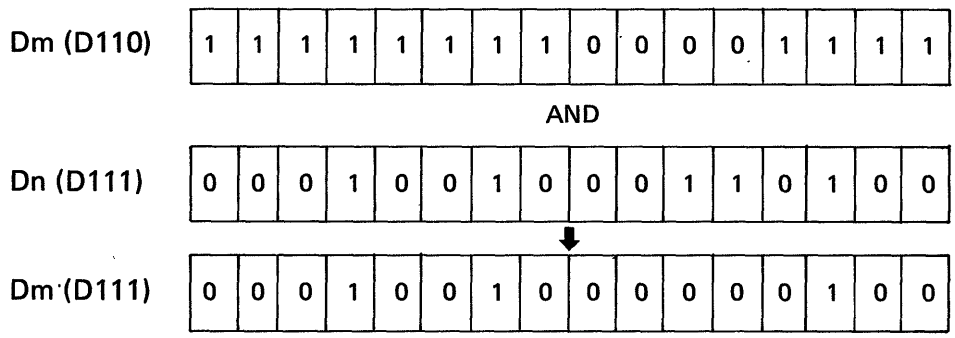


Fig. 5.4.4.1 16-bit data AND operation

5.4.4.2 Circuit applications

Ex.: The third digit of BCD 4-digit data of D10 should be masked with "0".
When D10 is "1 2 3 4", for example,

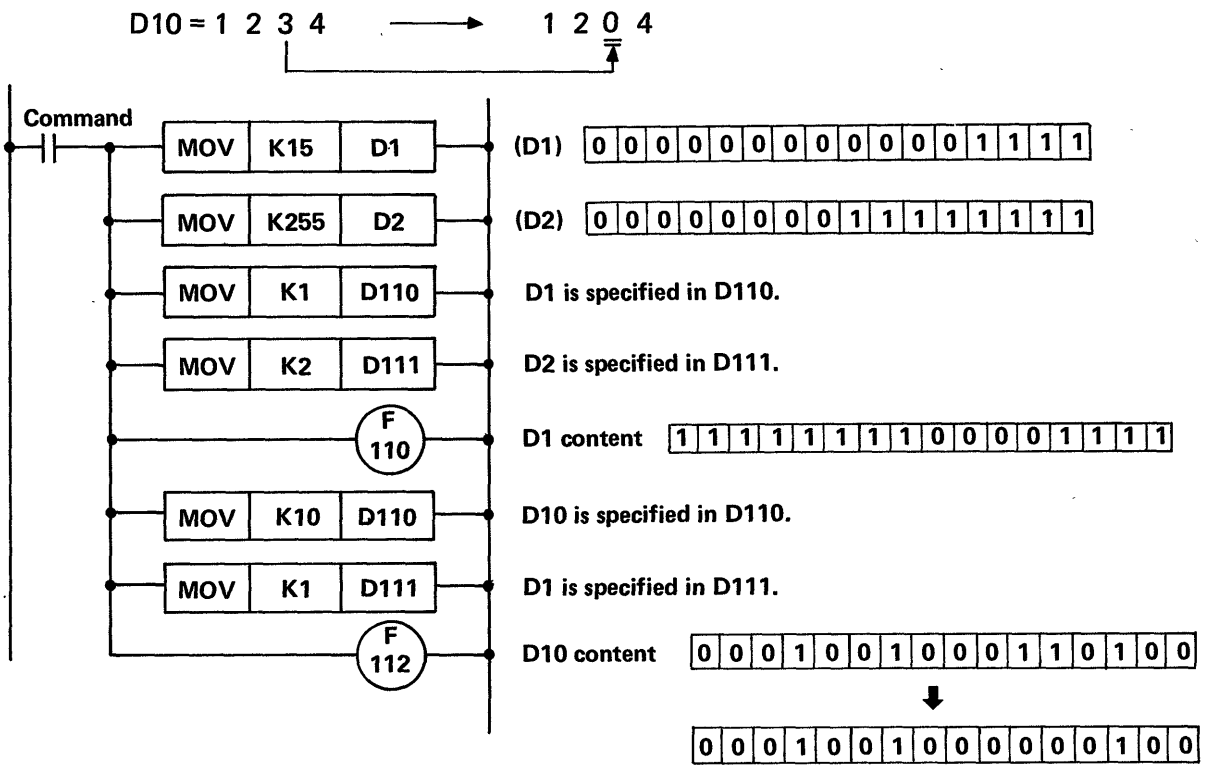


Fig. 5.4.4.2 AND Operation Circuit

5.4.5 16-bit data OR operation

Each bit-to-bit OR operation is performed between two data registers as follows:

5.4.5.1 Functions

Function No.: F113

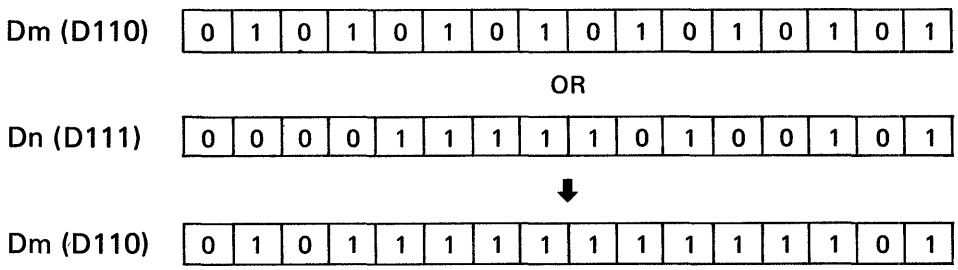


Fig. 5.4.5.1 16-bit data OR operation

5.4.5.2 Circuit applications

Ex.: OR operation is performed between D10 and D20 and the result is placed in D10.

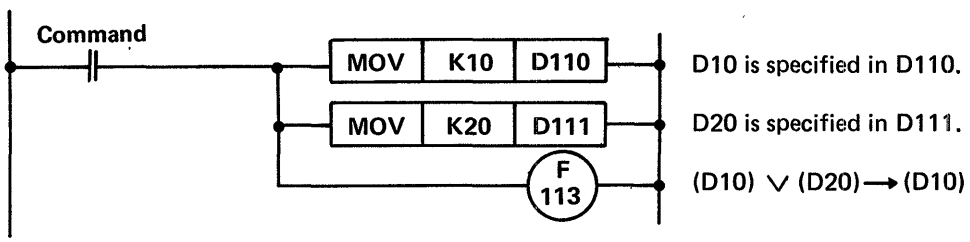


Fig. 5.4.5.2 16-bit data OR operation circuit

5.4.6 Batch shift of temporary memory M

Temporary memory M shift (SFT) instruction available in the standard CPU is of one bit shift instruction, and several steps are required for shift instruction with plural bits.
When the function F114 is used, contents of desired number of bits may be batch shifted leftward or rightward from the specified head No. of M.

5.4.6.1 Functions

Function No.: F114

Head No. of M:	D110	0060	Binary numerals
Number of bits to be shifted:	D111	0030	Binary numerals
Shift direction (leftward/rightward)	D112	0000 (Leftward shift)	0001 (Right ward shift)

Note:
M may be specified between the range from M0 to M249. If number of bits specified in D111 exceeds this range, shift is not executed.

5

(1) The head No. of shift register to be formed is placed in D110. The No. should be junior one no matter whether shift is leftward or rightward, and written with binary numerals* in D110.
(2) The length of shift register, that is, number of bits to be shifted, is written in D111 with binary numerals*.
* Writing with binary numerals
When decimal numeral "n" is written on PU or GPP in the form of MOV Kn D110,D111, it is automatically converted into binary numerals. However, binary numeral should be used as converting from decimal numeral when head No. and number of bits are specified in BCD code.
(3) Direction of shift should be specified in D112. When the contents in D112 are "0", the shift is leftward from junior No. to senior No. The shift, however, is rightward from senior No. to junior No. when the contents are "1".
(4) Circuit composition.

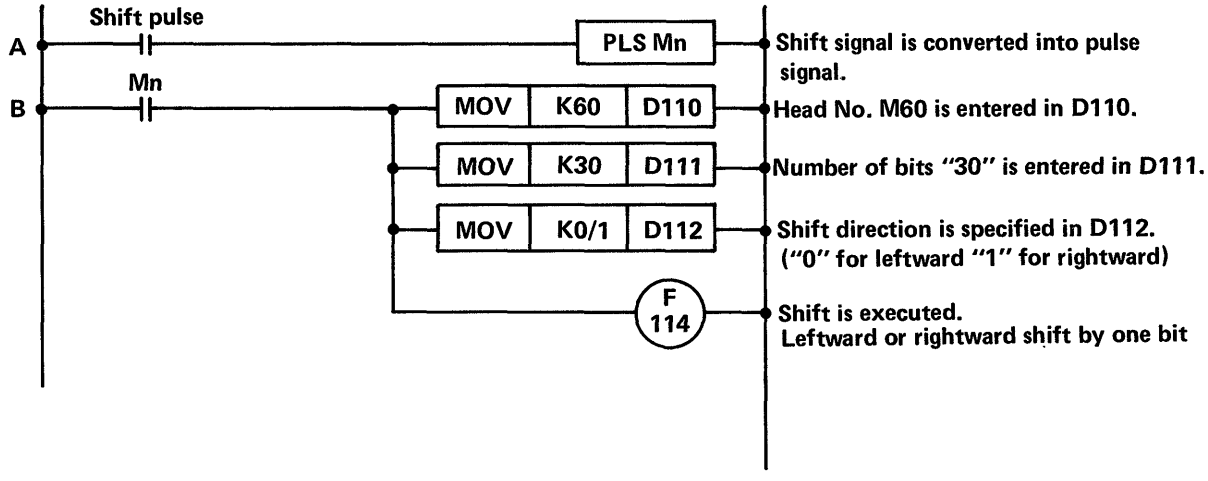


Fig. 5.4.6.1 Shift Register Circuit Composition

1) Shift command should be converted into pulses, otherwise "racing" (shift goes on without interruption although only one pulse is given) might occur.
2) When only one shift register is available in a program, it is recommended to enter the data (head No., number of bits, etc.) at start of execution, thereby "B" block may be simplified with only Mn and F114.
3) Actual shift register requires, in addition to the circuit shown in Fig. 5.4.6.1, reset circuit and data set circuit. For details, refer to para 5.4.6.2.
4) One-bit shift occurs each time when Mn turns on.

(5) The status of the shift register exemplified in Fig. 5.4.6.1 is as follows:

1) Leftward shift

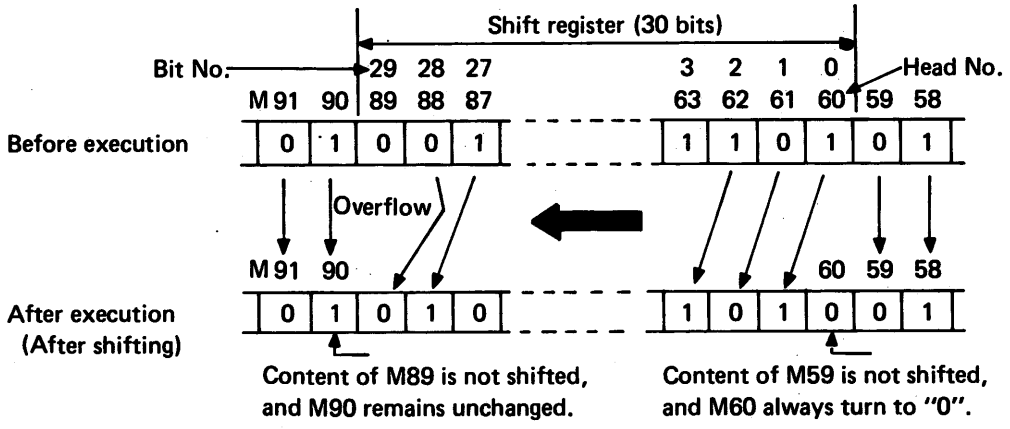


Fig. 5.4.6.2 Left ward Shift

2) Rightward shift

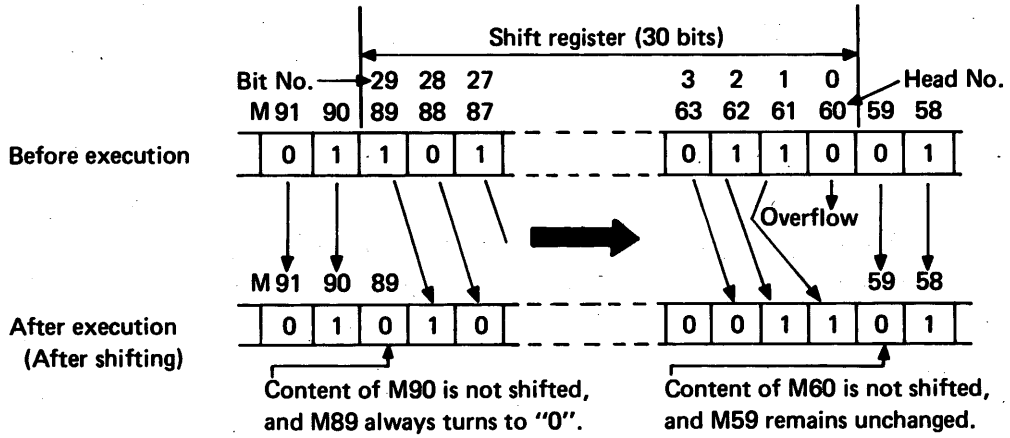


Fig. 5.4.6.3 Rightward Shift

a) In leftward as well as rightward shift, the first bit (M60 for leftward shift, and M89 for rightward (shift) is not affected by shifting, and replaced with "0" at all times. If any shift data must be entered, it should be placed after the shifting.
b) The contents at the final bit of the shift register (M89 for leftward shift, and M60 for rightward shift) is erased due to overflow.

(6) Any bit "Mn" in the shift register may be set or reset with set (SET) instruction or reset (RST) instruction.

5.4.6.2 Circuit applications

(1) Leftward shift register

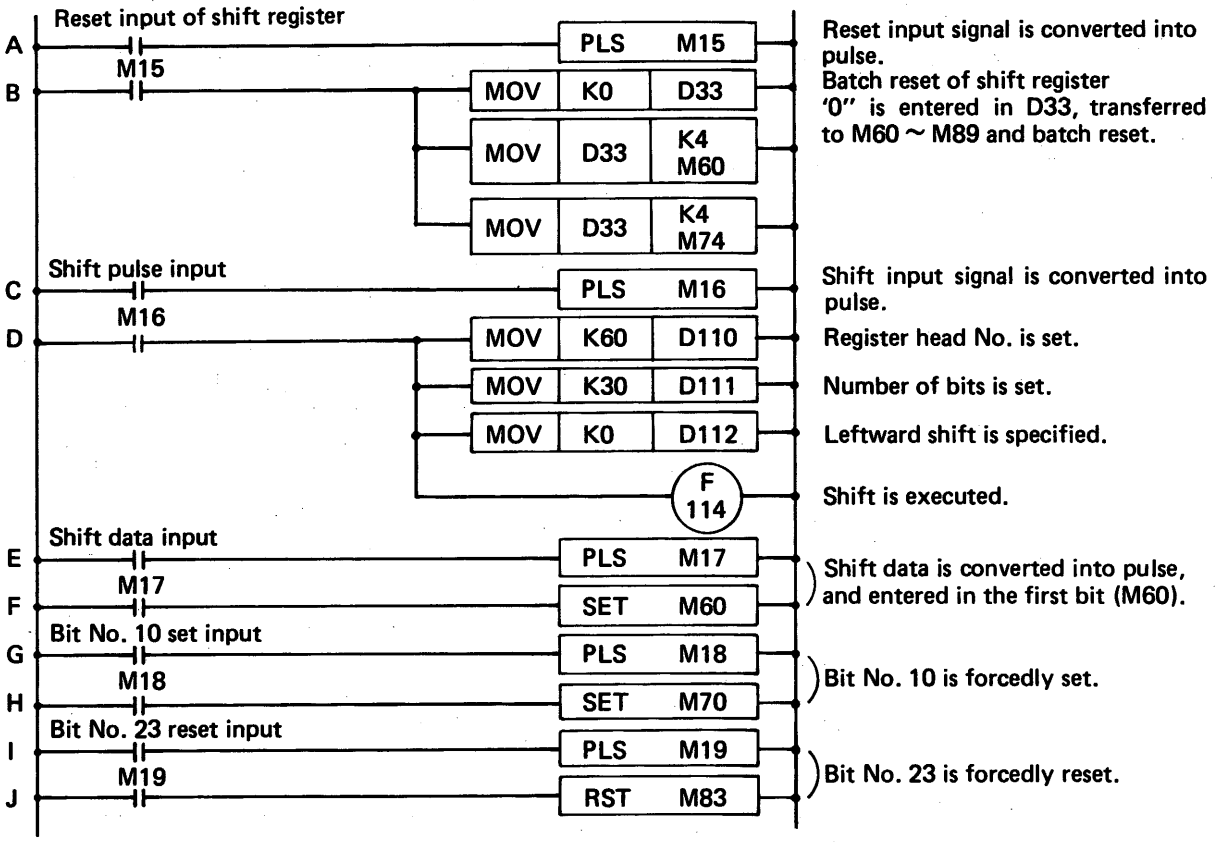


Fig. 5.4.6.4 Leftward Shift Register Circuit

(1) Contents shift from junior M No. to senior M No.
(2) "B" circuit block is for multi-bit batch reset that is accomplished as follows:

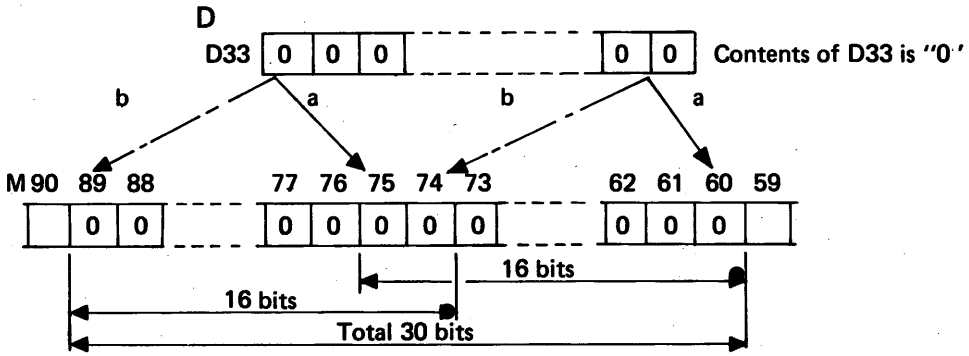


Fig. 5.4.6.5 Batch Reset of M

In "a", "0" is transferred to M60 ~ 75 with [MOV | D33 | K4M60] . "0" is transferred to M74 ~ M89 with [MOV | D33 | K4M74] in the case of "b".
Total 30 bits may be reset at the same time.
Although no function or instruction is available for batch reset, batch reset can be programmed as shown in Fig. 5.4.6.5.

(3) The "E" and "F" circuit blocks are for setting of shift data to the fead bit. The setting is accomplished without synchronization with shift pulse, and immediately realized when data is given.

(4) Any bit in the shift register may be forcedly set or reset with input signal, as the case may be with "G", "H", "I" and "J" circuit blocks.

(5) It is recommended for prevention of overlap of timing to convert each input signal into pulses, like in "A", "C", "E", "G" or "I" circuit block.

(6) Timing chart of circuit operation

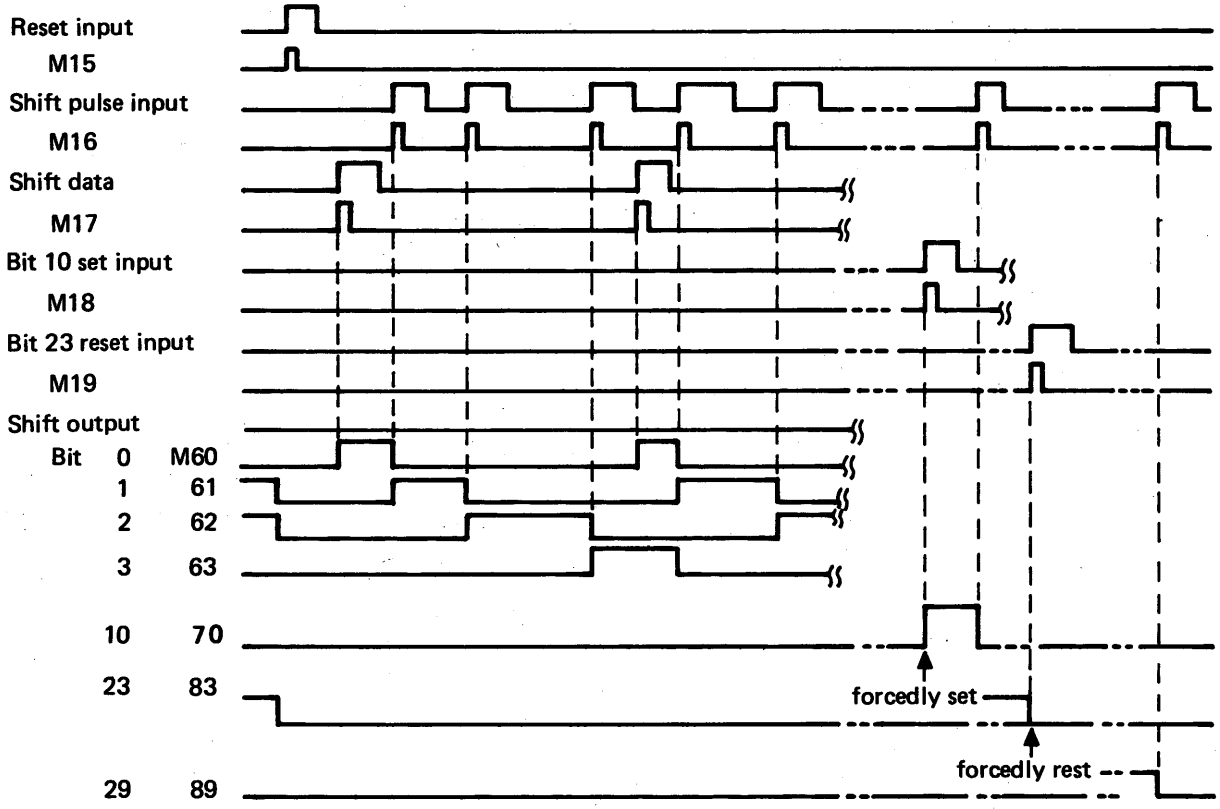


Fig. 5.4.6.6 Left ward Shift Register Timing Chart

(2) Rightward shift register

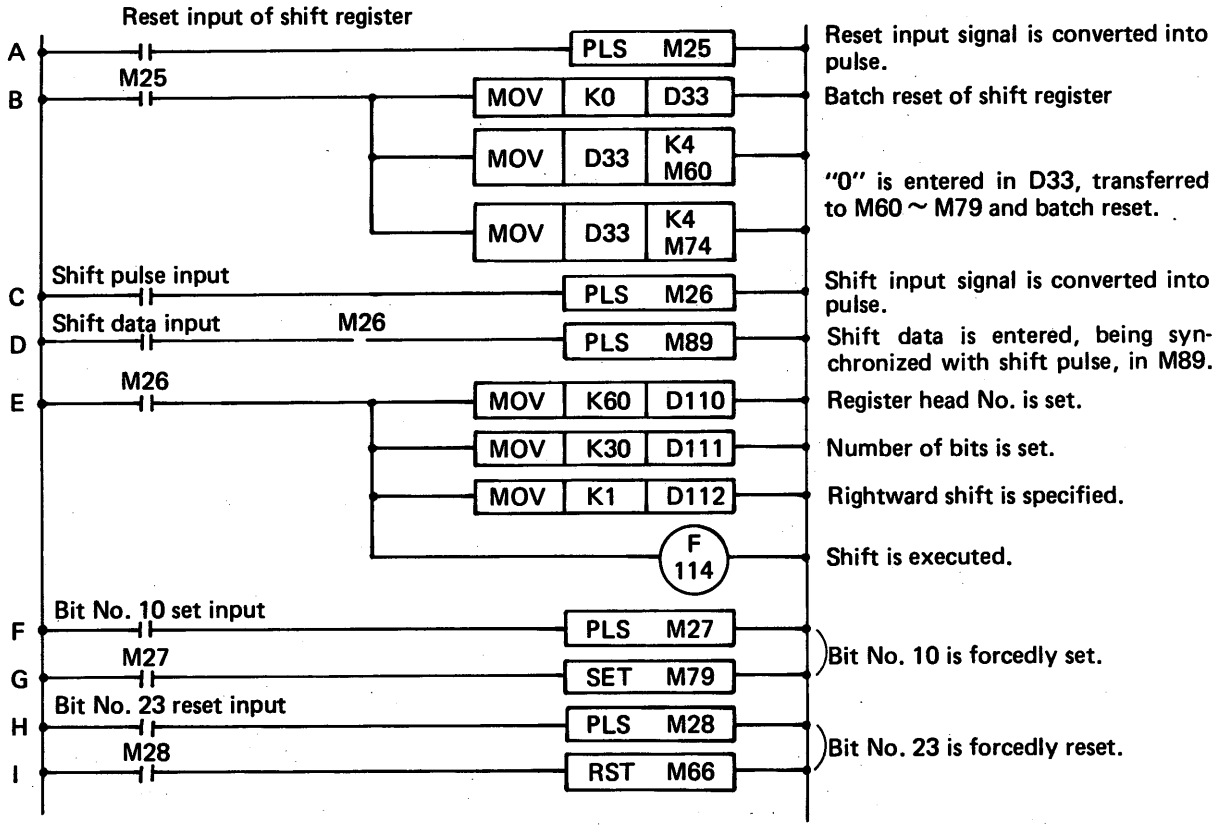


Fig. 5.4.6.7 Rightward Shift Register Circuit

(1) Circuit block "D" reads shift data, being synchronized with shift pulses, and sets the head No. of the rightward shift register "M89".
(2) Other functions and operations are the same as those of the leftward shift register.

(3) Timing chart of circuit operation

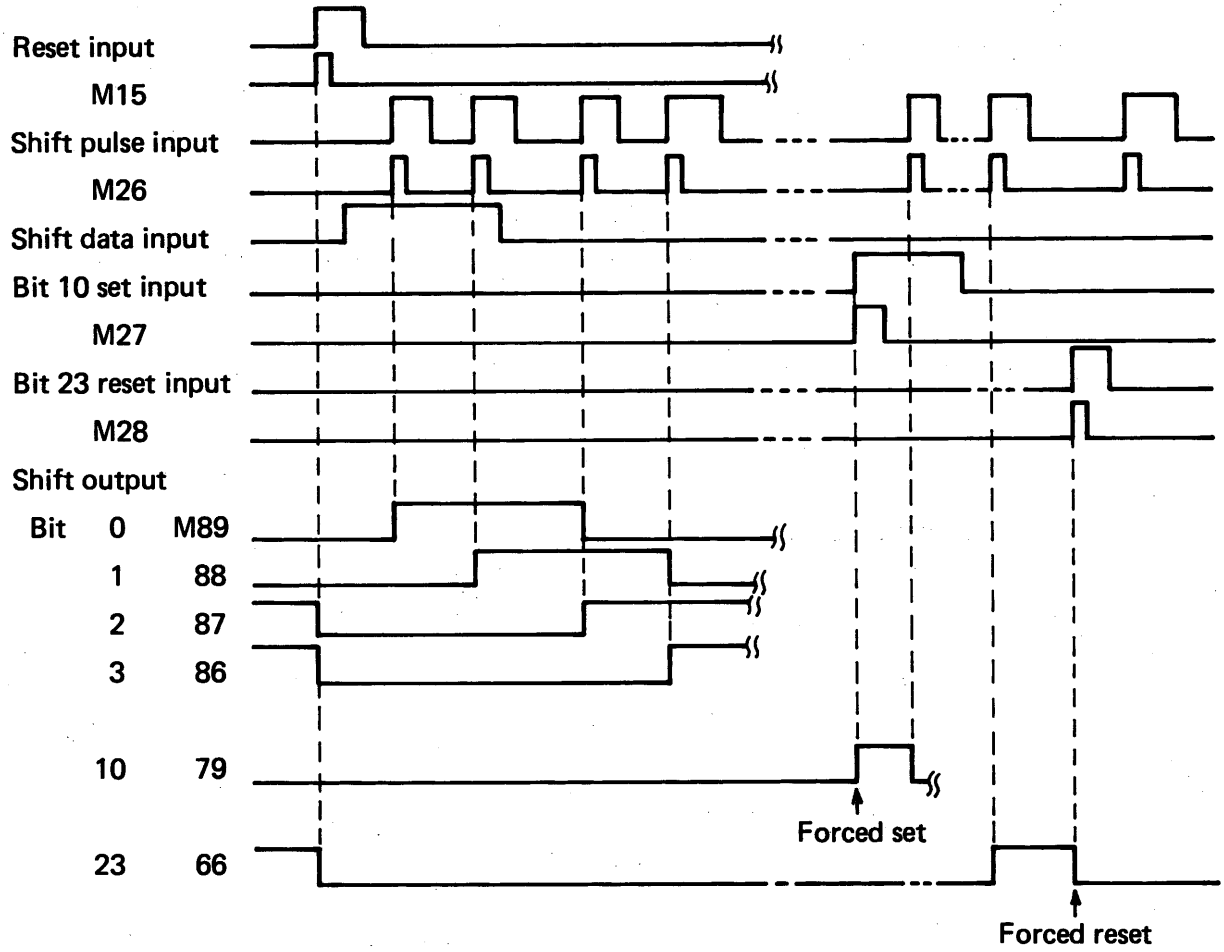


Fig. 5.4.6.8 Rightward Shift Register Timing Chart

5.4.7 Batch shift of data register D

In order to shift contents in data register of the standard CPU, MOV instruction must be repeated the same time as the number of data to be shifted and therefore a considerable number of steps must be programmed for a large number of data.
When the additional function is used, the data shift may be accomplished only by specifying head No. of data register, length of data (number of bits), and direction of shifting, thus facilitating programming with a short number of steps.

5.4.7.1 Functions

Function No.: F115

Head No. of register D:	D110	0057	Binary numerals
Number of data registers to be shifted:	D111	0016	Binary numerals
Direction of shift: (leftward/rightward)	D112	0000 Leftward	0001 Rightward

Note: Applicable number of register range is from D0 to D95. If number of registers specified by D111 exceeds D95, batch shift becomes impossible.

(1) Shift status

① Leftward shift

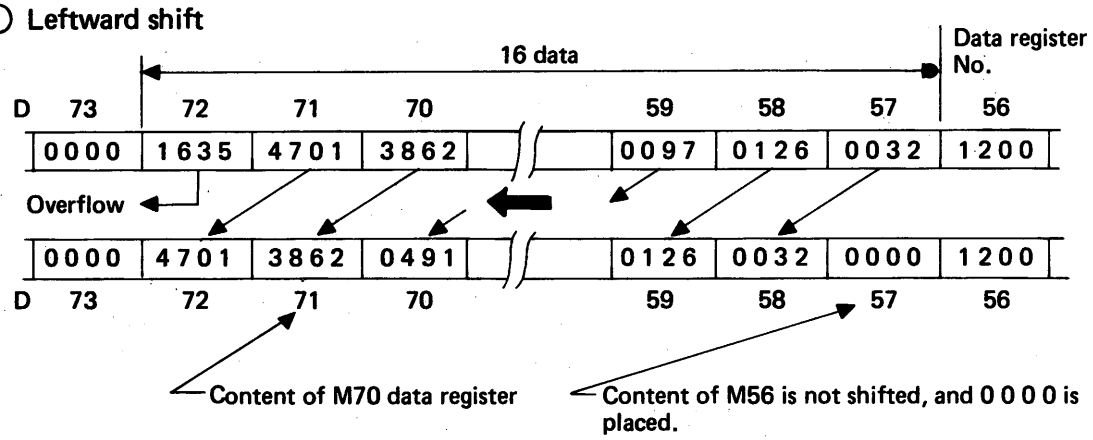


Fig. 5.4.7.1 Batch Shift (Leftward shift)

② Rightward shift

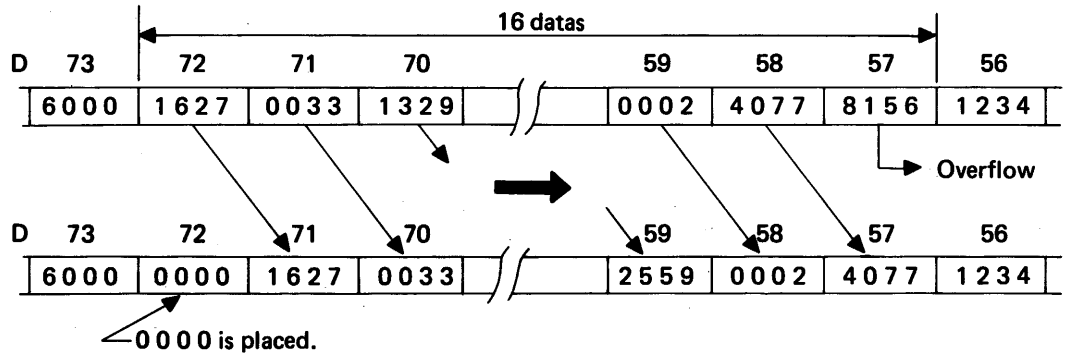


Fig. 5.4.7.2 Batch Shift (Rightward shift)

(2) The head No. of data register (junior No.) to be shifted should be specified in D110. The head No. should be one with junior No., no matter whether data shift is leftward or rightward, and be "D57" in Fig. 5.4.7.1 and Fig. 5.4.7.2.

(3) Length of data (words) to be shifted should be specified in D111. When 16 datas are desired to be shifted, for example, "16" is entered in D111. Care should be taken not to enter data over the range at D95 (leftsward shift) or D0 (rightward shift).

(4) Direction of shift is specified in D112.

Leftward	0 0 0 0	Junior No.	➡ Senior No.
Rightward	0 0 0 1	Senior No.	➡ Junior No.

(5) With a shift signal, leftward or rightward batch shift (a group of data is shifted at the same time) occurs once.

(6) Circuit composition.

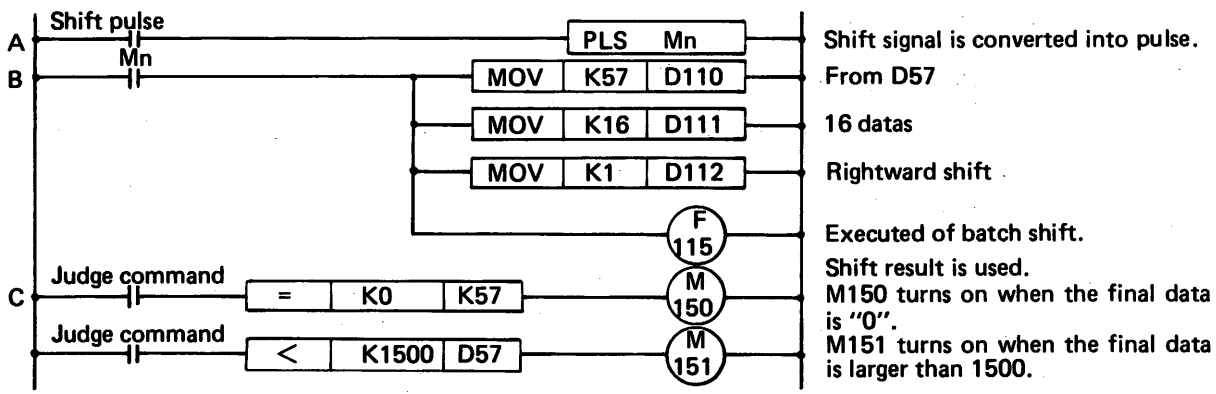


Fig. 5.4.7.3 Batch Shift Circuit Composition

① In order to prevent racing, be sure to convert shift signal into pulse .
② Circuit block "B" may be simplified to only Mn and F114 when one program has only one batch shift) in F115 and three MOV instructions in that block are given at initial time.
③ A separate circuit is required to enter data in the register with shift top (D72 in this example).
④ Each time shift signal Mn turns on, batch data shift occurs once.
⑤ As the result of data shift, the content of the final data register (D57 for rightward shift in Fig. 5.4.7.2, and D72 for leftward shift in Fig. 5.4.7.1) are judged as in circuit block "C" and the judged result (M150, 151) may be used in a sequential control system.

(7) The shift head register content becomes "0", as shown in Fig. 5.4.7.1 and 5.4.7.2 when F115 is executed.
Therefore, the data set mentioned in ③ should be performed at a step coming after the execution of F115.
(8) The last register content is erased after the execution of F115, due to overflow.
(9) Contents in the data registers out of shifting range are not affected by batch shifting.

5.4.8 Batch reset of data register D

All consecutive data register contents are cleared to "0".

5.4.8.1 Functions

Function No.: F116

Head No. of register D. D110 [0045] Binary numerals

Number of data registers to be reset: D111 [0020] Binary numerals

Note: Number of data registers ranges from D0 to D95. Batch reset becomes impossible when the number of data registers is out of this range.

(1) The head No. of data registers to be reset is specified in D110.
(2) Number (length) of data to be reset is specified in D111.
(3) When F116 is executed under the above-mentioned conditions (1) and (2), all the contents in the data registers up to 20wds. from D45 (D45 ~ D64) are cleared to "0".

5.4.8.2 Circuit applications

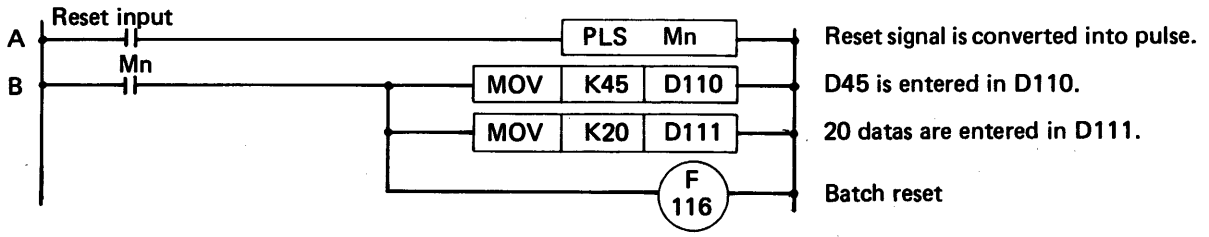


Fig. 5.4.8.2 Data Register Batch Reset Circuit

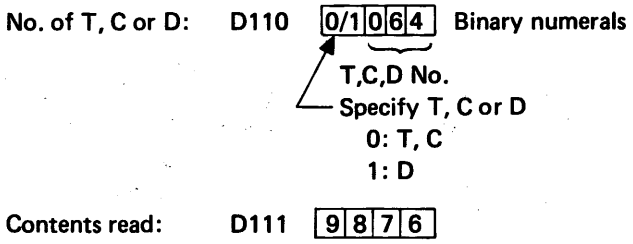
(1) Reset input signal should be converted into pulse signal at all times.
(2) The register D not backed up (latched) for power failure is automatically reset when the programmable controller is turned on or CPU "RESET" switch is operated.
(3) The functions may be used to reset the register D backed up for power failure.

5.4.9 Indirect reading of T,C,D (Timer, Counter, Register D)

When temporary values of timer (T) or counter (C), or contents of register (D) are read in the standard CPU, each one circuit must be programmed for each No. to be read.
On the contrary, desired current values or contents can be readily read with this additional function, only by specifying No. of T, C or D and executing this function (F117).
Therefore, the use of F117 is very advantageous when externally display or determination is desired for reading of current values or contents of T, C or D because the circuit may be simplified.

5.4.9.1 Functions

Function No.: F117



Note: T or C No. should be within a range from 0 to 127, and D within a range from 0 to 95. F117 may not be realized when No. out of this range is specified.

(1) Desired No. of T, C or D is binary specified in D110. When timer or counter temporary value is read, the 4th digit is filled with "0" (decimal numeral).
The 4 th digit is filled with "1" when register contnts is read.
Ex.: 0 0 6 4 T64 or C64
1 0 6 4 D64

(2) When F117 12 executed, the temporary value or content of specified No. is read out in D111. It should be noted that timer/counter is of binary, or BCD or bit pattern.

5.4.10 Indirect writing of T, C, D

With this fuction, temporary values of timer (T), counter (C) or register (D) contents are written with the No. of timer of register specified.
The indirect writing is mainly used to change content of register D, and utilizing this, it may be usable to change set values of T, C.
Although temporary values of timer (T) or counter (C) may be changed be using this function, it is recommended to change the temporary values by usual program edition.
It should be noted that T, C set value with Kn has been written at programming steps and therefore may not be changed with this function.
To change T, C set value, Dn should be specified for set value and the content of Dn should be changed with this function.

5.4.10.1 Functions

Function No.: F118

Function No.: D110 [0/1][0][9][3] Binary numerals

T,C,D No.
Specify T, C or D
0: T or C
1: D

Data to be written: D111 [5][4][3][2] Binary numerals

Note: T, C No. should be specified within a range from 0 to 127 and D No. should be specified within a range from 0 to 95. If specified No. is out of the range, F118 cannot be executed.

(1) T, C or D No. is entered in D110 with binary numerals. Numerals ranging from 0 to 127 may be used for T, C No. and numerals added with "1000", ranging from 1000 to 1095, may be used for D No.
(2) Data is written in D111 with binary numerals.
(3) The data entered in D111 is written to the T, C or D No. specified in D110 when F118 is executed.

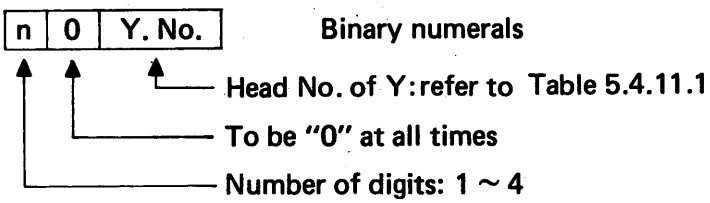
5.4.11 Data transference from Y to D

Although the standard CPU permits data transference from D to Y, reverse data transference from Y to D is impossible. 16-bit ON-OFF (L-H) status of Y, grouped for each four bits, can be transferred to the specified D when this function is executed.
The function may be used to check bit pattern (ON-OFF status) output from Y against the standard bit pattern, or to latch bit pattern in D in case of power failure.

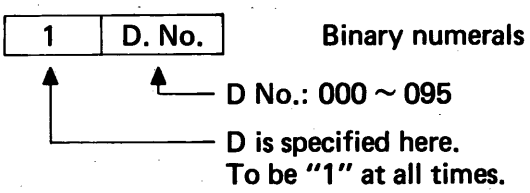
5.4.11.1 Functions

Function No.: F119

Y No. and digits: D110



D No. to be transferred: D111



(1) D110 can be set up to as follows:

① n : Number of 4-bit groups 1 ~ 4

Number of bit groups	Total number of bits
1	4
2	8
3	12
4	16

Note: D should be within a range from 0 to 95. If D is out of this range, F119 cannot be executed.

② 0 : To be "0" at all times.

③ Y. No.: Head No. of Y refer to Table 5.4.11

a) Y No. should be the head No. of 16-bit group, and expressed in decimal notation, as shown in Table 5.4.11.1.

Table 5.4.11.1 Y No. and Applicable Code

Y No.	Code
020	02
030	03
080	08
090	09
0A0	10
0B0	11
0C0	12
0D0	13
0E0	14
0F0	15

b) The head No. of Y is the head No. of 16-bit group. Therefore, transference of partial bits, such as 4-bits from "028", is impossible.

c) Example of setting of D110.

Con

Content of D110	Area of which data can be transferred	Bits
1011	Y0B0 ~ 0B3	4
4014	YE0 ~ YEY	16

(2) D111 is used to specify No. of D to which contents of Y (4 bits ~ 16 bits) are transferred, and filled with D No. plus "1000".

Ex.: D 0 1000
D39 1039
D74 1074

(3) Even when transferred data contents are of 4 ~ 12 bits, one register D should be used.

5.4.11.2 Circuit applications

As an example of the function F119, a circuit that permits checking of bit pattern with 12 bits starting from Y20 against the standard bit pattern is described here. The description also includes checking of 8-bit pattern from Y30, and how to form the standard bit pattern. Number of bits and destination of transference are also exemplified in this paragraph.

(1) When 12-bit contents starting from Y20 are transferred to D8 . . . . .

Y2B	2A	29	28	27	26	25	24	23	22	21	20
0	1	0	1	1	0	0	0	1	0	1	1
2048	1024	512	256	128	64	32	16	8	4	2	1

1024 + 256 + 128 + 8 + 2 + 1 = 1419

(2) When 8-bit contents from Y30 are transferred to D24 . . . . . .

Y37	36	35	34	33	32	31	30
1	0	1	1	1	0	1	0
128	64	32	16	8	4	2	1

128 + 32 + 16 + 8 + 2 = 186

When K1419 for Y20, or K186 for Y30, is entered to the specified D by using MOV instruction, the bit pattern in the D becomes as shown above and the standard pattern can be obtained.

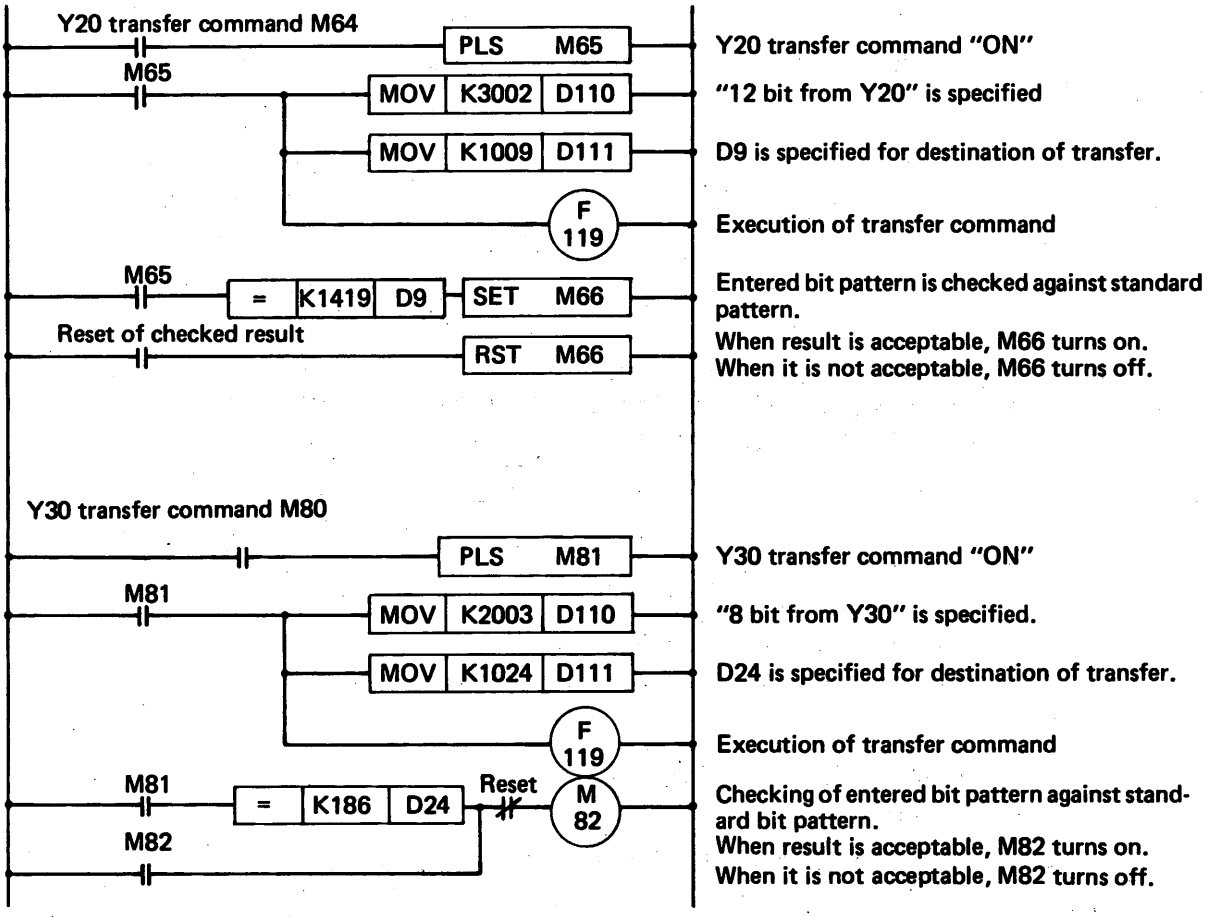


Fig. 5.4.11.2 Y → D Data Transfer Circuit

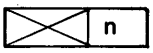
5.4.12 4←→16 Decode/encode

Decode means that 4-bit binary numerals are converted into 16-bit pattern. On the contrary, encode means that 16-bit pattern is converted into 4-bit binary numerals.
The decode function includes transference of converted 16-bit pattern to M, thereby M is used as control means. With this function, 1-bit in 16 bits is identified, and converted into binary numerals, thereby significant bit position is found.
The encode function may be used to identify step No. of counter, or shift position in 1-bit shift register.

5.4.12.1 Functions

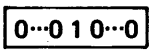
Function No.: F108

Data to be decoded or encoded: D110



Decode

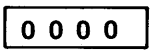
Lower 4 bits are effective and upper 12 bits are ignored in decoding.



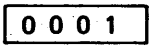
Encode

Only one "1" (H) bit exists in 16 bits in the case of encoding.

Decode/encode designation: D111

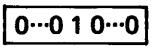


Decode



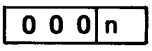
Encode

Decode/encode result: D112



Decode

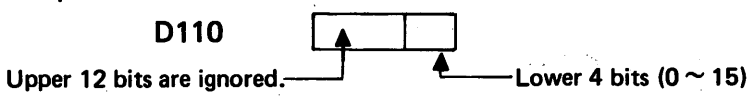
Only one "1" bit exists in 16 bits in the case of decoding.



Encode

In encoding, bit position is specified in lower four bits. Upper digits are filled all with "0".

(1) The data to be decoded or encoded is stored in D110.
   a) In decoding, only lower four bits (0 ~ 15 in decimal notation) are effective, and converted into bit pattern to be stored in D112.



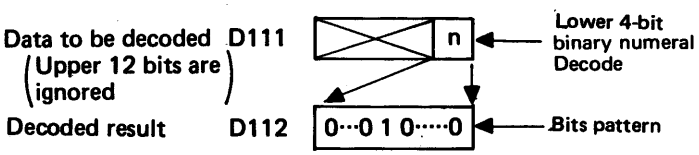
   b) In encoding, data having only one "1" (H) bit in 16 bits is handled. This single "1" bit is converted into 4-bit binary numerals, and stored in D112.
   The data handled in encoding should have only one "1" bit in 16 bits.

(2) Discrimination between decode and encode is specified in D111.

D111

   a) Decode 0 0 0 0
   b) Encode 0 0 0 1

(3) Decoded or encoded result is stored in D112.
   a) Decode



b) Encode

Data to be encoded D110 0 ····· 0 1 0 ··· 0 Bits pattern

Encoded result D112 0 ····· 0 | n Lower 4 bits are binary numerals

All upper 12 bits turn to "0".

(4) Decoded/encoded result

Table 5.4.12.1 Decoded/Encoded Results

ENCODE	D112 ←	D110
DECODE	D110 →	D112

	D112 15~4	3	2	1	Bit 0	D110 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
2	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
3	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
4	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
5	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
6	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
7	0	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
8	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
9	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
10	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
11	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
12	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
13	0	1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

a) In decoding, upper 12 bits of the data (D110) to be decoded are ignored.

b) In encoding, all upper 12 bits of the encoded result (D112) turn to "0".

(5) Circuit composition

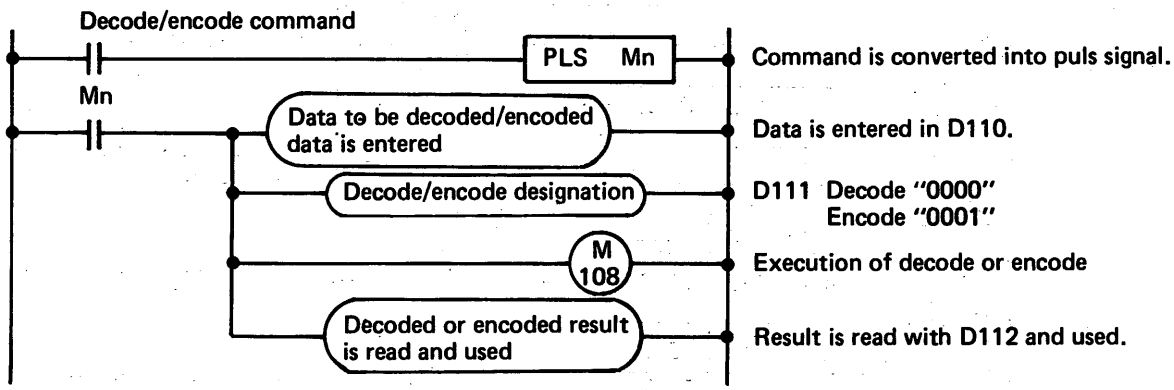


Fig. 5.4.12.1 Decode/Encode Circuit Composition

5.4.12.2 Circuit applications

(1) Decode circuit

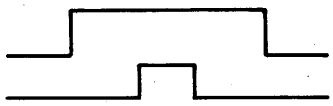
In this example, numerical data are taken from computer or N/C unit and converted into bit pattern for sequential control.

Input data and timing are assumed as follows:

Data: X0 ~ 3 4 bits, binary numerals

Data transmission: X4

Input timing: X0 ~ 3, X4



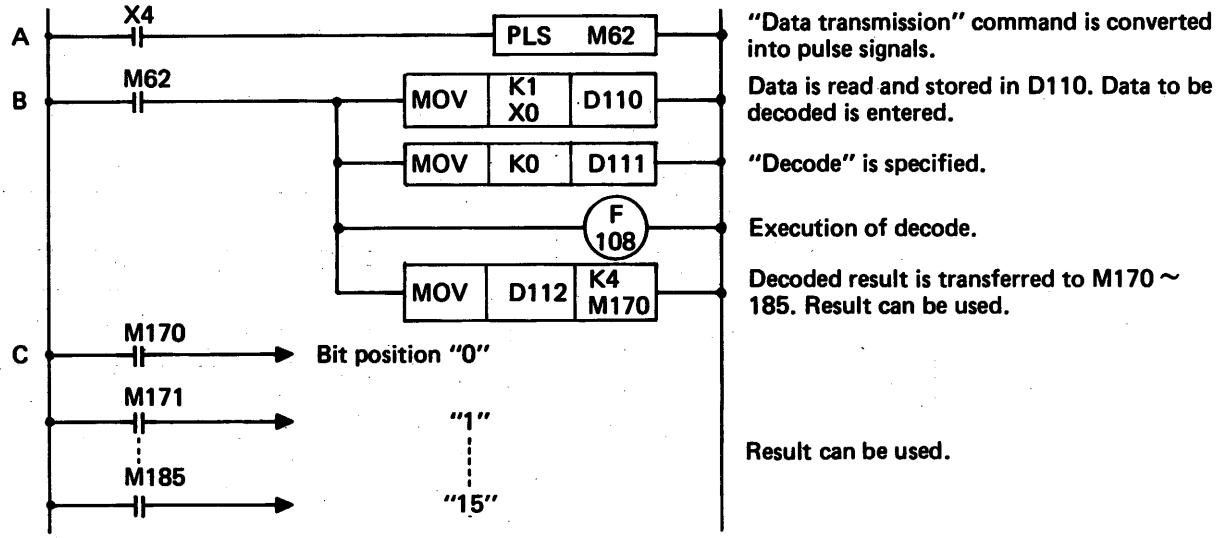


Fig. 5.4.12.3 Decode Circuit Composition

(2) Encode circuit

The example is that control command is changed by significant bit position where counter (1-bit data shift register) is on.

Counter : M130 ~ 145 16 bits

Bit position : 3 ~ 6 A control 7 ~ 11 B control 12 ~ 15 C control

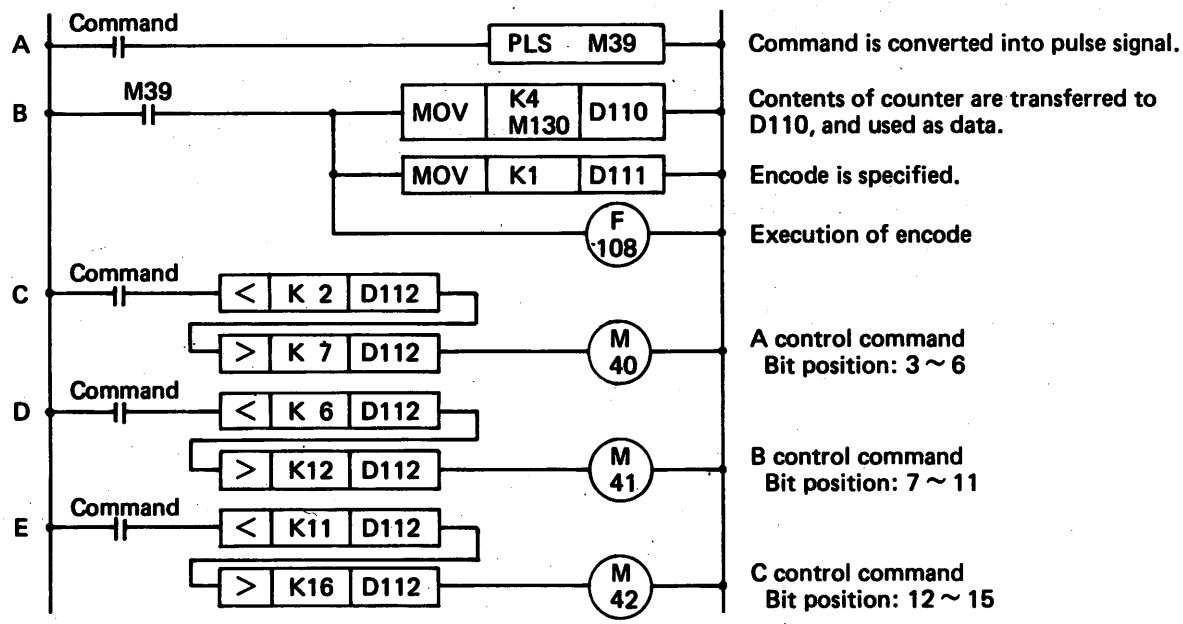


Fig. 5.4.12.4 Encode Circuit Composition

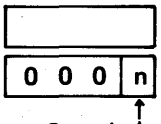
In this circuit, D112 is directly used for comparison. When D112 is used in any other circuit, M40 ~ M42 should be self-held, or D112 contents should be transferred to Dm for comparison.

5.4.13 16-bit check

This function is used to check and examine how many "1" (ON) bits exist in 16 bits of one register.
Practical application example of the function is that number of stored goods can be identified when flow of goods is traced in conveyor or any transfer, or material handling control system by making use of shift register functions, or the case where how many outputs are in ON within a certain range of output Y is examined.

5.4.13.1 Functions

Function No.:	F109
Check data:	D110
Cumulative number of bits:	D111



Cumulative number of bits ... binary numeral (0 ~ 16)

(1) Check data (how many bits of which are in ON is to be identified) are entered in D110.
(2) When F109 is executed, total number of bits in ON is stored in the lower four bits of D111 in the form of binary code and all upper 12 bits turn to "0".
(3) Circuit composition

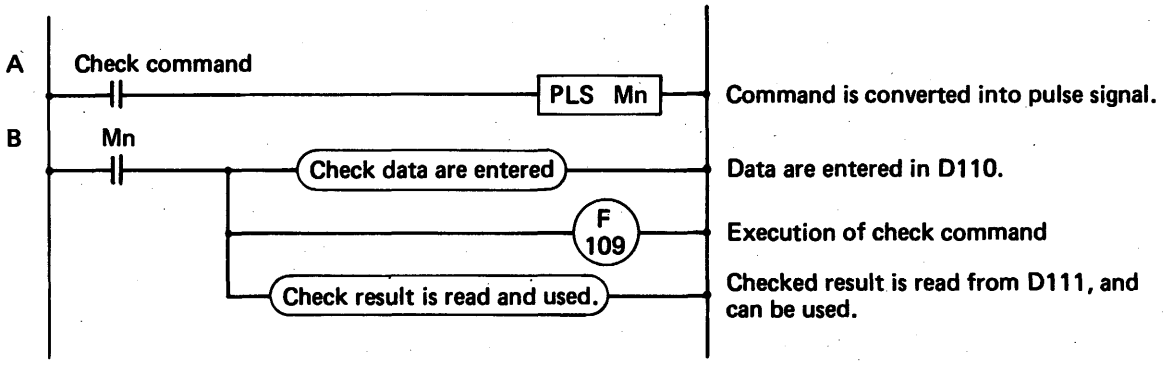


Fig. 5.4.13.1 16-bit Check Circuit Composition

5.4.13.2 Circuit applications

(1) Checking of number of bits "1" (ON) in shift register

This application example is used when number of goods in a conveyor line must be numerically displayed, for example.

Ex.: Shift register M50 ~ M81 32 bits
Display unit Y80 ~ Y87 Decimal 2 digits

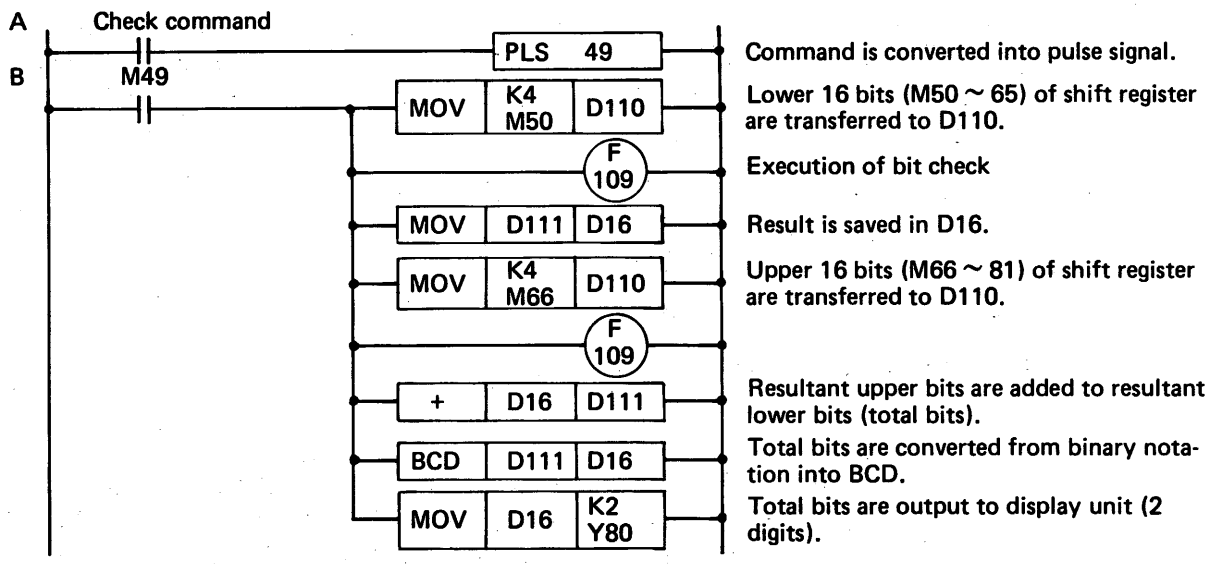


Fig. 5.4.13.2 Display of Number of Bits "1" in Shift Register

In the example shown in Fig. 5.4.13.2, number of stocked goods is numerically displayed. However, this circuit may be used for other control, such as quantitative comprison or definition of quantitative range of stored goods, by using instructions (>, <, =).

(2) Checking of number of bits "1" (ON) of output Y

In this example, number of bits being in "1" in output Y (4 bits) is checked. This application example may be actually employed for error detection.

Ex.: Output Y20 ~ 2B 12 bits
Error exists when number of bits "1" is larger than 9 bits.

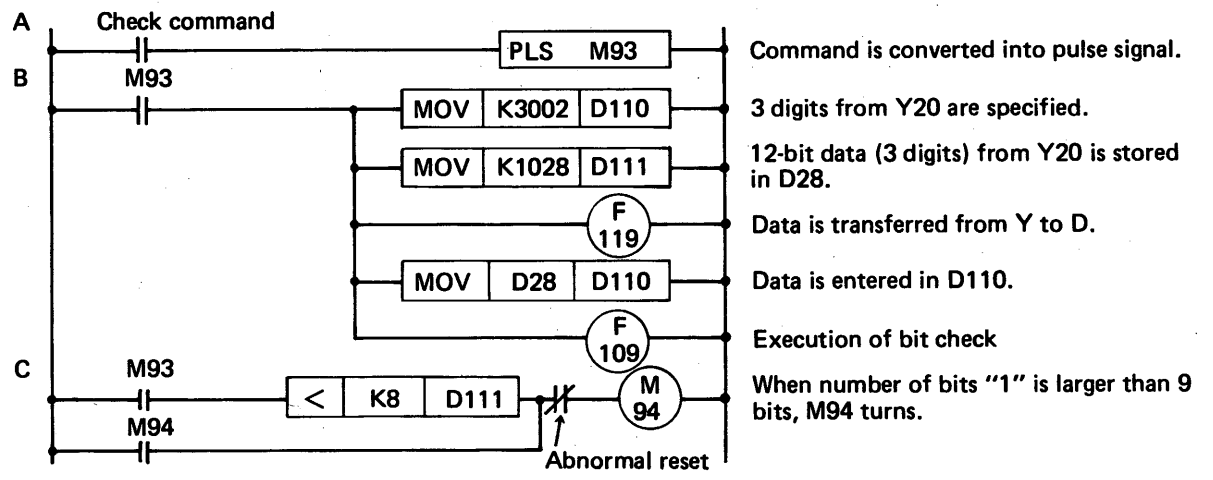


Fig. 5.4.13.3 Checking of Number of Bits "1" of Output Y

5.4.14 Data inversion

With this function, the contents in the specified data register are inversed, that is, "1"'s complement is obtained.

5.4.14.1 Functions

Function No.: F100

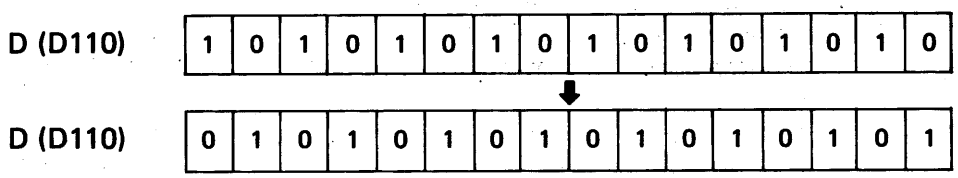


Fig. 5.4.14.1 Data Inversion

5.4.14.2 Circuit applications

Ex.: Since the subtracted result is obtained as "2"'s complement when the result is minus, it must be changed to absolute value as follows:

When (D10) – (D20) is equal to (D10), for example,

5 – 7 = –2 ⟶ 2

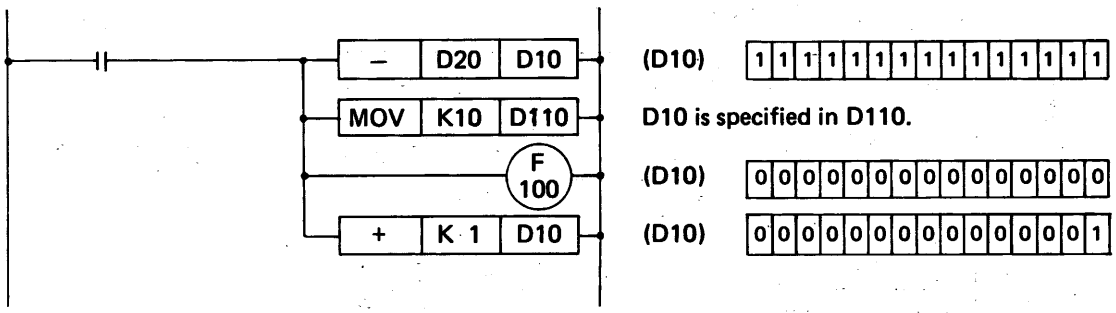


Fig. 5.4.14.2 Data Inversion Circuit

5.4.15 Functions and practical use of high-speed processing instructions

The high-speed processing instructions are that a program component required to high-speed processing is picked up, and high frequently executed several time as subroutine during execution of the main program at low speed, thus the executing time can be apparently shortened.

5.4.15.1 High-speed processing instructions and application data registers

(1) SET F126 : High-speed program call instruction
(2) RST F126 : High-speed program return instruction
(3) D126 : Register for storing of high-speed processing program head step No. (when 10mS timer is used)
(4) D123 : Register for storing of high-speed processing program head step No. (when call instruction is used)

5.4.15.2 Circuit applications

The circuit shown below is an example of practical application of the high-speed processing instructions, where it is intended to minimize timing error when Y20 and Y21 turn off.

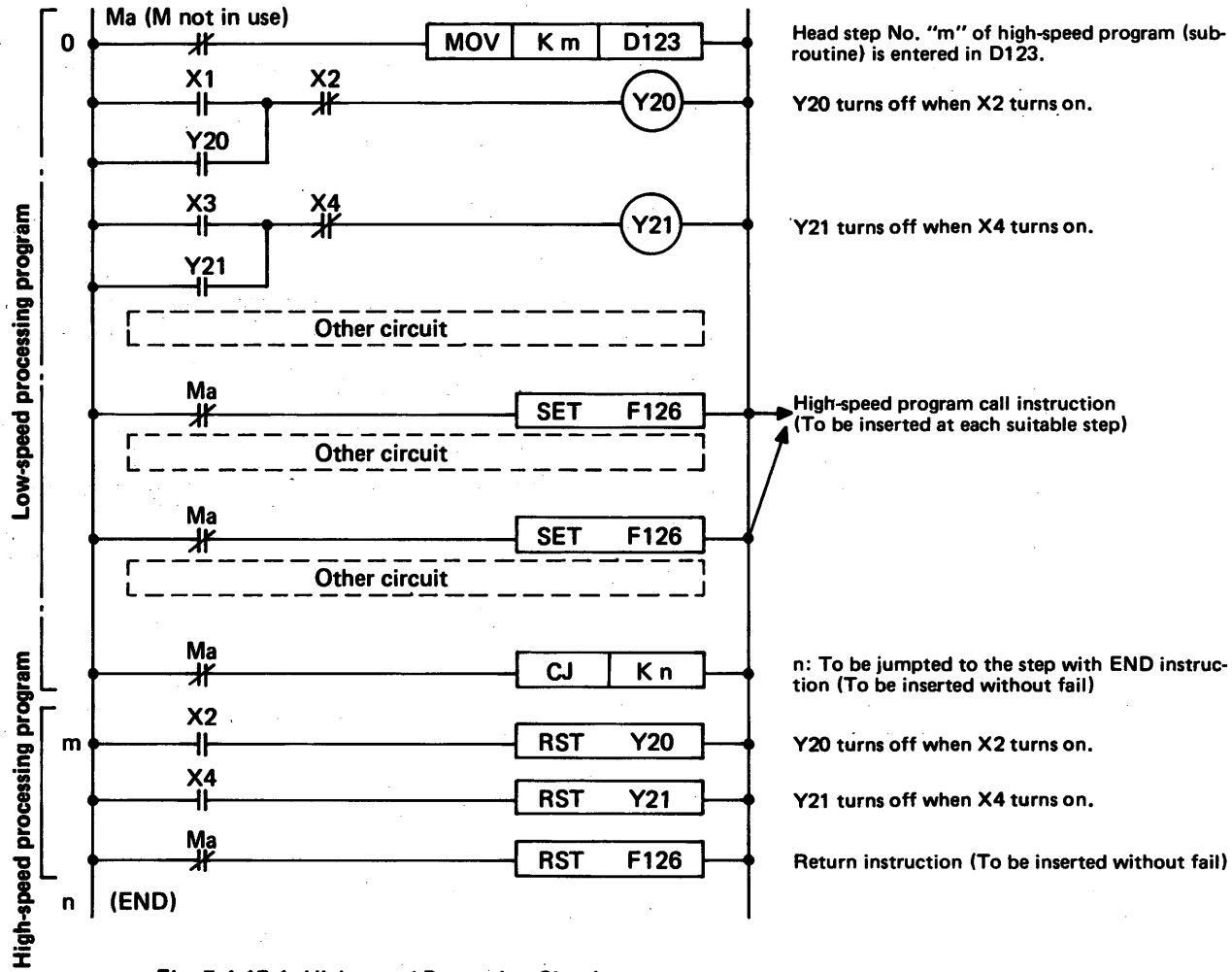
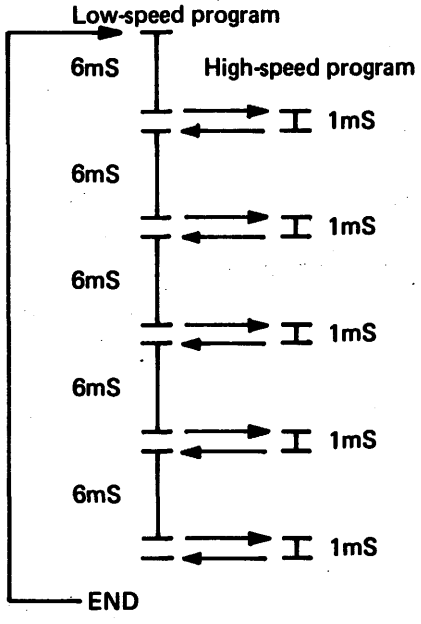


Fig. 5.4.15.1 High-speed Processing Circuit

(1) In order to minimize timing error at the time Y20, Y21 turn off, only Y20/Y21 reset circuit is programmed for high-speed processing.
(2) At the head of the low-speed program, the head step No. "m" of high-speed program component should be placed in D123, as shown in Fig. 5.4.15.1.
(3) For example, high-speed processing call instruction F126 should be inserted with suitable step internal, like 6mS.
(4) At the end of the low-speed processing program, CJ instruction should be inserted without fail and program sequence should be jumped to the step with END instruction.
(5) At the end of the high-speed processing instruction, return instruction F126 should be inserted without fail.
(6) END instruction should come next to the return instruction. This means that the high-speed processing program should be inserted before the END instruction.
(7) Program execution flow chart and execution time



Note 1: When scanning time exceeds 100mS, WDT error occurs.

Fig. 5.4.15.2 Program excution flow chart and excution time (when used Call instruction.)

5.4.15.3 Program for 10mS high-precision timer

96 timers (100mS), T0 ~ T95, and 32 timers (10mS), T96 ~ T127, are incorporated in MELSEC-KOJ1U.
Fig. 5.4.16.3 shows an example of circuit used in programming for 10mS precision timers.

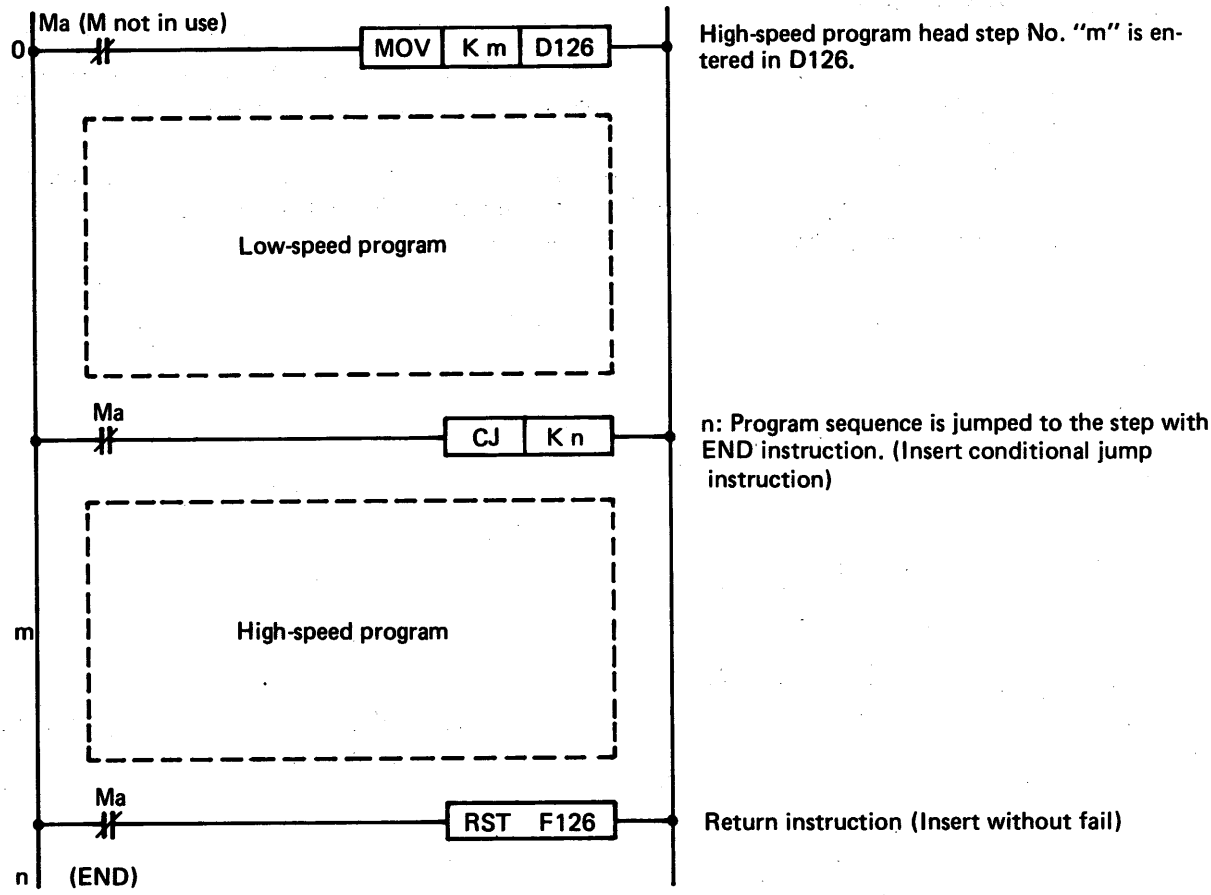
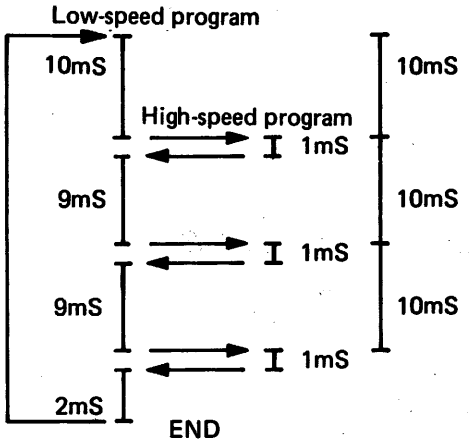


Fig. 5.4.15.3 Circuit for Programming with 10mS Timers

(1) When 10mS timer is used, the high-speed program head step No. "m" should be entered in D126 without fail.
(2) CJ instruction should be inserted at the end of low-speed program to let the program sequence jump to the step with END instruction.
(3) Return instruction RST F126 should be inserted at the end of high-speed program.
(4) Coil of 100mS timer (T0 ~ T95) should be inserted in the low-speed program, and coil of 10mS timer (T96 ~ T127) in the high-speed program.

(5) Program execution flow chart and execution time
Fig. 5.4.15.4 shows an example of execution flow chart and execution time, where the low-speed program has about 1000 steps and the high-speed program has 33 steps (same as the example shown in above mentioned (7) of 5.4.15.2).
In this example, execution times are 30mS and 1mS for low-speed program and high-speed program respectively.



Note 1: High-speed program is executed at every 10mS.
Note 2: Scanning time: 33mS

Fig. 5.4.15.4 Program Execution Flow Chart and Execution Time (When used with 10mS timer)

(6) High-speed timer function may be associated with call instruction SET function F126.
When the both functions are used at the same time, high-speed program head step No. "m" should be entered in D126 as well as D123.
In the case where the example in Fig. 5.4.15.2 combined with the example in Fig. 5.4.15.4, the high-speed program is called 8 times and the scanning time is 38mS.

5.4.16 Programming error display

The following two types of error check are available in the programming related to high-speed program.
When error is found, "RUN" display flickers.

(1) High-speed program time over (Error No.: 5030)
If execution time exceeds 10mS in high-speed processing (timer 10mS is used), the time over error occurs.
The high-speed processing should be executed within 10mS.
(2) Programming error (Error No.: 5031)
This error occurs when CJ Kn, RST F126 shown in Fig. 5.4.15.1 and 5.4.15.3 are not entered.

Note: Error No. may be verified in test mode of PU and GPP.

5.4.17 Scan time restriction

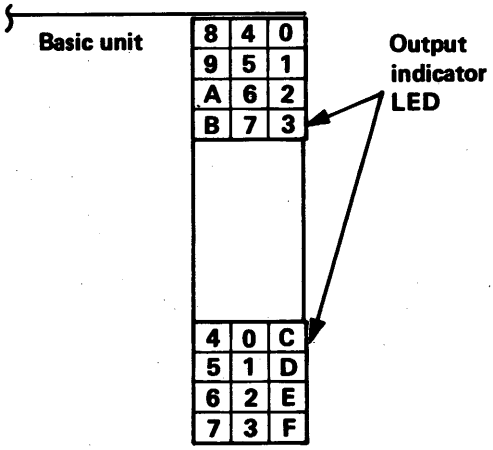
The check time of arithmetic operation watchdog timer (WDT) of KOJ1U is 0.1 second. The CPU resets the WDT after END instruction. When scan time exceeds 0.1 second, WDT error occurs and all outputs are turned off by hardware.

Scan time (Ts) = instruction execution time (T1) + peripheral unit intervention time (T2) (Max. 10mS)

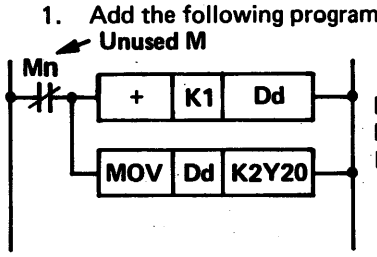
- Example of maximum instruction execution time

Max. instruction execution time = 100ms − 10mS = 90mS
(T2)

- Instruction execution time measuring method



1. Add the following program to the prepared program.



2. When the sequencer is run, Y20 to Y27 displays are indicated with 0 ~ 255 ~ 0. Therefore, measure the time T, i.e. from when Y20 to Y27 are all turned off to when they are all turned on again.

3. Overall instruction execution time (T1)

T1 = T/256

5.4.18 List of arithmetic operation processing time

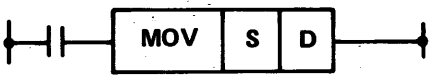
Sequence instruction

Instruction	Condition	Time (μS)
LD	X, Y	5.6
	M,T,C,F	
LDI	X, Y	
	M,T,C,F	
AND	X, Y	
	M,T,C,F	
ANI	X, Y	
	M,T,C,F	
OR	X, Y	
	M,T,C,F	
ORI	X, Y	
	M,T,C,F	
OUT	M	
	Y	
OUT F0 ~ 99	Non execution	81
	Execution	260
SET, Y	Non execution	5.6
	Execution	
SET, M	Non execution	
	Execution	
SET F0 ~ F99	Non execution	77
	Execution	260
RST M	Non execution	78
RST F	Execution	83
RST Y	Non execution	78
	Execution	93
RST C	Non execution	78
	Execution	95
SFT M	Non execution	82
	Execution	82
PLS M	Non execution	82
	Execution: 1st scan	87
	Execution: 2nd scan	88

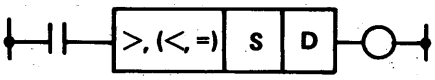
Instruction	Condition			Time (μS)
ANB	——			5.6
ORB	——			5.6
MC	——			84
MCR	——			79
NOP	——			5.6
END	——			170
OUT.T	Non execution			93
	Execution	Not added		103
		After time-up		90
		Added	K	130
			D	120
OUT.C	Non execution			90
	Execution	Not added		90
		After count-up		90
		Add	K	100
			D	100
CJ	Non execution			83
	Execution			120

Data instruction

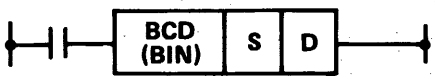
Instruction	Condition	Time (μS)
Data instruction	Non execution	83



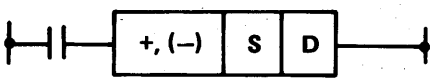
S	D	TIME (μS)
K	D	150
D	D	190
T	D	180
C	D	180
X	D	480
M	D	440
D	T	190
D	C	200
D	Y	500
D	M	630



Instruction	S	D	Time (μS)
>	K	D	180
	D	D	
<	K	D	
	D	D	
=	D	D	
	D	D	



Instruction	S	D	Time (μS)
BCD	D	D	660
	T	D	660
	C	D	660
BIN	D	D	290
	X	D	660



Instruction	S	D	Time (μS)
+	K	D	180
	D	D	
–	K	D	180
	D	D	

Application instruction

Ins. code	Content		Time (mS)
F108	4 ↔ 16	Decode	0.14
		Encode	0.16
F109	16-bit check		0.33
F114	Batch shift of M	10 bits	0.30
		100 bits	1.2
		200 bits	2.1
F115	Batch shift of D	5 data	0.31
		10 data	0.48
		50 data	1.0

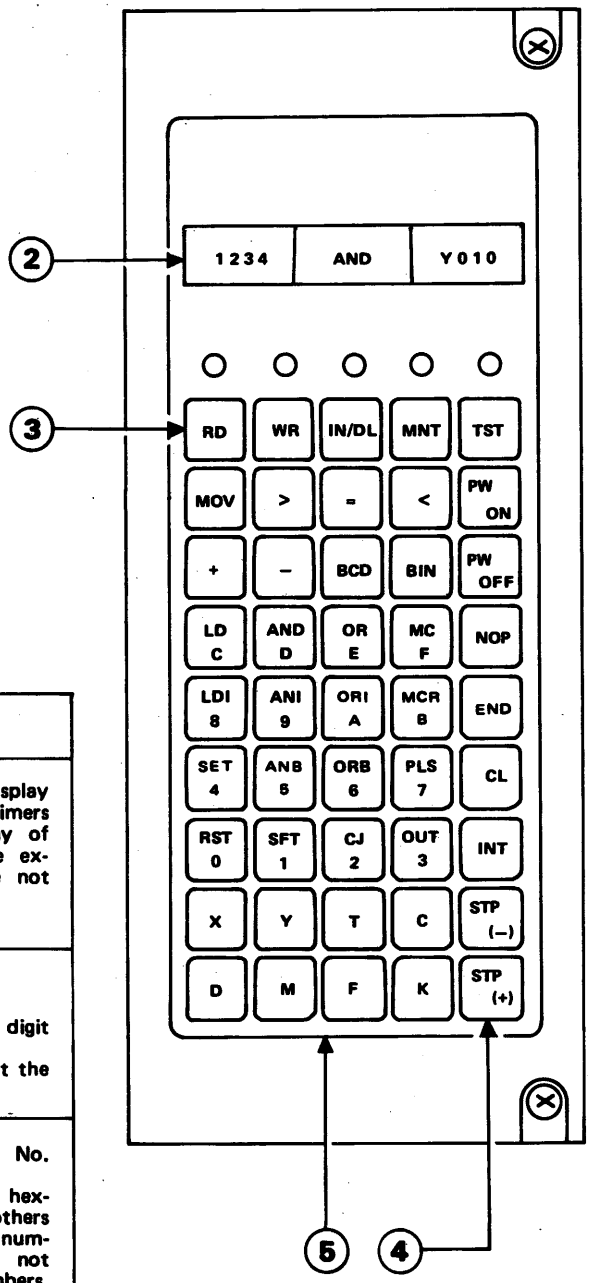
Ins. code	Content		Time (mS)
F116	Batch reset of D	10 data	0.33
		30 data	0.56
		90 data	1.3
F117	Indirect reading T,C,D		0.25
F118	Indirect writing of T,C,D		0.27
F119	Y → D data transfer		0.66
F100	16-bit data inversion		0.13
F110	8-bit data association		0.19
F111	16-bit data dissociation		0.19
F112	16-bit data AND		0.21
F113	16-bit data OR		0.21

6. PROGRAMMING UNIT

6.1 Explanation of Programming Unit Functions (K7PUE)

①Outline

○ Program read-out	(READ)
○ Program search	(READ)
○ Program write	(WRITE)
○ Program insertion	(INSERT)
○ Program deletion	(DELETE)
○ Check of the operation status	(MONITOR)
○ Forced output	(TEST)
○ Set and reset of latch and temporary memory, etc.	(TEST)



②DISPLAYS

Name	Display example	Function
Step No. (left side)	1 2 3	Display of step number, display of temporary values of timers and counters, and display of data register content are executed. Leading zeros are not displayed. Example: 0056 → 56
Instruction or constant, ON, OFF (center)	(1) A N D (2) K (3) O F F	(1) Display of instructions (2) Display of constants, digit symbol K (3) Display of ON, OFF at the time of monitor
Input/output (right side)	X 0 1 0 T 2	Display of input/output No. (device No.) is executed. X and Y are displayed as hexadecimal numbers, while others are displayed as decimal numbers. Leading zeros are not displayed for decimal numbers, but they are displayed for hexadecimal numbers.
Message display is executed using all of the above 3 types of displays. Example: MODE SET ERR.		

③MODE KEYS

Operation mode	Functions and Applications
READ (RD)	Read-out of the programs written into the memory and step number search by instructions or input/output number are possible. This is used for check of the memory contents.
WRITE (WR)	Writting of programs, timer and counter set values, etc. into the memory and consecutive writing of NOP instructions are possible. This is used for program writing and changes.
INSERT/DELETE (IN/DL)	All programs from the set step number on are shifted down by one step, and the newly set instruction is inserted at the position of the step number. Otherwise, all programs from the set step number + 1 on are shifted up by 1 step and the instruction which was at the set step number is deleted. This is used for program additions and deletions.
MONITOR (MNT)	The ON, OFF status of X, Y, M, T, C , F, and K, the temporary value of timers and counters, and the countent of D can be monitored. This is used for check of the operation status.
TEST (TST)	Forced output and latch of Y, set and reset of M and F, reset of T and C temporary value and contact, and reset of the content of D can be executed. Error generation step number read-out at the time of abnormal code error occurance is also possible. This is used at the time of test, at the time of inspection, and operation rise, etc.

④

Key name	Functions and applications
POWER ON (PW ON)	These keys are used to turn on and off the program unit power control section.
POWER OFF (PW OFF)	The CPU power cannot be turned on and off by these keys.
SET (INT = Set the initial step No.)	This key is used to declare the setting of initial step number.
CLEAR (CL)	This key is used to clear set content and display. It does not have influence on CPU program. This key is used to confirm ready status after power turns on and to re-execute operation in the case of key operation errors.
STEP (+) (STP(+))	This key is used to execute the step number or to insert for the step number of the input/output instruction, or when output is forced ON.
STEP (−) (STP(−))	This key is used to execute the step number or to delete for the step number of the input/output instruction, or when output is forced OFF.

⑤DEVICE KEYS

Device	Nomenclature		
X	Input signal	Example	X 0 1 0
Y	Output signal Latch, analog timer		Y 0 2 0
M	Temporary memory		M 1 2 3
T	Timer		T 1 6
C	Counter		C 3 2
D	Data register		D 1 8
F	External failure memory		F 5 5
K	(1) Constant	Example	K 1 2 3
	(2) Digit number		K 4 Y 0 2 0
	(3) MC, MCR number		K 1 2

6.2 List of Operations

	Mode		Operation
1	READ	Mode to read the memory of sequencer CPU	
	Program read-out with step number designation		RD INT Step No. □□□□ STP(+)
	Step number read-out with instruction or instruction and input/output number designation		RD Ins. key STP(+)
	Search of step number and used instruction with input/output number designation		RD I/O No. STP(+)
2	WRITE	Mode for writing new program into RAM memory or for altering program partially.	
	All clear (All programs written in RAM memory are cleared)		WR INT 0 STP(+) NOP K Memory final step □□□□ STP(+)
	Writing of sequence instruction		WR INT 0 STP(+) Ins.key SPT(+)
	Writing of data instruction		WR INT Step No. □□□□ STP(+) Data ins. STP(+) Data ins. STP(+) Data ins. STP(+)
	Alteration of program		RD INT Step No. □□□□ STP(+) WR Ins.key STP(+)
	Consecutive writing of NOP instructions		WR INT Step No. □□□□ STP(+) NOP K Final step No. □□□□ STP(+)
3	INSERT/DELETE	Mode to add and delete programs to and from RAM memory in order to change programs.	
	Program insertion		RD INT Step No. □□□□ STP(+) IN/DL Ins.key STP(+)
	Program deletion		RD INT Step No. □□□□ STP(+) IN/DL STP(+)
4	MONITOR	Mode for monitoring the operation status of the sequencer.	
	On-off status of X, Y, M, F, MC K		MNT I/O No. STP(+)
	On-off status of T, C temporary values and contact		MNT T/C No. STP(+)
	Monitoring of D		MNT D No. STP(+)
5	TEST	Mode to easily perform test of sequencer alone or test of sequencer connected with controllled device.	
	Forced ON, OFF of output Y	ON	TST Y No. STP(+)
		OFF	TST Y/No. STP(−)
	M and F set	Set	TST M/F No. STP(+)
		Reset	TST M/F No. STP(−)
	T, C and D reset		TST T/C/D No. STP(−)
	Reading of error occurrence step number at the time of abnormal code generation		K STP(+)

6.3 Error Messages and Corrective Actions

No.	Message	Message Contents	Corrective Action
1	CANT FIND	Search was executed at the time of program search, but the searched number could not be found. (This is not an error.)	Since this is not an error, the next operation can be executed.
2	CANT OPE.	Operations of write and insert/delete and not possible during RUN of CPU switch to reset the CPU. Writing during RUN can be made by changing initialization.	After stopping the CPU, execute the operation again. If the operation cannot be made, press the [RESET].
3	CJ STEP ERR.	In [WRITE] or [INSERT] mode (1) Jump destination step number of a CJ instruction is smaller than the present step number. (2) Jump destination step number has exceeded the max. step number of CPU (1023, 2047, 4095). (3) Jump destination step number has exceeded the max. step number because it was inserted in [INSERT] mode. (At this time, program insertion is executed.)	Press the [WRITE] or [INSERT] mode key again, and set jump destination step number again or alter program.
4	DUAL COIL ERR.	The same coil has been set in [WRITE] or [INSERT] mode. In this case, only program writing is executed.	Write a correct program. (Even if the same coil is set, error message may not be displayed sometimes.) When correct, proceed with writing operation.
5	INS. CODE ERR.	Conversion to an instruction is not possible, because of a wrong machine code.	Rewrite the correct instruction in [WRITE] mode.
6	INS. SET ERR.	In [WRITE] or [INSERT] mode (1) Combination of instruction and input/output number is wrong. (2) The 2nd or 3rd word is not written when 2-word or 3-word instruction is written.	Press the [WRITE] or [INSERT] mode key again and set the instruction again with instruction key.

No.	Message	Message Contents	Corrective Action
7	IO SET ERR.	Input/output number which cannot be set has been set.	Set the input/output number which is within correct range.
8	IONO OVER ERR.	The set input/output number exceeds the maximum number.	Set the input/output number which is within correct range.
9	MODE SET ERR.	A key other than the [CLEAR] key has been operated without selecting a mode key.	First select an operation mode with a mode key.
10	OPE. ERR.	Operation other than those listed in 6.2 has been set.	Restart setting from the pressing of the [INT] key.
11	RDY	This is not an error message and displayed in normal conditions. (1) The [POWER ON] key has been pressed and the control power of PU has been turned on. (2) The [CLEAR] key has been pressed.	When RDY is displayed, proceed with the operation as desired. When RDY is not displayed with the operations described at left. (1) Press the [POWER OFF] key and then press the [POWER ON] key again. If RDY is not displayed after aforementioned operation, the hardware is defective. (2) Possible cause is the wrong installation of PU. Remove and reinstall the PU.
12	STEP OVER ERR.	The step number is larger than the maximum step number.	Press the [INT] key and set a correct step number.
13	WR. ERR.	A program cannot be written into memory. (Although program has been written, the results of automatic check shows no coincidence.)	(1) Check if RAM is mounted. (2) Check if P-ROM is mounted. (3) Check if RAM is fitted to socket properly. (4) If the error is displayed again after rewriting, possible cause is the failure of RAM. Therefore, change RAM.

7. OPERATING PROCEDURE

7. OPERATING PROCEDURE

Test run flow → Step 1 → Step 2 → Step 3 → Step 4 → Step 5

Step 1

Memory types and Settings

Memory	No. of steps	Memory fitted to socket	CON setting	Socket fitting
RAM	1024	Standard equipped	RAM ROM	1 24 12 13
	2048	Standard equipped + KORAM (HM6116LP3)		
ROM	2048	2KROM(equivalent to 2732)	RAM ROM	

Note: When fitting socket, do not bend the lead legs of IC memory. Do not touch the lead areas by hand.

Extension unit No. setting

System: Basic unit, Ext. unit 1, Ext. unit 2

Switch setting: EXTENSION 1 SW, EXTENSION 2 SW

Basic unit K65B/K68B SW

1 2 3

Turn on only SW1.

Extenion cable wiring

1: KOJ basic, KOJ extension, KOJ extension

(KOJ-61CBL/KOJ-61CBL2) (KOJ-61CBL/KOJ61CBL2)

Note: Extension cables are available in 2 types of length. Either of upper or lower connector can be used as extension connector.

2: KOJ basic, K65B/K68B extension

KOJ-62CBL

Battery connection

Red lead wire, Blue lead wire, Battery, (+), (−)

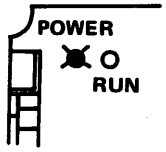
Note: When IC-RAM or EP-ROM is also provided with backup for power failure, battery is used. Connect lead wires of battery with connectors on printed circuit board, taking care of polarity.

STEP 2

Step 2 → **Power on**

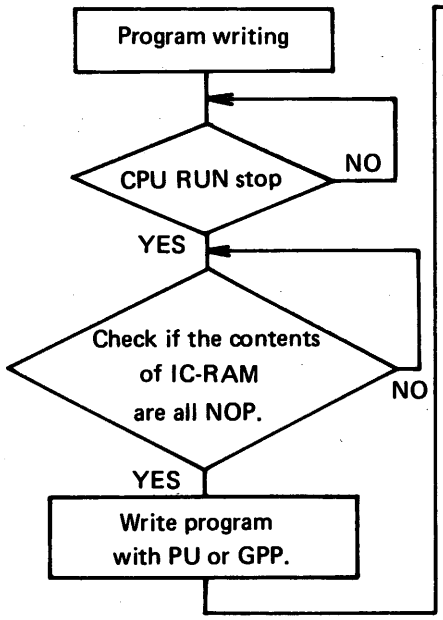
- After confirming line voltage, turn on the power.

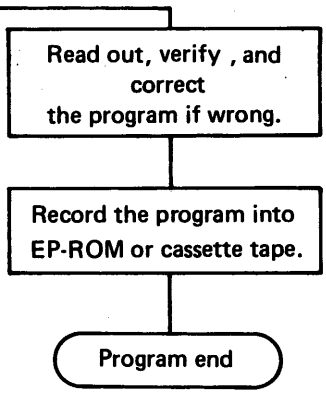
(Line voltage)
AC 115 V ± 15%



- Make sure that the POWER LED on basic unit turns on.

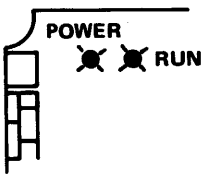
Step 3 → **Program writing**



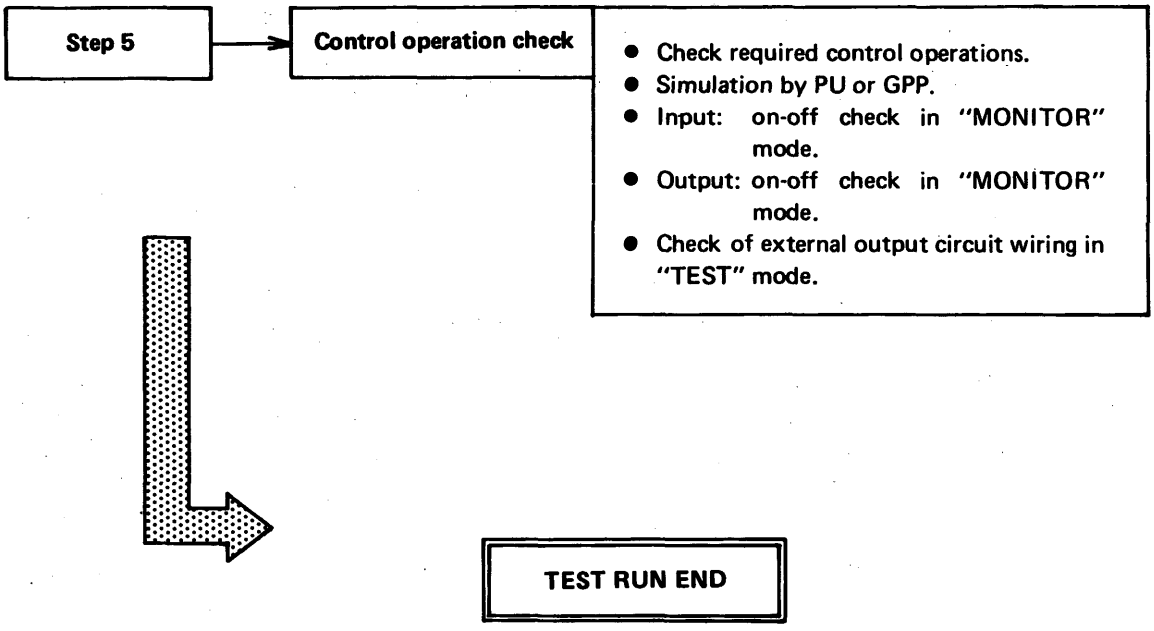


STEP 4 → **CPU test run**

- Set the RUN switch of basic unit to RUN position.
- Make sure that the RUN LED is lit. If the RUN LED flickers, something is wrong. In this case, check the following:
  - Program not provided with END instruction
  - Mistake in selecting between ROM and RAM
  - Abnormal program, etc.



STEP 5


Step 5
Control operation check
● Check required control operations.
● Simulation by PU or GPP.
● Input: on-off check in "MONITOR" mode.
● Output: on-off check in "MONITOR" mode.
● Check of external output circuit wiring in "TEST" mode.
TEST RUN END

8. INSTALLATION AND WIRING

8.1 Instructions for Installing Location

The KOJ1U has excellent durability against severe environmental conditions as well as high reliability.
However, in order to obtain higher reliability as a system, please install the KOJ1U in full consideration of the following:

Avoid installation at the locations described below.

(1) When the KOJ1JU is installed at locations or within panels where ambient temperature is outside the range of 0°C and 55°C, it is recommended to provide a ventilation fan at top.
(2) Locations where ambient humidity exceeds 90% RH, and locations where dew condensation takes place due to sudden temperature changes.
(3) Locations where acceleration exceeds 2 g with vibration at 10 to 55 Hz and amplitude at 0.5 mm, and locations where shock exceeds 10 g.
(4) Locations where there are particularly a lot of conductive powder such as dust and iron fittings, corrosive gases (acid, alkali), oil mist, salt, and organic solvents.
(5) Locations exposed to the direct rays of the sun.
(6) Locations having high electric field or high magnetic field.

8.2 External Dimensions

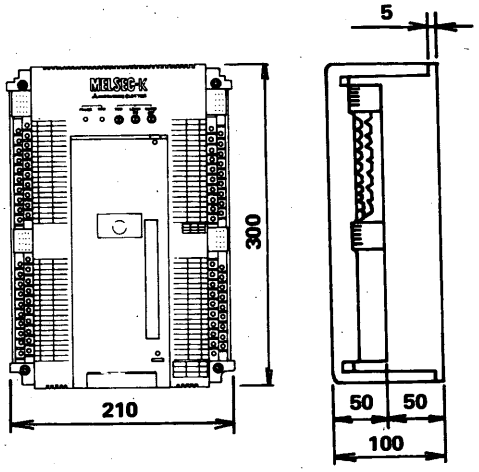


Fig. 8.2.1 External Dimensions of Basic Unit

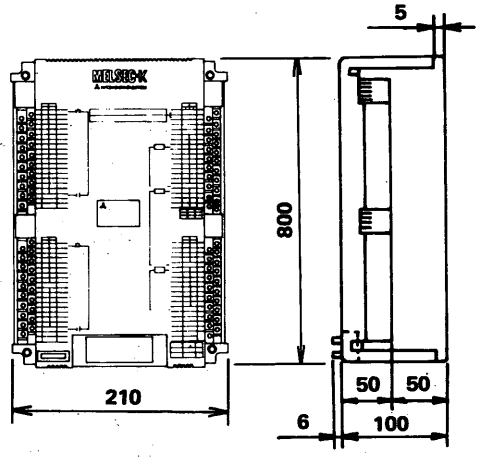


Fig. 8.2.2 External dimensions of E56 Extension Unit

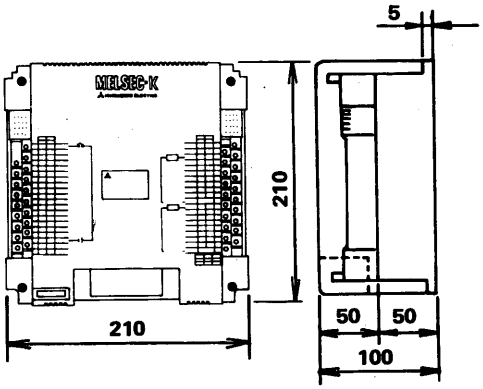


Fig. 8.2.3 External Dimensions of E32 Extension Unit

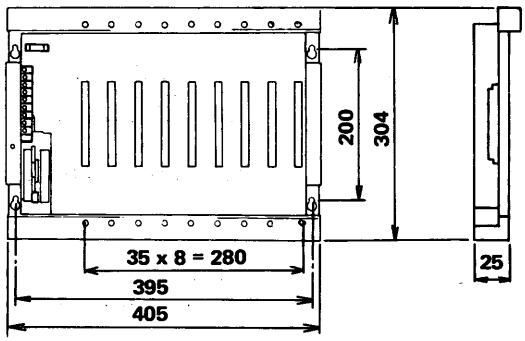


Fig. 8.2.4 External Dimensions of K68B Extension Unit

8.2.1 Mounting dimensions

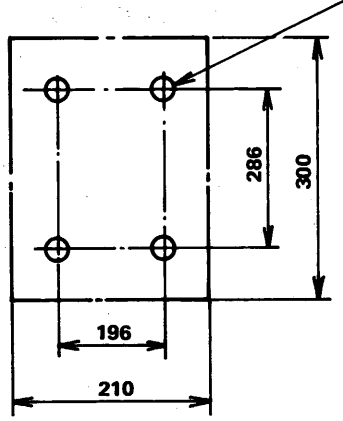


Fig. 8.2.5 Mounting Dimensions of Basic Unit and E56

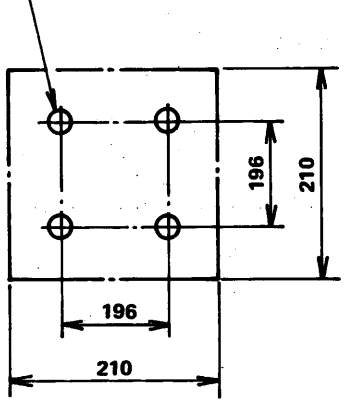


Fig. 8.2.6 Mounting Dimensions of E32

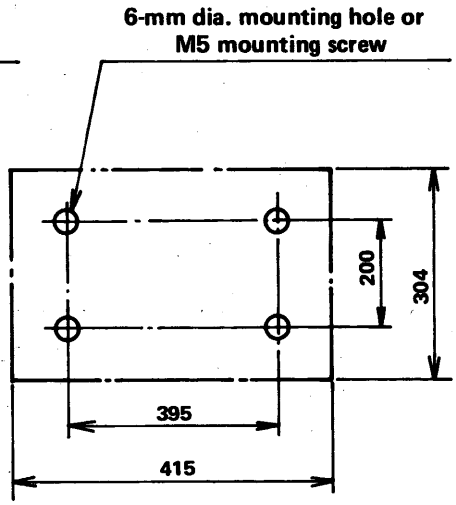
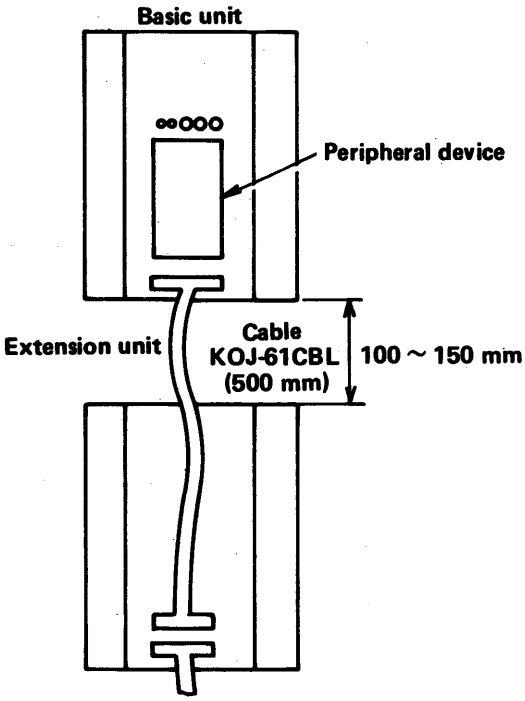
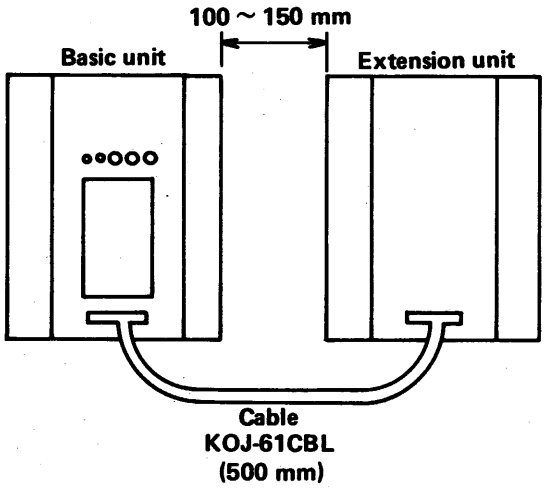


Fig. 8.2.7 Mounting Dimensions of K68B

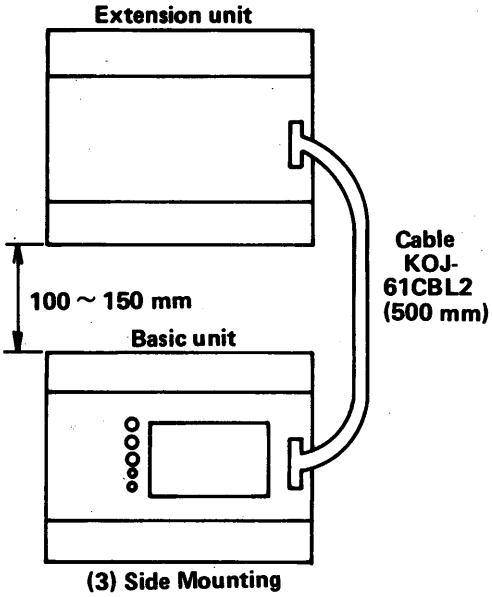
8.3 Panel Mounting Dimensions



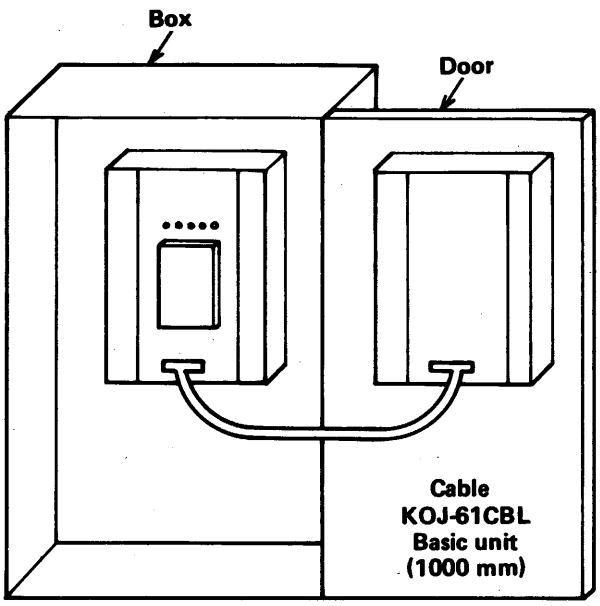
(1) Series Mounting



(2) Parallel Mounting



(3) Side Mounting



(4) Door Mounting

Fig. 8.3.1 Mounting Methods of KOJ1U

The KOJ1U may be mounted horizontally on the bottom surface of operating panel. However, because of poor ventilation and the absence of ventilating hole, temperature may possibly rise to excess. In horizontal mounting, therefore, provide cooling means.

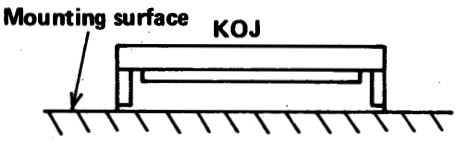


Fig. 8.3.2 Horizontal Mounting

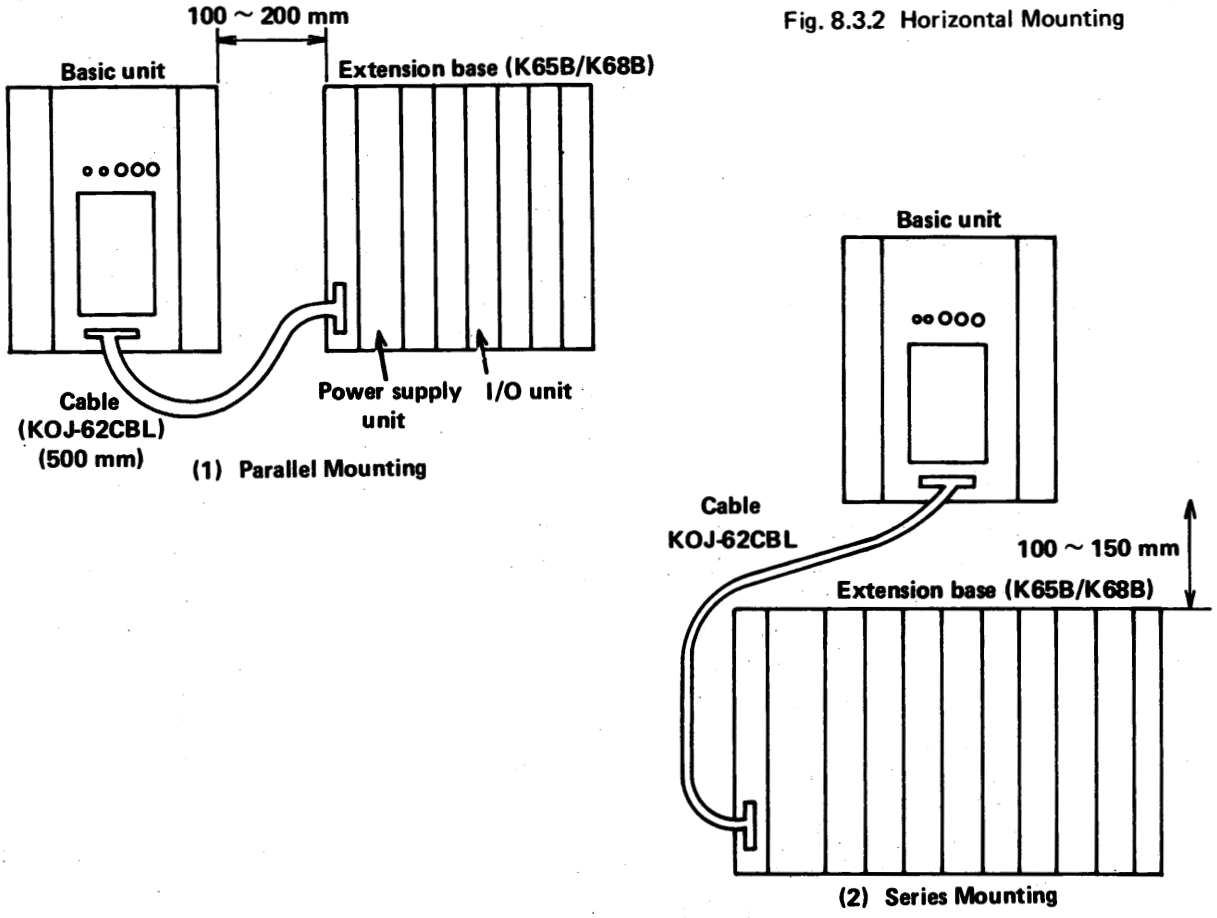
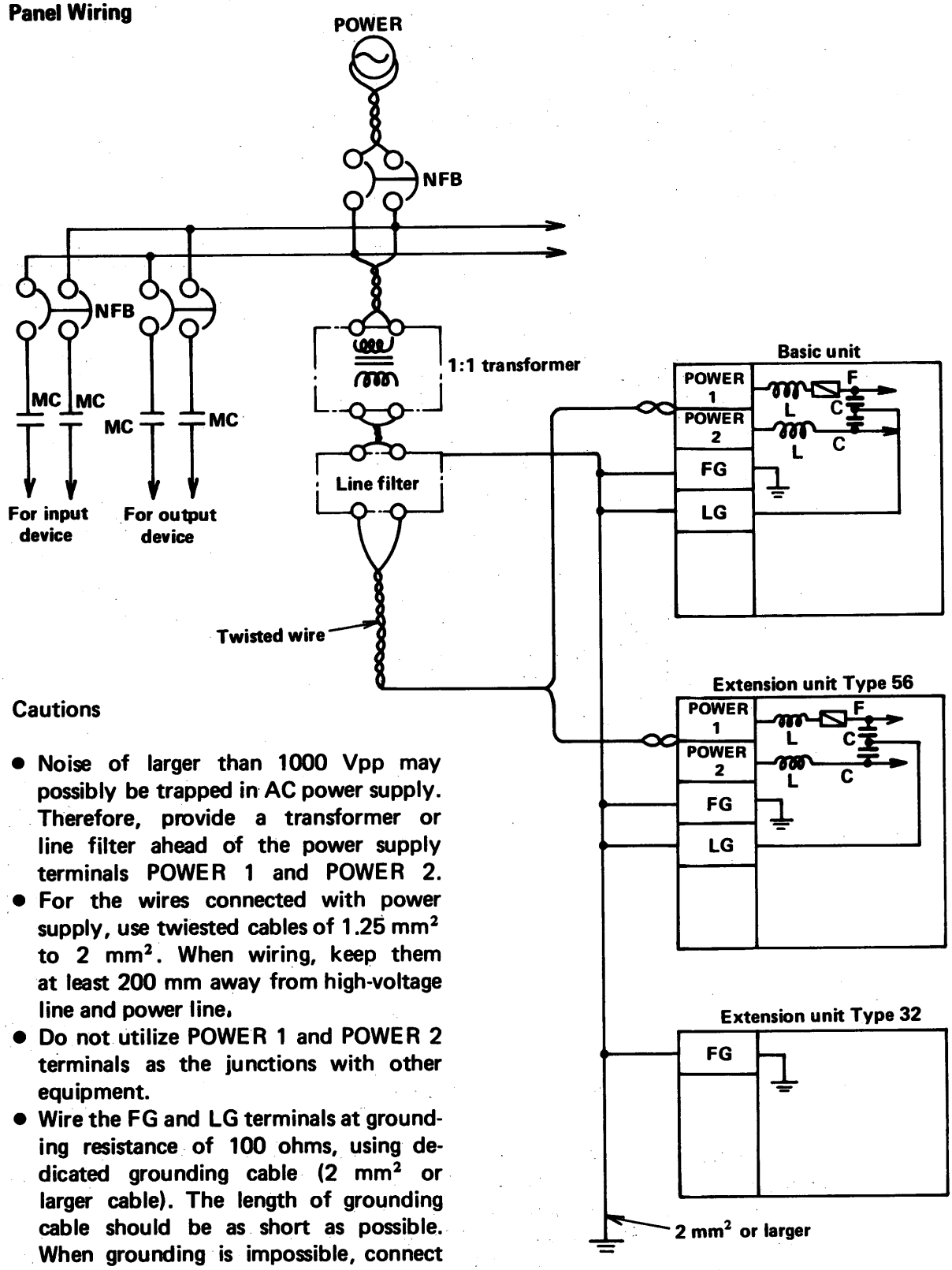


Fig. 8.3.3 Mounting to Extension Base

When the KOJ1U is used together with K65B/K68B extension base, install as shown in Fig. 8.3.3. When the panel door is on the left, the KOJ1U can be mounted on the door, and the extension base on the panel. In this case, cable used is KOJ-62CBL2 in 1000 mm length.
In the case of (2) Series Mounting, side mounting may be applied to the basic unit. Horizontal mounting shown in Fig. 8.3.2 is not applicable to the extension base. Side mounting of input/output unit, etc. is not possible, either.

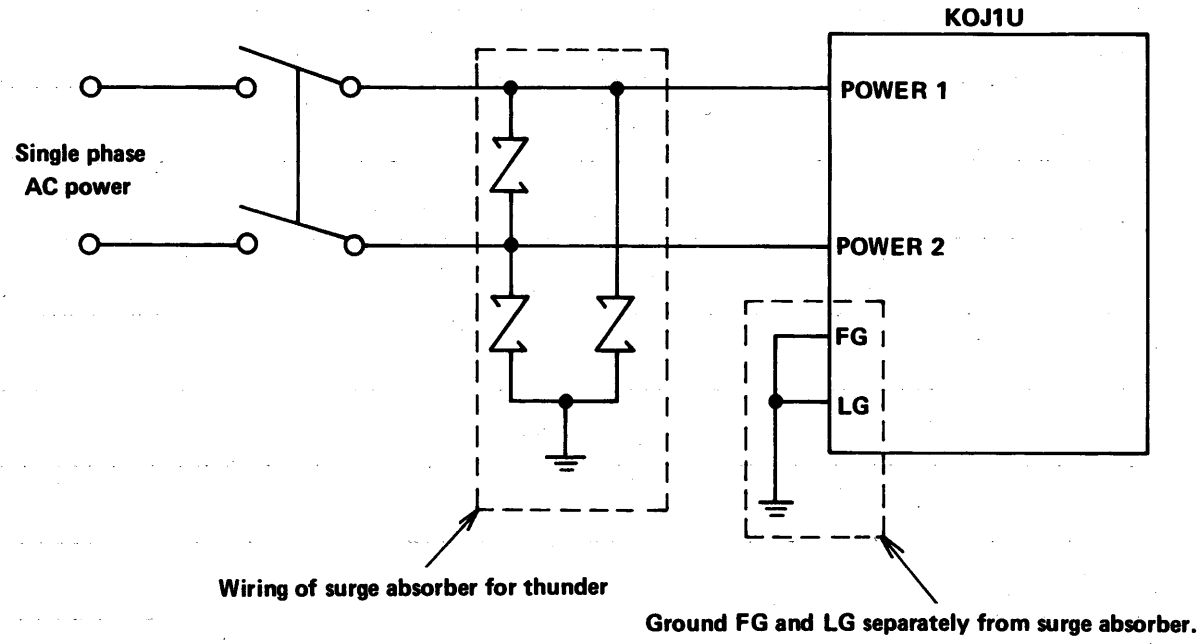
8.4 Panel Wiring



Cautions

- Noise of larger than 1000 Vpp may possibly be trapped in AC power supply. Therefore, provide a transformer or line filter ahead of the power supply terminals POWER 1 and POWER 2.
- For the wires connected with power supply, use twiested cables of 1.25 mm^2 to 2 mm^2. When wiring, keep them at least 200 mm away from high-voltage line and power line.
- Do not utilize POWER 1 and POWER 2 terminals as the junctions with other equipment.
- Wire the FG and LG terminals at grounding resistance of 100 ohms, using dedicated grounding cable (2 mm^2 or larger cable). The length of grounding cable should be as short as possible. When grounding is impossible, connect the cable to the panel.
- If grounding cable is used also for other equipment or connected with the beam of building, contrary effect is produced and the units may be adversely affected. For this reason, be sure to perform dedicated grounding.

8.5 Measures against "Thunder" Power Surge when AC Power Supply is used

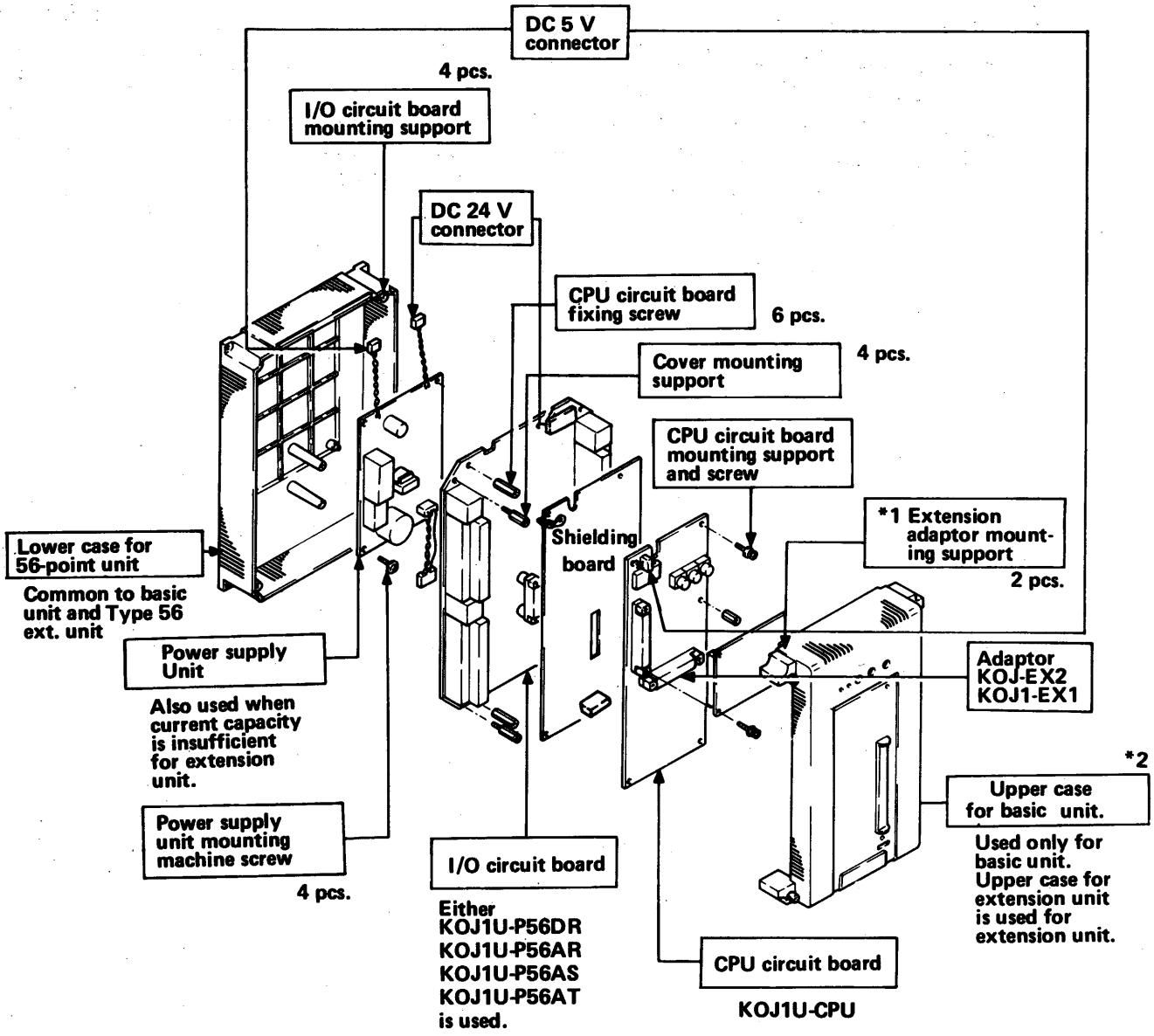


- As measures against power surge due to thunder, it is recommended to wire and ground as shown above.
- Select the varistor of surge absorber which will not cause voltage to exceed the maximum allowable value even when line voltage rises to maximum.

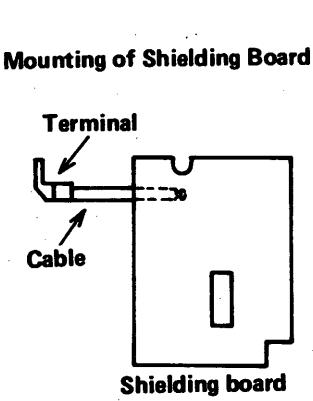
MEMO

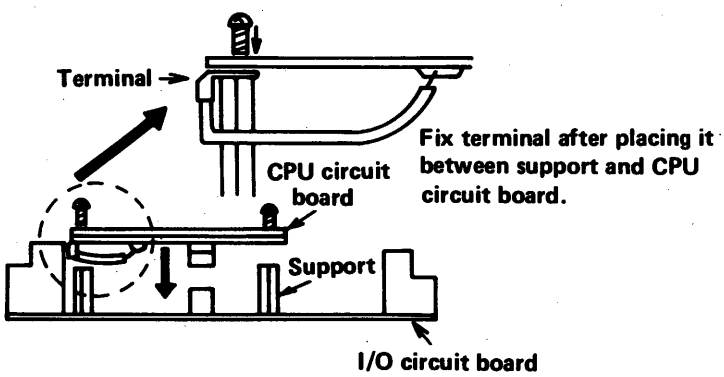
9. STRUCTURE OF UNIT

9.1 Structure of Basic Unit

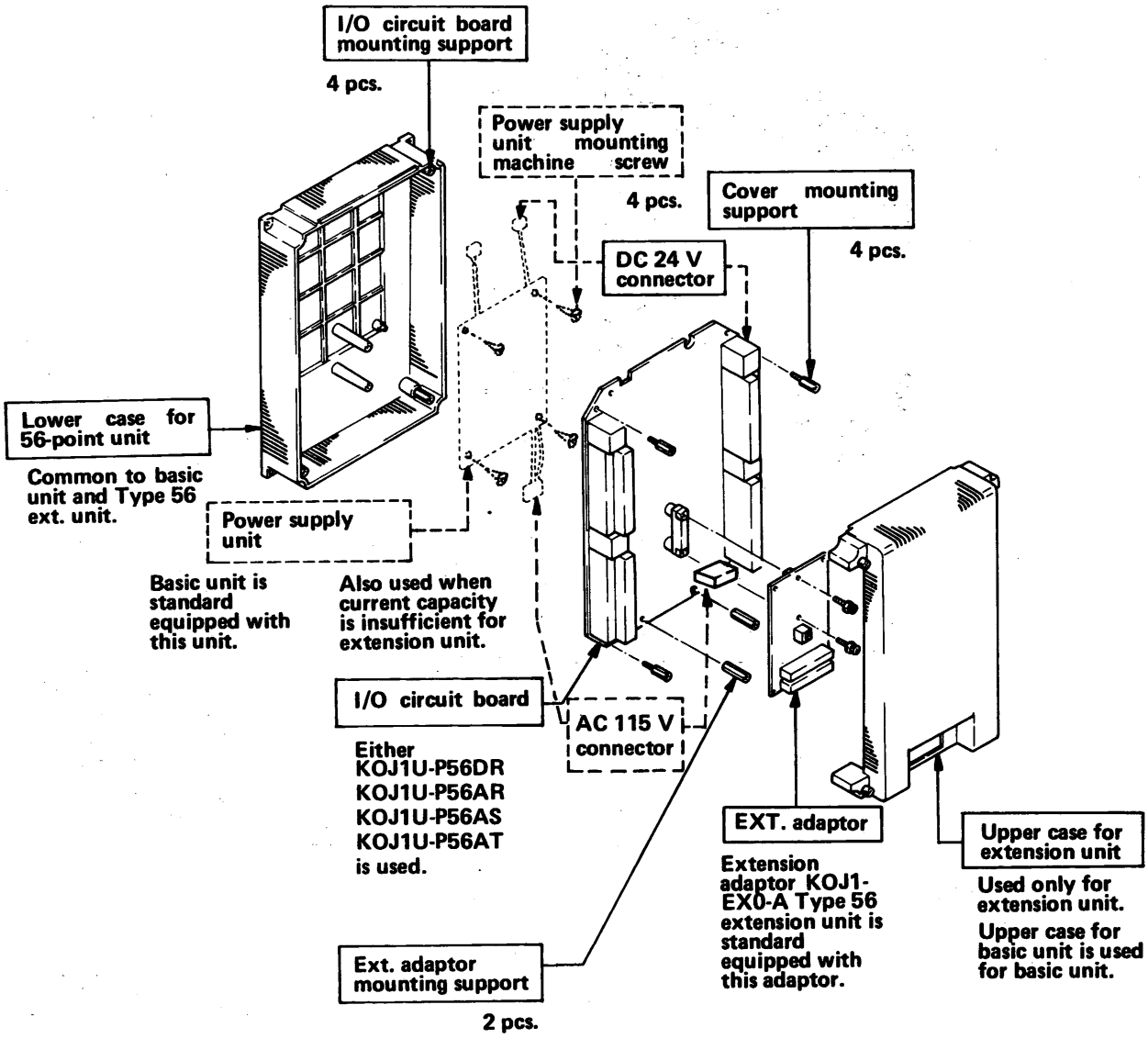


*1 When extension adaptor is used, this support is utilized. Fit it with attached screws.
*2 When extension adaptor is used, remove the cap (blind cap) located at the bottom of case.



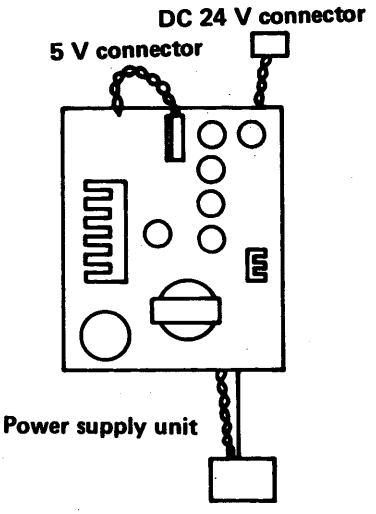


9.2 Structure of Type 56 Exention Unit

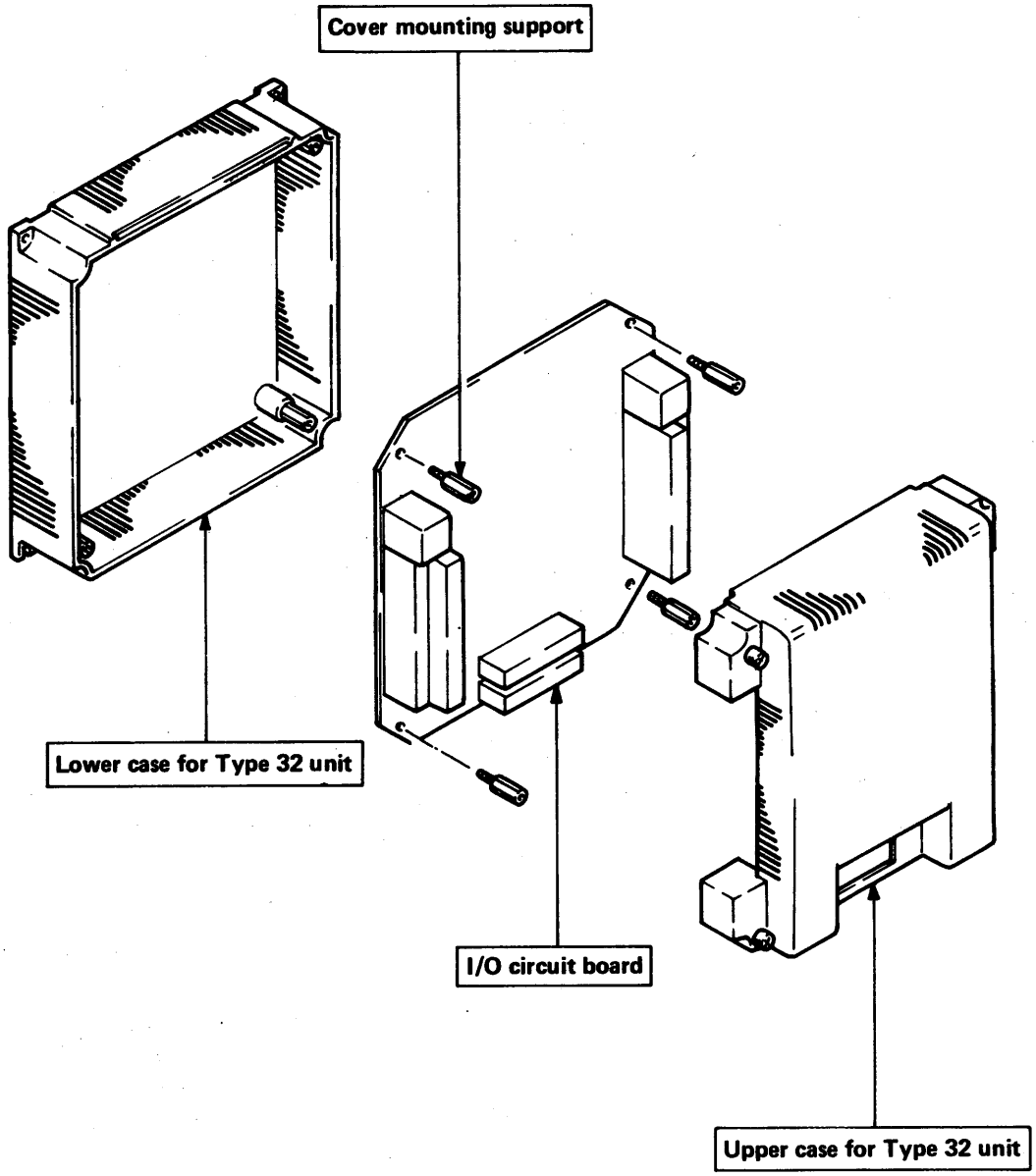


* Power Supply

When DC 24 V current capacity is insufficient for the extension unit, use the power supply unit KOJ1U-PW. In this case, DC 5 V connector is not used. Therefore, connect it with the connector in power supply unit.

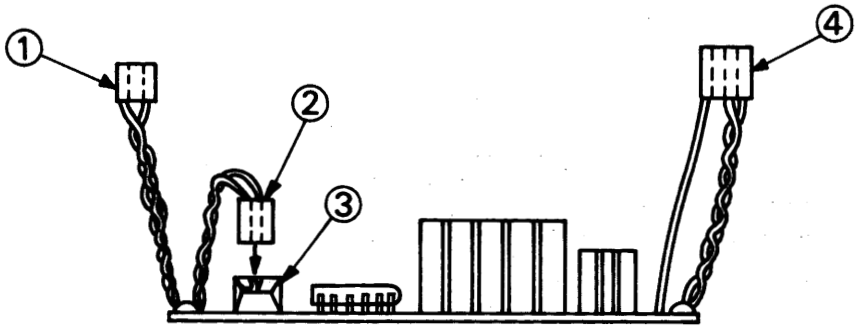


9.3 Structure of Type 32 Extension Unit



9.4 Structure of Extension Power Supply

When the capacity of power supply built in the basic unit is insufficient, provide extension power supply within the E56 extension unit.



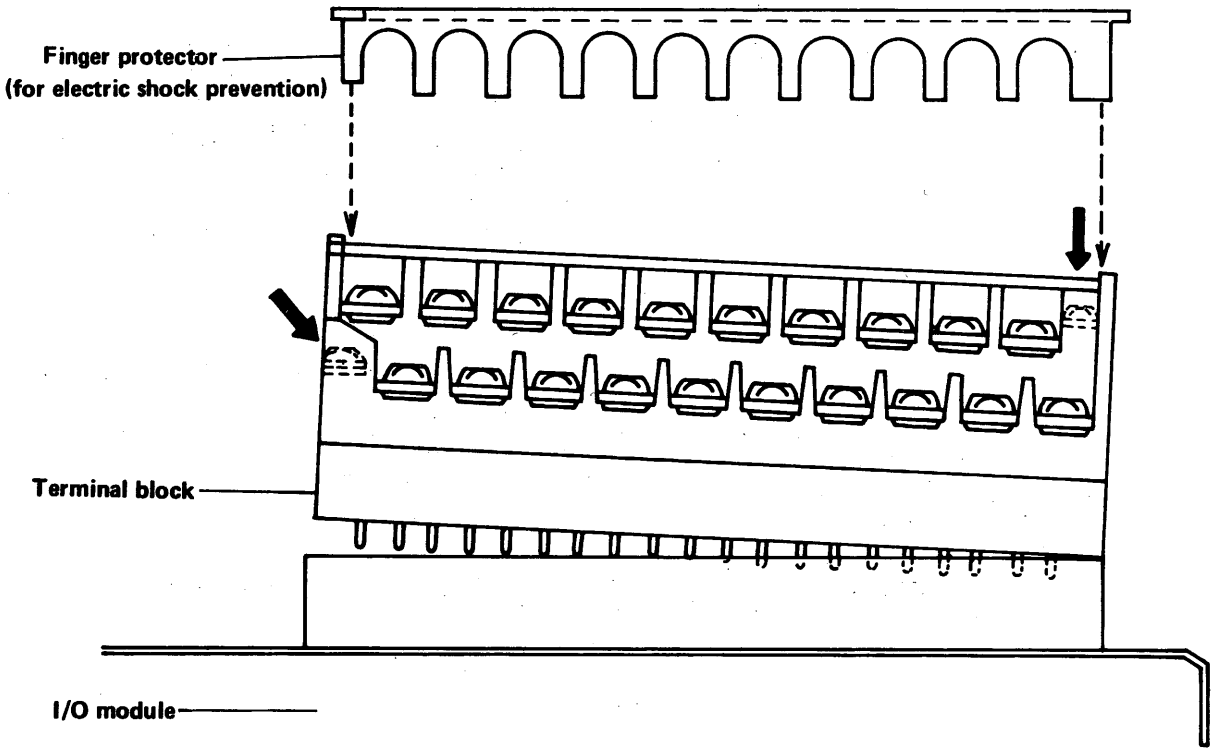
(KOJ1U-PW-DC24/KOJ1E-PW-AC220)

① Connector for DC 24 V:	Connected with specific connector in I/O unit.
② Connector for DC 5 V:	In the case of extension unit, it is not necessary to supply DC 5 V to I/O unit.
③ Connector for DC 5 V:	Before installing power supply, be sure to confirm that connectors ② and ③ are connected with each other.
④ Connector for power supply:	Connected with specific connector in I/O unit.

* The mounting procedure of extension power supply is identical to that of the basic unit. Refer to 9.1.

9.5 Loading and Unloading of I/O Module Terminal Block

Since the I/O module utilizes a 2-piece type terminal block, it can be loaded or unloaded without disconnecting cables in the terminal block. When the machine screws indicated by arrows are turned clockwise, the terminal block is gradually pushed and then fixed. Conversely, when they are turned counterclockwise, the terminal block is gradually lifted and eventually comes off of itself.



Terminal Block Specifications	
Specifications	**2-piece type w/finger protector**
Applicale cable rating	22 AWG ~ 14 AWG
Reference screw tightening torque	11.2 ± 15% kg.f.cm

10. MAINTENANCE AND INSPECTION

10.MAINTENANCE AND INSPECTION

10.1 Periodic Maintenance

The following table shows the items to be inspected daily or periodically so that the K0J1U is always operated in the best conditions.

General Items

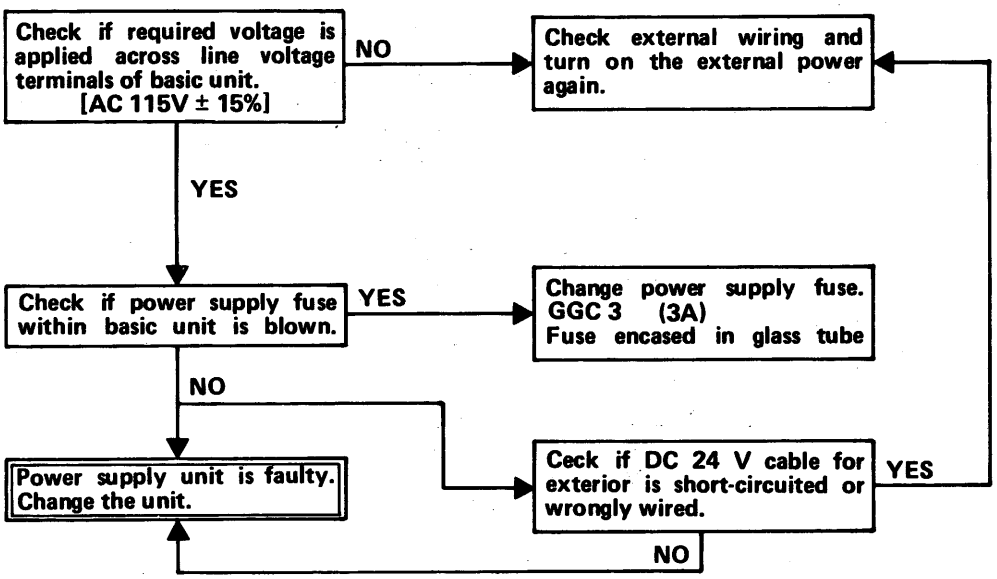
Inspection item	Inspection	Standard	Remark
Ambient temperature	Check if the items are within the range of values in specification table. (When installed inside panel, temp. within panel is regarded as ambient temperature.)	0 ~ 55°C	Check for dew condensation.
Ambient humidity		10% ~ 90% RH	
Ambience		Without dust and corrosive gases.	
Vibration		16.7Hz, double amplitude 3 mm 2 hr	
Shock		10g x 3 times in X, Y and Z directions	

Control Unit

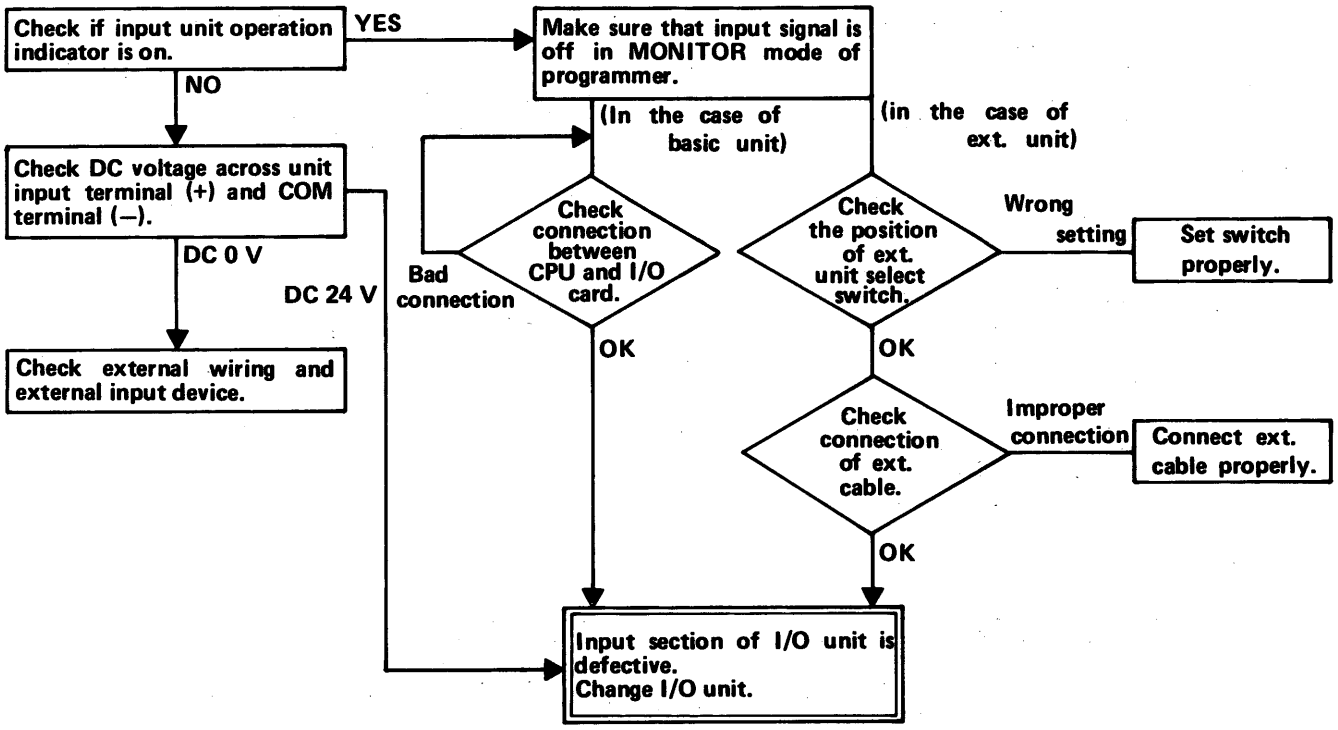
No.	Inspection Item	Inspection Method	Standard	Corrective Action
1	Voltage			
	Line voltage	Measure voltage across "POWER 1,2" terminals of basic unit with tester or synchroscope.	AC 115 V ± 15% 50, 60 Hz	Modify supply power circuit so that it becomes within the range of specification.
2	Unit mounting condition			
	① Looseness or rattle	Retighten.	Unit should be mounted firmly.	Retighten unit fixing screws.
	② Adhesion of dust or foreign materials	Visual inspection.	Free of dust or foreign materials	Remove and clean.
3	Connecting condition			
	① Loose terminal screw	Retighten.	Screws should not be loose.	Retighten.
	② Solderless terminals too close	Visual inspection.	Provide proper space.	Correct.
	③ Loose connector	Retighten.	Connectors should not be loose.	Retighten.
	④ Loose screws for wiring I/O devices	Retighten.	Screws should not be loose.	Retighten.
4	Battery	(1) Check how many years have passed since data of manufacture. (2) Make sure that M254 battery capacity reduction signal is not on.	(1) Within 5 years. battery. (2) M254 should not be on.	Change iwith spare.
5	Fuse	If fuse is not melted off, change periodically because element may be worn due to rush current.	(Preventive maintenance)	Change.
6	IC	Make sure that IC inserted in socket is set firmly.	IC should be set firmly.	Set firmly.

10.2 Checking Procedure during Abnormal Condition

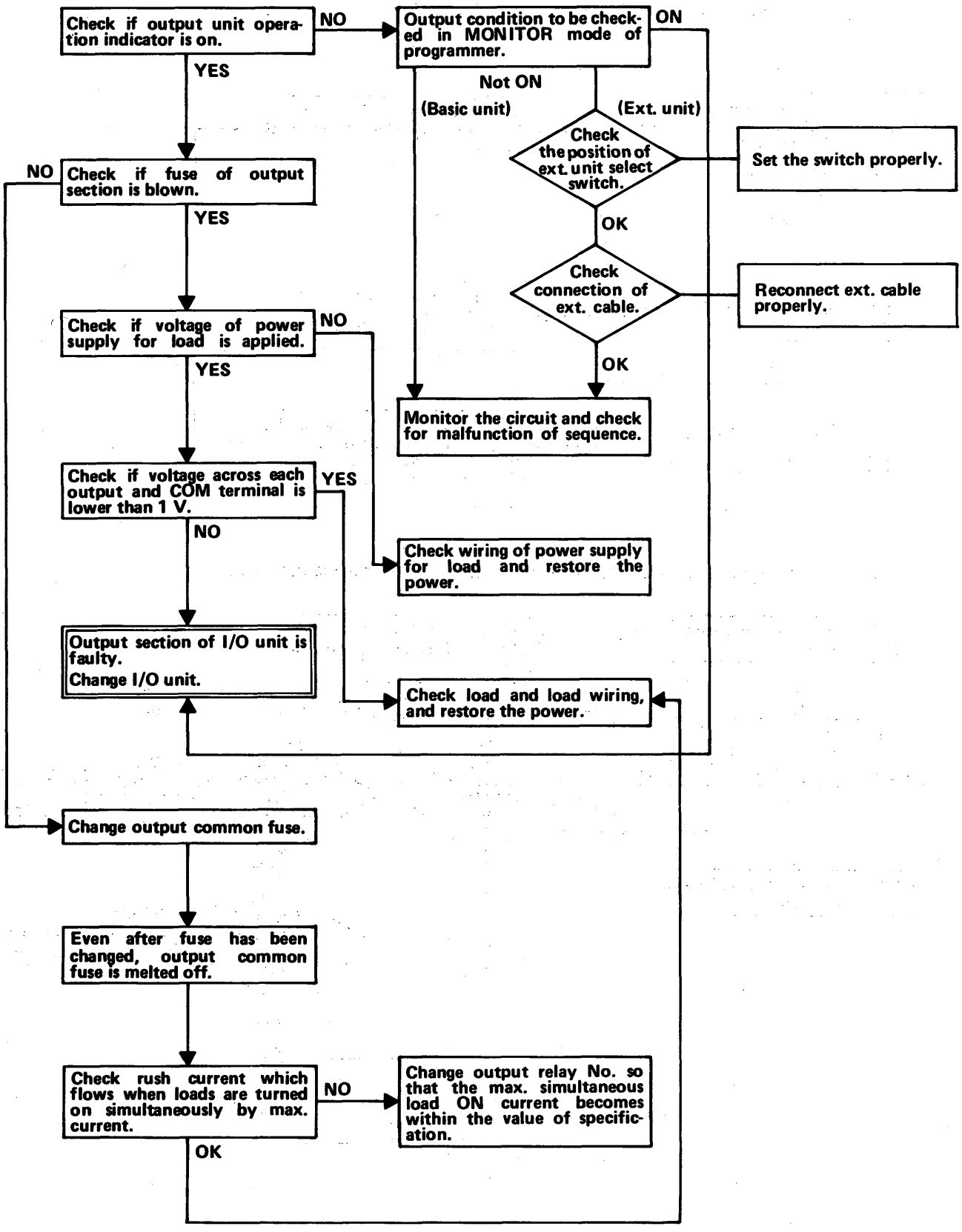
10.2.1 In case POWER indicator of basic unit is off



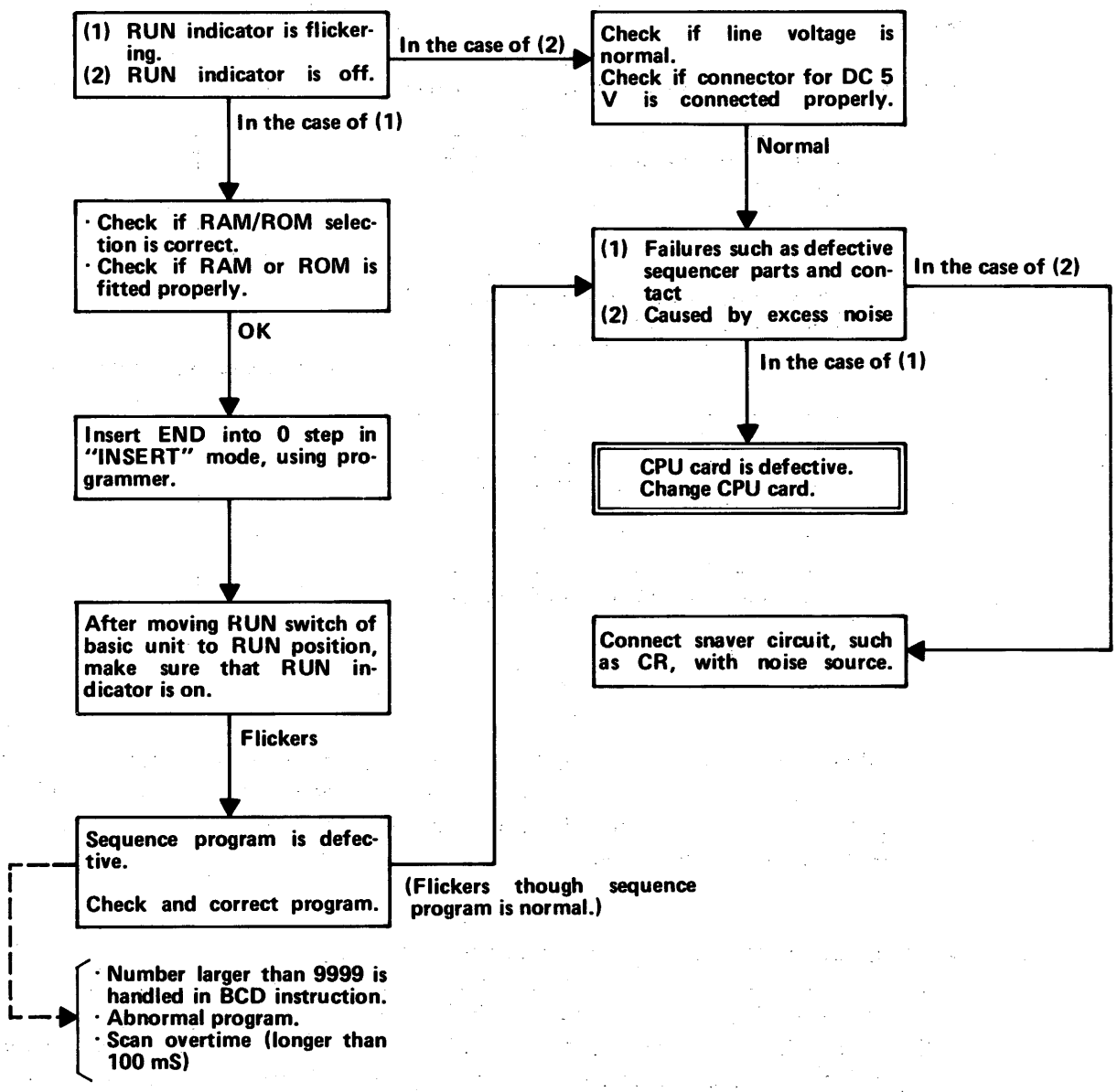
10.2.2 In case input signal fails to turn on while input device has turned on



10.2.3 In case external output load fails to turn on while output signal has turned on



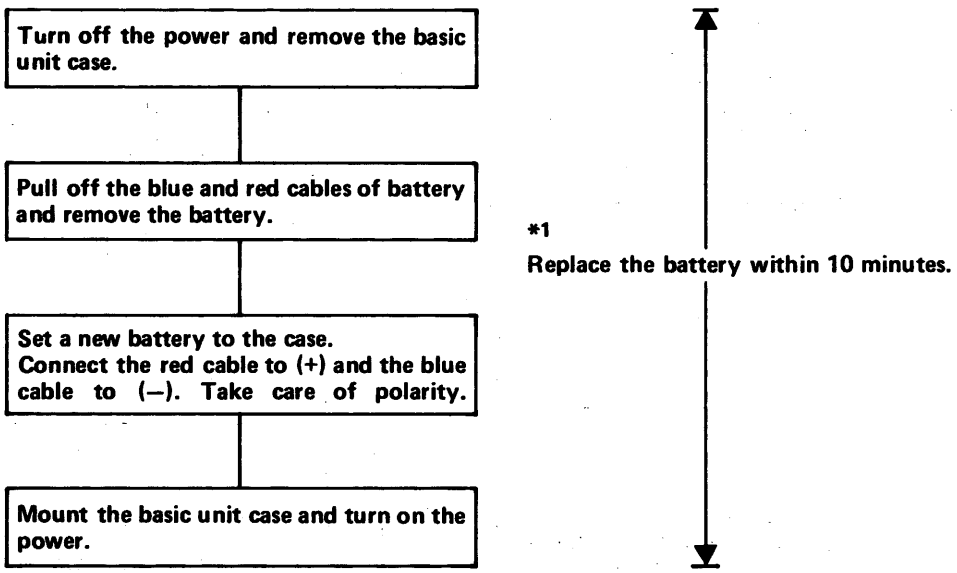
10.2.4 In case RUN indicator flickers or turns off when RUN switch of basic unit is moved to RUN position



10.3 Battery Changing Procedure

The battery for memory backup which is used for the KOJ1U gives alarm (M254) when the battery voltage (capacity) reduces. Please change the battery within one month after this alarm is given.

- When the battery abnormal relay M254 turns on



*1 When the battery is changed, the time from when the power is turned off and the battery is changed to when the power is turned on again should be within 10 minutes. If it exceeds 10 minutes, enough care should be taken because the contents of program and latch function will be cleared.

- The guides of preventive maintenance are as follows:
  1) When the battery is guaranteed within 5 years and the total power cut time is less than 300 days (7200 hours), change the battery in 4 to 5 years.
  2) When the battery is guaranteed within 5 years and the total power cut time has exceeded 300 days (7200 hours), calculate the day when the total power cut time will exceed 7200 hours, in terms of the operating hours during one day or one week and also the power cut time, thus obtaining the time to change the battery.

Example: If the operating time is 10 hours a day (i.e. power is stopped for 14 hours a day) and the power is stopped for 2 days (i.e. 24 hours) a week,

14 hours x 5 = 70 hours
24 hours x 2 = 48 hours
7200 hours/(70 + 48) hours = 61 weeks
61 weeks x 7 days/30 days = approx. 14 months

Therefore, change the battery every 14 months.

CAUTION

Since the printed circuit boards inside the KOJ1U are mounted with the electronic parts which will be adversely affected by static electricity, handle the printed circuit board as described below when they are handled directly.

(1) Ground human body and work bench.

(2) Do not touch directly the conductive area of printed circuit board and the electrical parts.

MEMO

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